

SHIFT REGISTER, DRIVER CIRCUIT AND DISPLAY DEVICE

Abstract

A shift register is configured so that each of first and
5 second intermediate stages includes (i) a first input terminal
supplied with a clock signal, (ii) a second input terminal
supplied with a clock signal different in phase from the clock
signal supplied to the first input terminal, (iii) an output
terminal connected to the first input terminal via an output
10 transistor, and (iv) a setting circuit, which is connected to the
second input terminal and the output transistor, for setting an
electric potential of a control terminal of the output transistor,
the second intermediate stage includes a control circuit which
is (i) connected to the setting circuit of the second intermediate
15 stage and (ii) supplied with a control signal, an operation period
(i) starts at a time when a shift start signal supplied to an initial
stage is activated and (ii) ends at a time when an output of a
final stage changes from activation to inactivation, and when
the clock signal supplied to the first input terminal of the
20 second intermediate stage is initially activated after the
operation period starts, the clock signal supplied to the second
input terminal of the second intermediate stage is inactive.

FIG. 1