

GOLD CONTAINING DIE BOND SHEET PREFORM SPOT-WELDED TO A
SEMICONDUCTOR BOND SITE ON A
SEMICONDUCTOR PACKAGE AND CORRESPONDING MANUFACTURING METHOD

BACKGROUND

[0001] This disclosure relates to the die bonding of semiconductor chips to ceramic or metals, and more particularly, to die bonding of semiconductor chips to semiconductor packages using a gold die bond sheet preform.

[0002] Die bonding of semiconductor chips to packages or headers typically involves metalizing the semiconductor package with gold alloy and bonding of the die to the substrate. Die bonding is of critical importance for power devices, for example, that require a high quality die bond to dissipate heat from the package, and, in some cases, provide a low impedance interface between the bottom of the die and the die bond area.

[0003] For the package manufacturer the amount of gold plated on to the semiconductor package is an important factor in the cost of the package. The thickness of the gold layer on the package must be enough to provide a secure bond surface for the die attach process. In addition, variations in die types by the same manufacturer when the die is manufactured affects die bond.

[0004] Therefore, it can be appreciated that a package that require less gold than conventional packages while still maintaining a comparable level of performance is highly desirable.

[0005] Further, a package in which the thickness of the gold at the die bond area can be easily adjusted to accommodate variations in die types and other features is also highly desirable.

INCORPORATION BY REFERENCE

[0006] WIPO Patent Publication WO 200804577 of International Application No. PCT/US2007/080552; applicant, Williams Advanced Materials, Inc.; Inventors Jech, David and Kothandapani, Ramesh is incorporated herein by reference.

BRIEF DESCRIPTION

[0007] In accordance with one aspect of the present disclosure, a method of forming a die bond site on a package includes forming a die bond sheet preform, placing the die bond sheet preform on a die bond area of the semiconductor package, and tack bonding the die bond sheet preform to the semiconductor package at more than one location.

[0008] Further in accordance with the disclosure, a gold-tin die bond sheet preform is used.

[0009] Yet further in accordance with the disclosure, a gold-tin die bond sheet preform is about 0.0005 inch (13 μ m) thick.

[0010] Still further in accordance with the disclosure, the preform is tack bonded by electric resistance welding to the package by means of an electric current that has a welding current wave form with only one principal current peak.

[0011] In accordance with another aspect, a method of forming a semiconductor bond site on a semiconductor package comprises the steps of forming a gold containing die bond sheet preform having a width, a length and a substantially uniform thickness, placing the die bond sheet preform on a die bond area on a semiconductor package, and welding the die bond sheet preform to the package die bond area at two spaced apart spots, the two spaced apart spots having a total area significantly smaller than the area of the sheet preform.

[0012] The die bond sheet preform can contain gold and tin. The die bond sheet preform can be about 0.0005 inch thick. The die bond sheet preform can be rolled to a final thickness of 0.0005 inch. The die bond sheet preform can be welded to the package die bond area with an electric current resistance welding using a welding current waveform having only one principal current peak. The welding the die bond sheet preform to the package die bond area includes using a working electrode having a very small contact area (approximately 0.3mm to 0.5mm). The method can further include placing a die on the die bond sheet preform, and attaching the die to the package die bond area by at least partially liquefying the die bond sheet preform.

The die bond sheet preform can be slightly larger than a footprint of the die. The total area of the spot welds can be approximately 0.4mm to 0.7mm.

[0013] In accordance with another aspect, a semiconductor package comprises a copper tungsten base having a die bond site and a die bond sheet containing gold and tin welded to the base die bond site in at least two locations spaced from one another.

[0014] The die bond sheet can be a preform having a thickness of about 0.0005 inch. The die bond sheet can be spot welded to the base die bond site. The at least two locations can comprise welds having an area of approx. 6.20 mm x 2.39mm.

[0015] In accordance with still another aspect, a semiconductor package is formed by forming a gold containing die bond sheet preform having a width, a length and a substantially uniform thickness, placing the die bond sheet preform on a die bond area on a semiconductor package, and welding the die bond sheet preform to the package die bond area at two spaced apart spots, the two spaced apart spots having a total area significantly smaller than the area of the sheet preform.

[0016] The die bond sheet preform can be about 0.0005 inch thick. The die bond sheet preform can be rolled to a final thickness. The die bond sheet preform can be welded to the die bond area with an electric current resistance welding using a welding current waveform having only one principal current peak. The die bond sheet preform can be spot welded to the die bond area. The at least two spots can comprise welds having an area of approx. 0.4mm to 0.7mm.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] The present disclosure is described with reference to the accompanying drawings, wherein:

[0018] FIG. 1 is a top view of an example package ready to receive semiconductor chips or dies with a gold die bond preform according to the present disclosure;

[0019] FIG. 2 is a combination cross section of the ceramic package of FIG. 1 and an electrical schematic of a method of spot welding the gold die bond strip to the ceramic package;

[0020] FIG. 3 is a top view of the ceramic package of FIG. 1 with a semiconductor chip or die bonded to the ceramic package;

[0021] FIG. 4 is a top view of a second example package ready to receive a semiconductor chip or die with a gold-tin preform in place; and,

[0022] FIG. 5 is a top view of a third example package ready to receive a semiconductor chip or die with a gold-tin preform in place.

[0023] Corresponding reference characters indicate corresponding parts throughout the several views. The elements in the drawings have not necessarily been drawn to scale in order to better illustrate the features of the disclosure. The example set out herein illustrates one embodiment of the disclosure but should not be construed as limiting the scope of the disclosure in any manner.

DETAILED DESCRIPTION

[0024] Referring to FIG. 1, one exemplary embodiment 10 of the present disclosure includes a dual chip package 12 with rectangular gold, or a gold alloy such as AuSn and AuGe, die bond sheet preforms 14 attached to die bond areas 16. The die bond sheet preforms 14 are secured by tack welds 18 with two spaced apart welds for each die bond sheet preform 14. While two spaced apart welds are illustrated, it will be appreciated that more or fewer welds could be used depending on the application. However, in most applications, two spaced apart welds as illustrated is preferred. Each die bond sheet preform 14 is solder that will be used to bond a die to the package 12 in a subsequent step.

[0025] The illustrated package 12 (sometimes called a header) has positions for mounting two dies. Other packages or headers have a position for mounting a single semiconductor die only, or more than two dies. Such single and multiple position headers are otherwise identically used in the present disclosure.

[0026] The exemplary package or header 12 is a copper-tungsten mix which is often used in headers to provide electrical conductivity, thermal conductivity, and heat resistance. The package 12 has horizontal members 20 which span the width of the package 12 and are electrically connected to conductive regions 22 and 24 on the ceramic. Two upper leads 26 and 28 are electrically and thermally connected to conductive regions 30 and 32 on the package. The conductive regions 30 and 32 include the die bond regions 16. Two lower leads 34 and 36 are electrically and thermally connected to conductive regions 38 and 40.

[0027] One exemplary application of the current disclosure is the mounting of gallium nitride semiconductor dies to copper tungsten packages 12. Bonding of gallium nitride to copper tungsten is better if a gold, tin mixture is used as the bonding material (e.g., a preform of gold-tin).

[0028] The thickness of the gold-tin die bond sheet preform should be thick enough for a reliable die bond of a semiconductor die to the package 12. The preferred thickness is about 0.0005 inch (13 μ m), for example. The gold-tin die bond sheet preform is about the same size as the die or generally only slightly larger than the bottom of the die to be mounted thus minimizing the amount of gold used.

[0029] As compared to conventional techniques including gold plating applied to larger areas, the amount of gold used in accordance with the present disclosure for mounting the die on the package is less. Moreover, as compared to the plating process, the present disclosure is less time consuming and less costly. Accordingly, avoiding the plating process reduces costs. The process described in accordance with the present disclosure can be used with headers and packages which are not gold plated or only very thinly gold plated. The use of the gold-tin sheet preform provides reliable die bonding with a minimum amount of gold.

[0030] Turning now to FIG. 2, the preforms 14 are attached to the package 12 by tack welds 18. It will be appreciated that the tack welds 18 should be strong enough to keep the gold-tin die bond sheet preform 14 attached to the package 12 until a die is attached to the package. The tack welds 18 are formed using a tack welder having welding electrodes 46 (only one is schematically shown in FIG. 2), an

electrical power supply 48, and a work piece contact 50. The work piece contact 50 is pressed onto the appropriate lead 26 or 28 and the electrodes 46 are pressed onto the corresponding gold-tin die bond preform 14 at the tack weld positions 18, as shown in FIG. 2. The welding electrodes 46 have working ends with a very small area of contact (e.g., 1mm to 1.5mm) when brought against the preform 14. This creates very small welds 18 between the preform 14 and the package 12.

[0031] Applicants have found that the welds 18 can be very small and still hold the preform in place because two spaced apart welds are created in each preform 14. Two small, spaced welds 18 reliably hold the preform 14 in place to prevent both lateral and rotational movement of the preform 14 relative to the package 12. In one embodiment, the welds are approximately 0.3mm to 0.5mm.

[0032] The gold-tin sheet for use in accordance with the present disclosure is originally a uniform mix of gold and tin. Gold-tin foil or sheet can be changed by melting and resolidification. For example, the gold and tin can separate in what is sometimes called phase separation. If this occurs to a large portion of the gold-tin sheet used to bond a die to a package, the bond may be compromised to the point of unreliability.

[0033] It will be appreciated that when the die is attached, the gold die bond sheet preform must at least partially liquefy and bond to both the die and the package. Accordingly, care should be taken to minimize phase separation issues during the spot welding.

[0034] In accordance with the present disclosure, phase separation issues are minimized by i) creating only very small weld areas (areas of melting), and ii) by applying welding current to the electrodes with a single principal current peak. Dual pulse resistance welding is performed to bond the gold-tin preforms onto the package.

[0035] In some spot welding approaches, a preheat current is applied prior to the current expected to create the weld. Applicants have found that these approaches can cause phase separation issues with a gold-tin preform.

[0036] In accordance with the present disclosure applicants concentrate current in one peak during the spot welding process to avoid phase separation issues that occur in other spot welding approaches.

[0037] FIG. 3 shows the package 12 after semiconductor chips 52 and 54 have been die bonded onto the package 12. In one particular embodiment the chips 52 and 54 cover about 98% of the area of the die bond sheet preforms 14.

[0038] While the gold-tin die bond sheet preform shown in the drawings is rectangular, the preform will be generally shaped to the contour of the bottom of the die. Virtually any desired shape preform can be used in accordance with the present disclosure.

[0039] FIGS. 4 and 5 show examples of packages or headers with a gold-tin preform attached. A gold-tin sheet is first rolled or otherwise processed to a sheet of .0005" thick, for example. The gold-tin sheet is then cut to dimensions appropriate for the die to be mounted. For instance, a die size of 20 mm x 1.2 mm might call for a preform measuring 2.1 mm x 1.3 mm. The thickness can remain 0.0005" for all sizes. This size preform provides adequate solder volume for this size die.

[0040] It will be appreciated that the preforms 14 should be placed with precision in the location where the die is to be mounted to the package 12 so the solder (gold-tin) is where it can be used in bonding. Accordingly, very tight tolerances are used in preform attachment. This becomes very important when the die is placed for attachment. Often the die is placed on the package or header without pressure applied. If the preform on which the die is placed is not anchored, the die may move. In the illustrated embodiments, the preform is held in place by the tack welds such that the die does not move and is mounted at its intended location.

[0041] As described above, since the entire package does not have to have enough gold plating for reliably die bonding a chip to the package, the total amount of gold used on the package, including the gold-tin die bond sheet preform, is significantly reduced as compared to other method such as plating. Since the cost of manufacturing a custom thickness gold die bond sheet preform is much less than manufacturing a package with a custom thickness of gold plating, the cost of each of

the packages for a new die type is reduced, which can become significant for small package orders by the semiconductor manufacturer.

[0042] While the disclosure has been described with reference to particular embodiments, it will be understood by those skilled in the art that various changes may be made and equivalents may be substituted for elements thereof without departing from the scope of the disclosure. In addition, many modifications may be made to adapt a particular situation or material to the teachings of the disclosure without departing from the scope of the disclosure.

[0043] Therefore, it is intended that the disclosure not be limited to the particular embodiments disclosed as the best mode contemplated for carrying out this disclosure, but that the disclosure will include all embodiments falling within the scope and spirit of the appended claims and the equivalents thereof.

CLAIMS:

1. A method of forming a semiconductor bond site on a semiconductor package comprising the steps of:

forming a gold containing die bond sheet preform having a width, a length and a substantially uniform thickness;

placing the die bond sheet preform on a die bond area on a semiconductor package; and

welding the die bond sheet preform to the package die bond area at two spaced apart spots, the two spaced apart spots having a total area significantly smaller than the area of the sheet preform.

2. The method of claim 1, wherein the die bond sheet preform contains gold and tin.

3. The method of claim 1, or any other preceding claim, wherein the die bond sheet preform is about 0.0005 inch thick.

4. The method of claim 3, or any other preceding claim, wherein the die bond sheet preform is rolled to a final thickness.

5. The method of claim 1, or any other preceding claim, wherein the die bond sheet preform is welded to the package die bond area with an electric current resistance welding using a welding current waveform having only one principal current peak.

6. The method of claim 1, or any other preceding claim, wherein the welding the die bond sheet preform to the package die bond area includes using a working electrode contact area of approximately 6.2mm x 2.39mm.

7. The method of claim 1, or any other preceding claim, further comprising placing a die on the die bond sheet preform.

8. The method of claim 7, or any other preceding claim, further comprising attaching the die to the package die bond area by at least partially liquefying the die bond sheet preform.

9. The method claim 7, or any other preceding claim, wherein the die bond sheet preform is slightly larger than a footprint of the die.

10. The method of claim 1, or any other preceding claim, wherein the total area of the spot welds is approximately 0.3mm to 0.5mm.

11. A semiconductor package comprising a copper tungsten base having a die bond site and a die bond sheet preform containing gold and tin welded to the base die bond site in at least two locations spaced from one another.

12. The semiconductor package of claim 11, wherein the die bond sheet preform is a preform having a thickness of about 0.0005 inch.

13. The semiconductor package of any one of claims 11-12, wherein the die bond sheet preform is spot welded to the base die bond site.

14. The semiconductor package of any one of claims 11-13, wherein the at least two location comprise welds having an area of approximately 0.3mm to 0.5mm.

15. A semiconductor package formed by:
forming a gold containing die bond sheet preform having a width, a length and a substantially uniform thickness;

placing the die bond sheet preform on a die bond area on a semiconductor package;

welding the die bond sheet preform to the package die bond area at two spaced apart spots, the two spaced apart spots having a total area significantly smaller than the area of the sheet preform.

16. The semiconductor package of claim 15, wherein the die bond sheet preform is about 0.0005 inch thick.

17. The semiconductor package of any one of claims 15-16, wherein the die bond sheet preform is rolled to a final thickness.

18. The semiconductor package of any one of claims 15-17, wherein the die bond sheet preform is welded to the die bond area with an electric current resistance welding using a welding current waveform having only one principal current peak.

19. The semiconductor package of any one of claims 15-18, wherein the die bond sheet preform is spot welded to the die bond area.

20. The semiconductor package of any one of claims 15-19, wherein the at least two spots comprise welds having an area of approximately 6.2mm x 2.39mm.