CLAIMS

1. A semiconductor substrate processing system, comprising:

a chamber having a top structure, a bottom structure, and sidewalls extending between the top and bottom structures, the chamber including a processing region;

a substrate support disposed within the chamber, the substrate support having a top surface defined to support a substrate in exposure to the processing region;

a top plate assembly disposed within the chamber above the substrate support, the top plate assembly having a lower surface exposed to the processing region and opposite the top surface of the substrate support, the top plate assembly including:

a first set of plasma microchambers each formed into the lower surface of the top plate assembly,

a first network of gas supply channels formed to flow a first process gas to each of the first set of plasma microchambers, each of the first set of plasma microchambers defined to transform the first process gas into a first plasma in exposure to the processing region,

a set of exhaust channels formed through the lower surface of the top plate assembly to provide for removal of exhaust gases from the processing region,

a second set of plasma microchambers respectively formed inside the set of exhaust channels, and

a second network of gas supply channels formed to flow a second process gas to each of the second set of plasma microchambers, each of the second set of plasma microchambers defined to transform the second process gas into a second plasma in exposure to the processing region.

2. A semiconductor substrate processing system as recited in claim 1, wherein the first set of plasma microchambers are interspersed with the second set of plasma microchambers in a substantially uniform manner across the lower surface of the top plate assembly.

3. A semiconductor substrate processing system as recited in claim 1, further comprising:

a first power supply defined to supply a first power to the first set of plasma microchambers;

a first process gas supply defined to supply a first process gas to the first network of gas supply channels;

a second power supply defined to supply a second power to the second set of plasma microchambers; and

a second process gas supply defined to supply a second process gas to the second network of gas supply channels.

4. A semiconductor substrate processing system as recited in claim 3, wherein either the first and second power supplies are independently controllable, or the first and second process gas supplies are independently controllable, or both the first and second power supplies and the first and second process gas supplies are independently controllable.

5. A semiconductor substrate processing system as recited in claim 3, further comprising:

a first set of power delivery components respectively disposed within the top plate assembly about the first set of plasma microchambers, each of the first set of power delivery components connected to receive the first power from the first power supply; and

a second set of power delivery components respectively disposed within the top plate assembly about the second set of plasma microchambers, each of the second set of power delivery components connected to receive the second power from the second power supply.

6. A semiconductor substrate processing system as recited in claim 5, wherein each power delivery component of the first set of power delivery components is defined as a respective coil.

7. A semiconductor substrate processing system as recited in claim 5, wherein each power delivery component of the second set of power delivery components is defined as a respective coil.

8. A semiconductor substrate processing system as recited in claim 1, wherein the first and second sets of plasma microchambers are defined to operate in either a simultaneous manner or a pulsed manner, wherein the pulsed manner includes either the first set of plasma microchambers or the second set of plasma microchambers operating at a given time and in an alternating sequence.

9. A semiconductor substrate processing system as recited in claim 1, wherein the substrate support is defined to be movable in a direction perpendicular to both the top surface of the substrate support upon which the substrate is to be supported and the lower surface of the top plate assembly.

10. A semiconductor substrate processing system as recited in claim 1, wherein the substrate support includes an electrode defined to apply a bias voltage across the processing region between the substrate support and the lower surface of the top plate assembly.

11. A semiconductor substrate processing system as recited in claim 1, wherein each plasma microchamber of the first set of plasma microchambers is formed in part by a respective cavity recess defined to extend from the lower surface of the top plate assembly into the top plate assembly.

12. A semiconductor substrate processing system as recited in claim 1, wherein each plasma microchamber of the first set of plasma microchambers includes a respective outlet of the first network of gas supply channels.

13. A semiconductor substrate processing system as recited in claim 1, wherein each plasma microchamber of the second set of plasma microchambers is formed in part by a portion of a respective exhaust channel located adjacent to an inlet of the respective exhaust channel at the lower surface of the top plate assembly.

14. A semiconductor substrate processing system as recited in claim 1, wherein each plasma microchamber of the second set of plasma microchambers includes a respective outlet of the second network of gas supply channels.

15. A semiconductor substrate processing system as recited in claim 1, wherein the second network of gas supply channels is formed physically separate from the first network of gas supply channels, such that the first and second networks of gas supply channels are fluidly isolated from each other upstream of the first and second sets of plasma microchambers.

16. A semiconductor substrate processing system as recited in claim 1, wherein first process gas is fluidly isolated from the second process gas upstream of the first and second sets of plasma microchambers.

17. A semiconductor substrate processing system as recited in claim 1, wherein each exhaust channel of the set of exhaust channels is formed to extend through an entirety of the top plate assembly in a direction perpendicular to the lower surface of the top plate assembly.

18. A semiconductor substrate processing system as recited in claim 17, wherein a portion of each gas supply channel of the second network of gas supply channels is formed to extend through a portion of the top plate assembly in an angled direction to a respective exhaust channel of the set of exhaust channels.

19. A semiconductor substrate processing system as recited in claim 1, further comprising:

an exhaust pump connected to apply fluid suction to the set of exhaust channels.