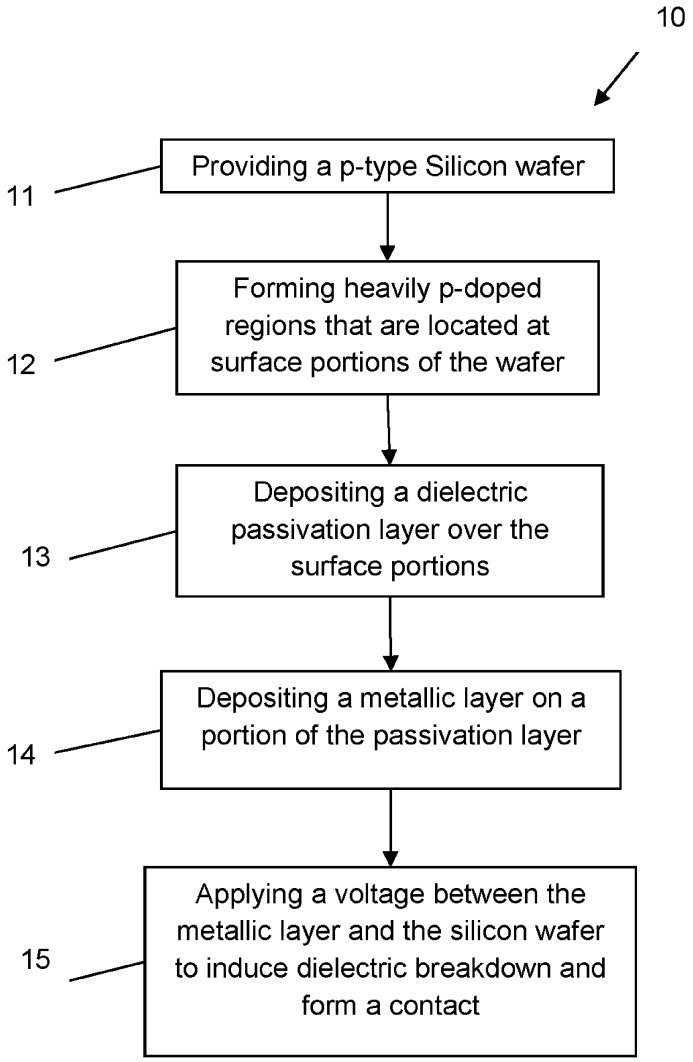

10
Providing a p-type Silicon wafer
11
Forming heavily p-doped regions that are located at surface portions of the wafer
12
Depositing a dielectric passivation layer over the surface portions
13
Depositing a metallic layer on a portion of the passivation layer
14
Applying a voltage between the metallic layer and the silicon wafer to induce dielectric breakdown and form a contact
15

Figure 1

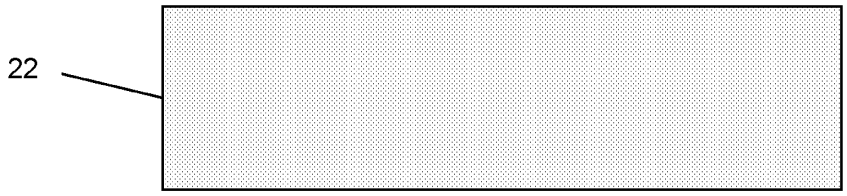


Figure 2

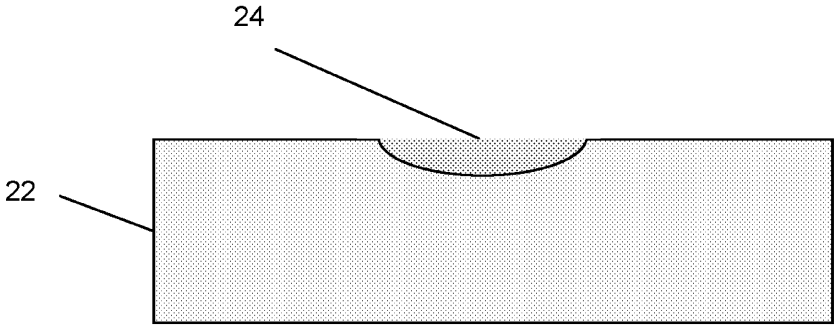


Figure 3

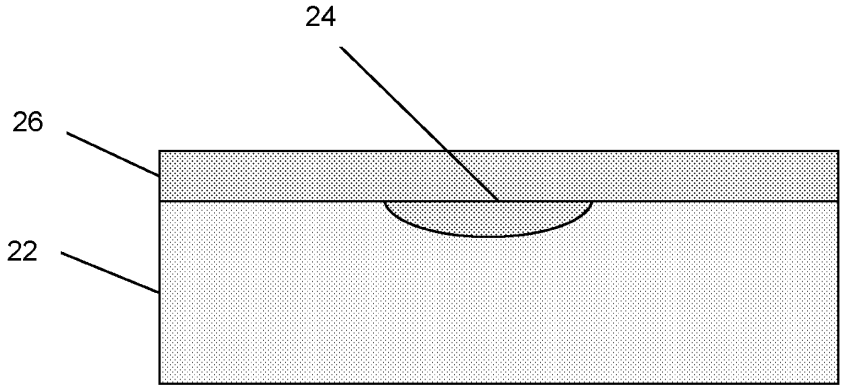


Figure 4

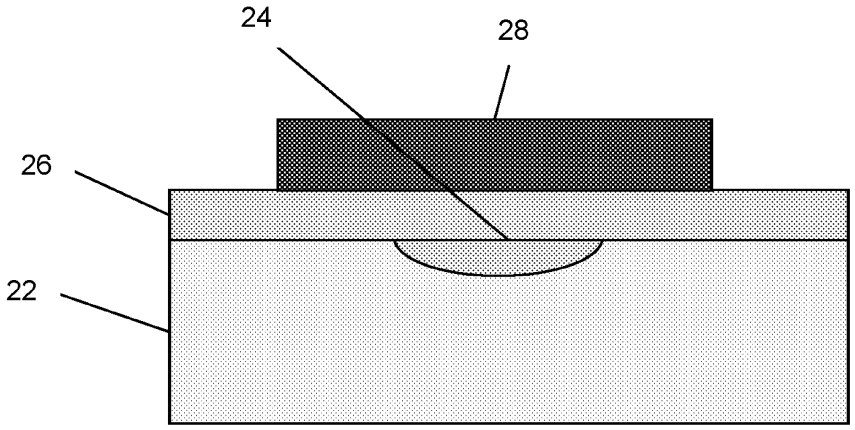


Figure 5

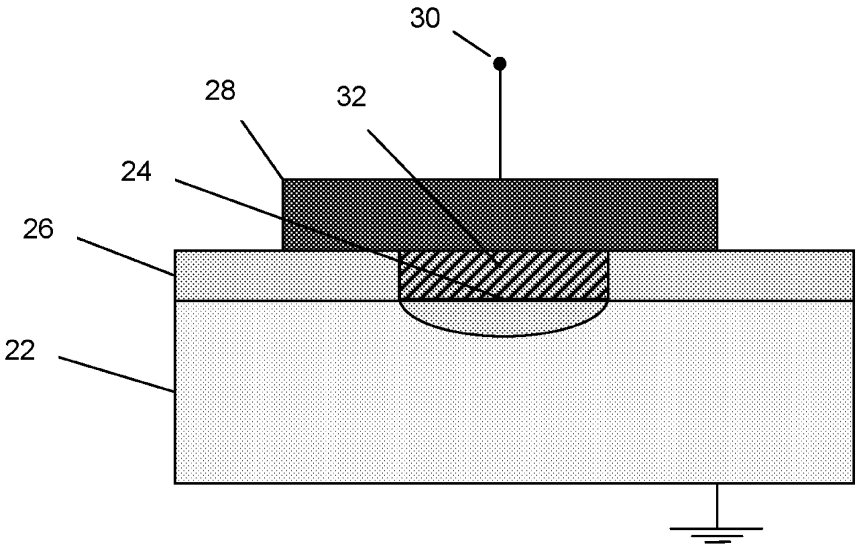


Figure 6

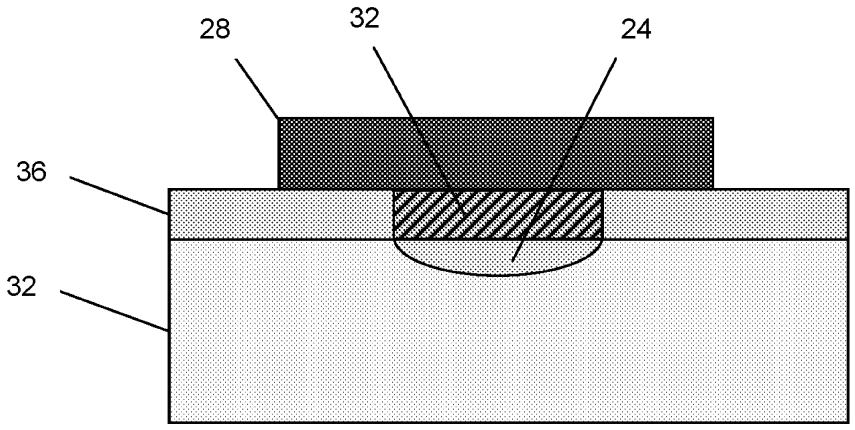


Figure 7