

PATENT SPECIFICATION

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(54) LOGIC GATES

(71) We, TELETYPE CORPORATION, of 5555, Touhy Avenue, Skokie, Cook County, State of Illinois, United States of America, a Corporation organised under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to logic gates. Preferred embodiments include MOS circuit gates suitable for fabrication by integrated circuit techniques.

Existing integrated circuit logic gates often employ field effect transistors as internal load drain devices, thereby requiring that a bias current from a power supply be supplied to the circuit. The energy supplied from the power supply is dissipated on the circuit chip, limiting the packing density obtainable. Also more than the minimum number of circuit devices are employed. A further disadvantage is that the necessary power supply leads increase circuit complexity.

According to the invention there is provided a logic gate comprising means responsive to each of at least two input bit signals for providing that bit signal and its inverse on distinct leads, at least two switching circuits, each having first and second input terminals and an output terminal respectively, the output terminal of each switching circuit except the last being connected to the first input terminal of the next succeeding switching circuit, and each connected to be controlled by signals on a pair of the distinct leads corresponding to a different said input bit signal to interconnect its output terminal and its first or its second input terminal depending on the value of the corresponding said bit signal, whereby, in operation, the output terminal of the last switching circuit is, in response to only one predetermined combination of said bit signals, energized to correspond with a predetermined energisation of the first input terminal of the

first switching circuit to produce a unique output signal.

Advantageously a field effect transistor gate structure may be provided wherein the only current required by the circuit is that supplied to an output load device which is driven by the circuit. Furthermore, said output load current may be supplied by the inputs to the circuit.

The first terminal of the first switching circuit may be connected to a first constant voltage source, and the second input terminal of each switching circuit may be connected to a second different constant voltage source.

Alternately, the first input terminal of the first switching circuit is connected to receive a signal based on a further input bit signal, and the second input terminal of each switching circuit is connected to that one of the associated pair of leads that is to be energised similarly to the output terminal of the last switching stage for said only one predetermined combination of input bit signals and said predetermined energisation of the first input terminal of the first switching circuit.

Preferably, MOS devices are arranged in a MOSFET coincidence gate circuit for producing an output signal to charge a capacitor only in response to one selected combination of a plurality of binary data signals, and for discharging the capacitor, if previously charged, for all other combinations of the data signals. Phase splitters provide two input signals for each binary data signal, one corresponding to the binary data signal and one to its complement. A plurality of logic-steering FETs ("LFs") are arranged in a sequence such that each has its gate connected to a first one of the input signals for an associated bit selected such that each LF becomes conductive only when the associated bit assumes the selected state. A capacitor-charging signal is supplied to a first controlled terminal of the first LF in the sequence, and each subsequent LF has its first controlled terminal connected in series with the second controlled terminal

of the preceding LF. The output capacitor is connected to the second controlled terminal of the last LF in the sequence so that the capacitor is connected to the charging signal through all the LFs only whenever all of the LFs have been rendered conductive in response to the selected combination of the binary input signals. A plurality of ground-return FETs ("GFs") are arranged in a sequence corresponding to that of the LFs, each having its gate connected to the second input signal for an associated binary data signal such that each GF becomes conductive only when the associated binary data signal assumes the non-selected state. The last GF in the sequence has its controlled terminals connected in series between the output capacitor and a source of ground potential to provide a ground-discharge path for the capacitor whenever the last binary data signal assumes the non-selected state. Each preceding GF is connected in series between the first controlled terminal of the following LF and a source of ground potential to provide a ground-discharge path for the capacitor whenever the associated bit assumes the nonselected state and all following bits have assumed the selected state.

Two embodiments of the invention will now be described, by way of example, with reference to the accompanying drawing, in which:—

Fig. 1 is a circuit diagram of a first embodiment of the invention;

Fig. 2 is a truth table describing the logic performed by the circuit of Fig. 1;

Fig. 3 is a circuit diagram of a second embodiment of the invention; and

Fig. 4 is a truth table describing the logic performed by the circuit of Fig. 3.

The gate circuit structures of Figs. 1 and 3 are shown as applied to MOSFET (metal-oxide-silicon field-effect transistor) integrated circuits using P-channel enhancement-mode devices. Each field effect transistor employed is characterised in that a negative voltage applied to its gate will cause a low impedance between a pair of controlled terminals, while a ground potential applied to its gate will cause a high impedance between its controlled terminals. Although the ensuing description concerns P-channel enhancement-mode devices, it should be understood that the principles of the invention apply equally well to circuits using different types of field-effect devices.

Fig. 1 shows a gate using MOS field effect transistors as the primary elements of each stage of the gate, the function of which gate being defined by the truth table shown in Fig. 2. The circuit contains two identical circuits 10 and 11, each enclosed in dashed lines, which serve as basic building blocks for embodiments of this invention. Each identical circuit, such as circuit 10, includes two field effect transistors such as transistors 12 and

13. The transistor 12 serves as a logic steering device while the transistor 13 serves as a ground return device. The circuit 11 employs a logic steering transistor 14 and a ground return transistor 16.

In operation two separate binary data signals, in which a "1" is represented by a $-V$ potential and "0" is represented by ground potential, are applied to input terminals A and B. The input terminals A and B are connected to the circuits 10 and 11 by two phase splitters 17 and 18. Each phase splitter has a signal input terminal A and B, respec-

tively, and two output terminals A and $\bar{A}$,

and B and $\bar{B}$, respectively. A signal will appear on output terminal A which is identical to the signal applied to the input terminal A while the complement thereof will appear

on output terminal $\bar{A}$. In a like manner the signal applied to the input terminal B will appear on the output terminal B while the complement thereof will appear on output

terminal $\bar{B}$. One compatible form of phase splitter, using MOS integrated circuits, is disclosed in our copending British application No. 21772/70 (Serial No. 1,310,930). It should also be apparent that a simple inverter circuit could be used to provide the same function as a phase splitter 17 or 18. When an inverter is employed, the input terminals A and B would also serve as output terminals A and B, respectively.

In the specific example of Fig. 1, the circuit is connected to provide an output only when the inputs A and B are both "0". When this preset combination is applied, the two outputs,

A and $\bar{A}$, of the phase splitter 17 will provide a "0" and "1" respectively. The "1"

provided at the output $\bar{A}$ is applied to the gate of the transistor 12, thereby rendering the transistor 12 conductive and allowing it to pass a $-V$ potential applied to a terminal 22 to a terminal 24 of the transistor 14. The "0" obtained from the output A of the phase splitter 17 is applied to the gate of the transistor 13. However, the characteristic of the transistor 13 is such that a "0" applied to its gate will not render it conductive; therefore the transistor 13 is unable to pass a ground potential applied to a terminal 27 to the terminal 24 of the transistor 14.

The "0" at the input B of the phase splitter 18 provides a "0" and "1" at the two outputs,

B and $\bar{B}$ respectively. The "1" appearing at

the output $\bar{B}$ of the phase splitter 18 is applied to the gate of the transistor 14, rendering the transistor 14 conductive and allowing it to pass

the $-V$ potential appearing at the terminal 24 to a load device, such as an output capacitor X_1 . This capacitor X_1 preferably consists of the distributed capacitance between the transistors 14 and 16 and a transistor 25 of a succeeding circuit (shown in dashed lines) plus the insulated gate capacitance of the transistor 25. The "0" appearing at the output B of the phase splitter 18 and applied to the gate of the transistor 16 will not render the transistor 16 conductive; therefore the transistor 16 is unable to pass a ground potential applied to a terminal 34 to the output capacitor X_1 .

It is seen that by the proper coincidence of inputs the transistors 12 and 14 have been enabled to steer the $-V$ potential appearing at the terminal 22 of the transistor 12 through the transistors 12 and 14 to the output capacitor X_1 ; and the transistors 13 and 16 have been prevented from coupling the ground potential appearing at the terminals 27 and 34, respectively, to the output capacitor X_1 . This condition is indicated in the last line of Fig. 2.

Assume that an input wherein A is "1" and B is "0" is applied to the gate circuit, so that the condition for obtaining a "1" output from the circuit as shown by the truth table of Fig. 2, is not met. The outputs obtained at

A and $\bar{A}$ of the phase splitter 17 will be "1" and "0" respectively. The "0" obtained from

the output $\bar{A}$ is applied to the gate of the transistor 12, thereby preventing the $-V$ potential on the terminal 22 of the transistor 12 from being passed through the transistor 12 to the terminal 24 of the transistor 14. The "1" obtained from the output A of the phase splitter 17 and applied to the gate of the transistor 13, however, will enable the transistor 13 to conduct and pass the ground potential applied to the terminal 27 through the transistor 13 to the terminal 24 of the transistor 14.

The "1" obtained from the output $\bar{B}$ of the phase splitter 18 and applied to the gate of the transistor 14 will render the transistor 14 conductive and enable it to pass the ground potential at the terminal 24 to the output capacitor X_1 . The "0" obtained from the output B of the phase splitter 18 and applied to the gate of the transistor 16 fails to render the transistor 16 conductive. If a "1" were initially stored on the output capacitor X_1 , it will be discharged to ground through the transistors 14 and 13 which have been rendered conductive by the signals "1" and "0" appearing on the inputs A and B, respectively. Similarly, all signals applied to the inputs A and B other than "0" and "0", respectively, will fail to provide a "1" at the output capacitor X_1 , since the $-V$ potential will be

blocked by one or both steering transistors 12 and 14 and the capacitor X_1 , if charged will discharge to ground through the transistor 16 or 13.

It is to be noted that, in the circuit of Fig. 1, no current flows except that which is necessary to charge or to discharge the output capacitor X_1 . If the circuit has just received a proper input and the capacitor has been charged to the "1" state, it will either remain charged, if the next input is also proper, or it will be discharged through a transistor to ground if the next input is improper. The gate circuit may be programmed to provide a "1" output for any desired input applied to the input terminals A and B by connecting which ever output of each phase splitter is to be a "1", when the desired input is applied, to the gate of the steering transistor associated with that particular phase splitter; and by connecting the other output of each phase splitter, which is to be a "0" when the desired input is applied, to the gate of the ground return transistor associated with that particular phase splitter.

Fig. 3 illustrates a preferred, simplified embodiment of a gate having three inputs D, E and F for achieving the same type of gate function as the circuit of Fig. 1. Ground and $-V$ potential reference leads to the gate structure have been eliminated. Each ground return transistor terminal, which would otherwise be connected to the ground lead as shown in Fig. 1, is connected to the normal or complementary output lead of the associated phase splitter, whichever is to be at "1" when a proper desired input is received which will enable a "1" to be obtained at the output of the circuit. The output voltages from the phase splitters then substitute for the ground and the $-V$ potentials which were otherwise provided to the circuit of Fig. 1 through separate power supply leads. The input to the first stage of the gate circuit is provided by

an output $\bar{D}$ of a phase splitter 37, which output is to be a "1" when the predetermined inputs are supplied to the circuit to provide a "1" at an output capacitor X_2 . (No separate output D is utilised in this particular example so only an inverter function is required.) By analogy to the operation of the circuit of Fig. 1 as described above, only if the input D is "0", the input E is "0", and the input F is "1" will the input requirements be satisfied to provide a "1" at the output capacitor X_2 as shown in the truth table of Fig. 4. For any other combination of inputs a "0" will be obtained at the output capacitor.

For example, assume that the desired input signal wherein D is "0", E is "0" and F is "1" is applied to the circuit. The output $\bar{D}$

obtained from the phase splitter 37 will be a "1" the output $\bar{E}$ and $\bar{E}$ obtained from phase splitter 38 will be "0" and "1" respectively, and the outputs F and $\bar{F}$ obtained from phase splitter 39 will be "1" and "0" respectively.

The "1" obtained at the output $\bar{E}$ of the phase splitter 38 is applied to the gate of a steering transistor 41 rendering the transistor 41 conductive and allowing it to pass the "1" signal, being applied to a terminal 42 by the

output $\bar{D}$ of the phase splitter 37, to a terminal 44 of a second steering transistor 46. The "0" obtained from the output E of the phase splitter 38 and applied to the gate of a first ground return transistor 47 will not render the transistor 47 conductive.

The "1" obtained from the output F of the phase splitter 39 and applied to the gate of the transistor 46 will render the transistor 46 conductive and allow it to pass the "1" signal being applied to the terminal 44 to the output capacitor X_2 . This capacitor X_2 consists of the distributed capacitance between the transistors 46 and 48 and a transistor 50 of a succeeding circuit (shown in dashed lines) plus the insulated gate capacitance of the transistor 50. The "0" obtained from the out-

put $\bar{F}$ of the phase splitter 39 and applied to the gate of a second ground return transistor 48 will not render the transistor 48 conductive. It is seen that, by the coincidence of desired inputs, the transistors 41 and 46 have been enabled to steer the "1" signal provided

from the output $\bar{D}$ of the phase splitter 37 to the output capacitor X_2 .

To illustrate the manner in which the circuit of Fig. 3 provides a "0" at the output capacitor X_2 when an input other than "0", "0" and "1" is applied to the inputs D , E and F , respectively, assume that the input signal applied is "0", "1" and "1". Since the input D is "0", a "1" is obtained from the output

$\bar{D}$ of the phase splitter 37 and applied to the terminal 42 of the transistor 41. With a "1" at the input E a "0" is obtained at the

output $\bar{E}$ of the phase splitter 38 and applied to the gate of the transistor 41 and to a terminal 49 of the transistor 47. The transistor 41 is not rendered conductive, however, since its characteristics are such that a "0" applied to its gate will fail to render it conductive.

Thus, the "1" signal from the output $\bar{D}$ cannot be passed by the steering transistor 41 to the capacitor X_2 . The "1" obtained from the output E of the phase splitter 38 is applied to the gate of the transistor 47, thereby render-

ing it conductive and allowing it to pass the "0" ($\bar{E}$) from the terminal 49 to the terminal 44 of the steering transistor 46. It is to be noted that the "0" which is being applied to the terminal 44 of the transistor 46 has been

obtained from the output $\bar{E}$ of the phase splitter 38 has been passed through the transistor 47 which was rendered conductive as a result of the "1" input to the phase splitter 38. The "1" obtained from the output F of the phase splitter 39 is applied to the gate of the transistor 46, rendering the transistor 46 conductive and allowing it to pass the "0" being applied to the terminal 44 to the output capacitor X_2 . If the output capacitor X_2 was previously charged to the "1" state as a result of the proper coincidence of inputs to the circuit, it will now be discharged through

transistors 46 and 47 to the "0" output $\bar{E}$ of the phase splitter 38. If, however, the capacitor X_2 was previously charged to the "0" state it will remain in the "0" state and no current will flow when the transistors 46 and 47 are rendered conductive.

Similarly, it should be obvious that all other non-programmed combinations of inputs D , E , F will not charge the capacitor X_2 to a "1" state and will discharge that capacitor, if

charged, to a "0" input (F , $\bar{E}$ or $\bar{D}$). For example, if the input F is "0" instead of "1", the second steering transistor 46 will not turn ON to pass a "1" signal, if present on the lead 44, to the capacitor X_2 , and the capacitor if charged will be discharged through the transistor 48 to the output F , which is "0" in this case. If the input D is "1", and

therefore, the output $\bar{D}$ is "0", then only a "0" can be applied to the capacitor X_2 through the steering transistors 41 and 46, if both are ON (corresponding to an input signal "1", "0" and "1").

It is also noted that, in the circuit of Fig. 3, no current flows except that which is necessary to charge and to discharge the output capacitor X_2 , thereby minimising the power dissipated on the silicon chip containing the circuit. A further point to be noted is that the output load device, which was described as a capacitor for the two particular embodiments of the invention disclosed, need not be a capacitor, but may be any impedance which is to be driven by the gate structure.

Although two particular embodiments of the invention have been described in detail, it is to be understood that various modifications may be made to fit particular conditions. For example, although this circuit has been described through the use of two common building blocks such as circuits 10 and 11 of Fig. 1, thereby providing for two possible

inputs to that circuit, and for three possible inputs to the circuit of Fig. 3, as many building blocks may be connected in series as are necessary to provide any desired number of inputs. The building blocks may be serially connected by merely connecting the output controlled terminal of the steering transistor of the preceding building block to the input controlled terminal of the steering transistor of the succeeding building block. Also, although specific reference has been made to MOS integrated transistor circuitry, it should be understood that the principles involved are equally applicable to circuits using discrete conventional components.

WHAT WE CLAIM IS:—

1. A logic gate comprising means responsive to each of at least two input bit signals for providing that bit signal and its inverse on distinct leads, at least two switching circuits, each having first and second input terminals and an output terminal respectively, the output terminal of each switching circuit except the last being connected to the first input terminal of the next succeeding switching circuit, and each connected to be controlled by signals on a pair of the distinct leads corresponding to a different said input bit signal to interconnect its output terminal and its first or its second input terminal depending on the value of the corresponding said bit signal, whereby, in operation, the output terminal of the last switching circuit is, in response to only one predetermined combination of said bit signals, energised to correspond with a predetermined energisation of the first input terminal of the first switching circuit to produce a unique output signal.

2. A logic gate according to claim 1, wherein the first input terminal of the first switching circuit is connected to a first constant voltage source, and the second input terminal of each switching circuit is connected to a second different constant voltage source.

3. A logic circuit according to claim 2, wherein the second voltage source is ground.

4. A logic gate according to claim 1, 2 or 3 wherein the output of the last switching circuit is energised to correspond with the ener-

gisation of the second input of a said switching circuit, in response to another combination of the binary signals.

5. A logic gate according to claim 1, wherein the first input terminal of the first switching circuit is connected to receive a signal based on a further input bit signal and the second input terminal of each switching circuit is connected to that one of the associated pair of leads that is to be energised similarly to the output terminal of the last switching circuit for said only one predetermined combination of input bit signals and said predetermined energisation of the first input terminal of the first switching circuit.

6. A logic gate according to any preceding claim, comprising an output load impedance connected to the output terminal of the last switching circuit.

7. A logic gate according to claim 6, wherein the output load impedance is capacitive.

8. A logic gate according to any preceding claim, wherein each switching circuit comprises a pair of field effect transistors each having its gate electrode connected to a different one of the associated said pair of leads, and one controlled electrode connected to the output terminal, the first input terminal being the other controlled electrode of a first of the transistors that serves to steer any energisation of the first input terminal towards the output terminal, and the second input terminal being the other controlled electrode of the other transistor that serves to control any energisation at the output terminal.

9. A logic gate according to claim 8 with claim 7, comprising MOSFET integrated circuitry of which the load impedance comprises distributed capacitance.

10. A logic gate arranged and adapted to operate substantially as herein described with reference to and as shown in Figs. 1 and 2, or Figs. 3 and 4 of the drawing.

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inputs to that circuit, and for three possible inputs to the circuit of Fig. 3, as many building blocks may be connected in series as are necessary to provide any desired number of inputs. The building blocks may be serially connected by merely connecting the output controlled terminal of the steering transistor of the preceding building block to the input controlled terminal of the steering transistor of the succeeding building block. Also, although specific reference has been made to MOS integrated transistor circuitry, it should be understood that the principles involved are equally applicable to circuits using discrete conventional components.

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gisation of the second input of a said switching circuit, in response to another combination of the binary signals.

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6. A logic gate according to any preceding claim, comprising an output load impedance connected to the output terminal of the last switching circuit.

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8. A logic gate according to any preceding claim, wherein each switching circuit comprises a pair of field effect transistors each having its gate electrode connected to a different one of the associated said pair of leads, and one controlled electrode connected to the output terminal, the first input terminal being the other controlled electrode of a first of the transistors that serves to steer any energisation of the first input terminal towards the output terminal, and the second input terminal being the other controlled electrode of the other transistor that serves to control any energisation at the output terminal.

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