FIG. 1

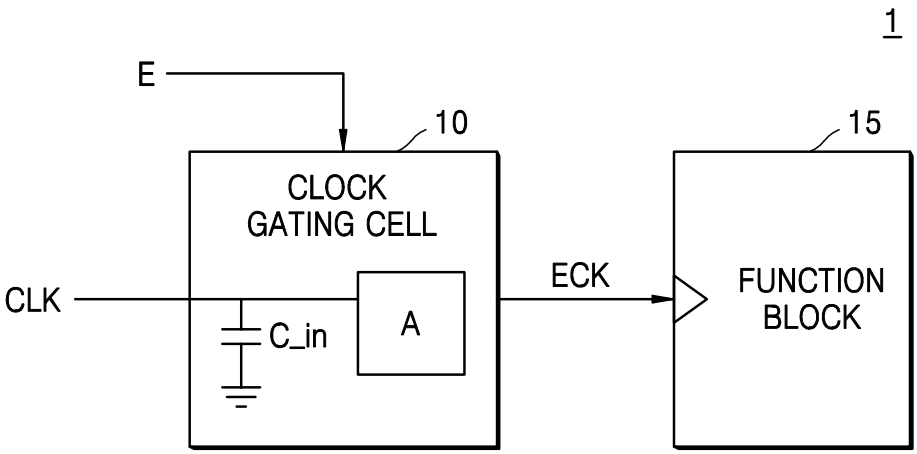


FIG. 2

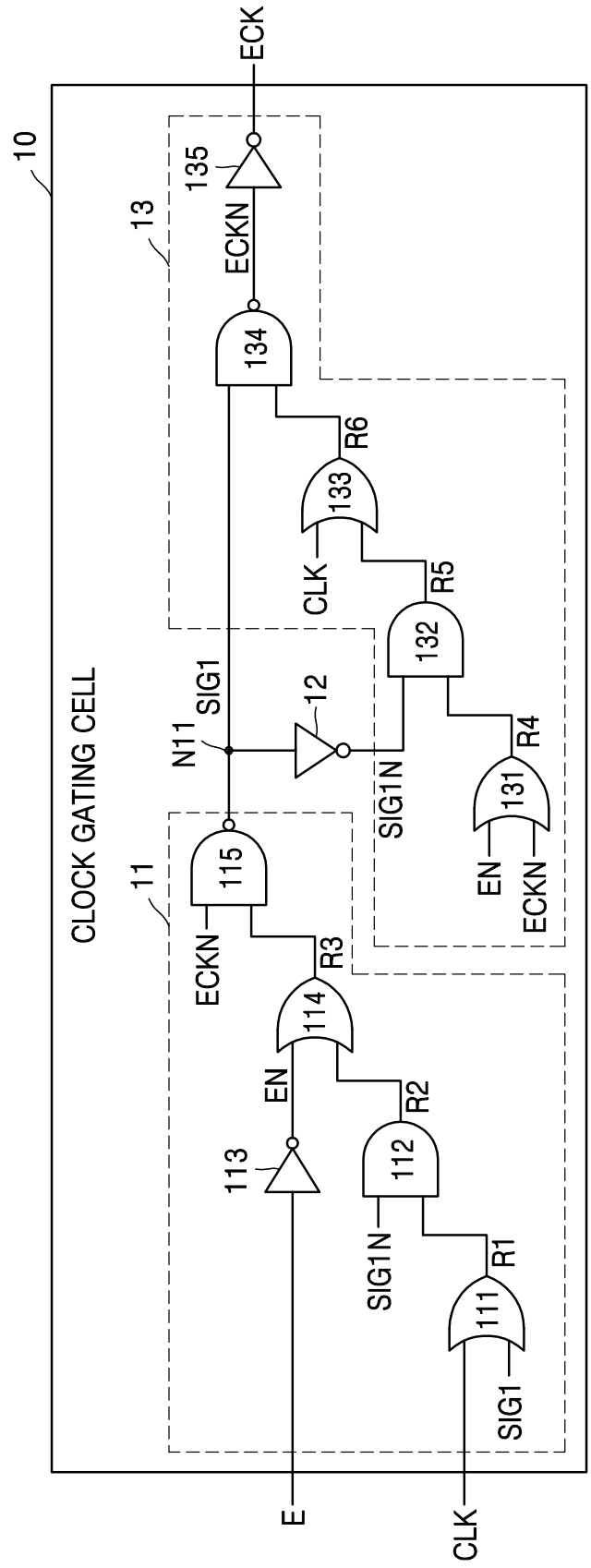

10
CLOCK GATING CELL
11
13
ECK
135
ECKN
134
R6
133
CLK
R5
132
SIG1
N11
12
SIG1N
R4
131
EN
ECKN
115
ECKN
R3
114
EN
R2
113
112
SIG1N
R1
111
SIG1
E
CLK

FIG. 3A

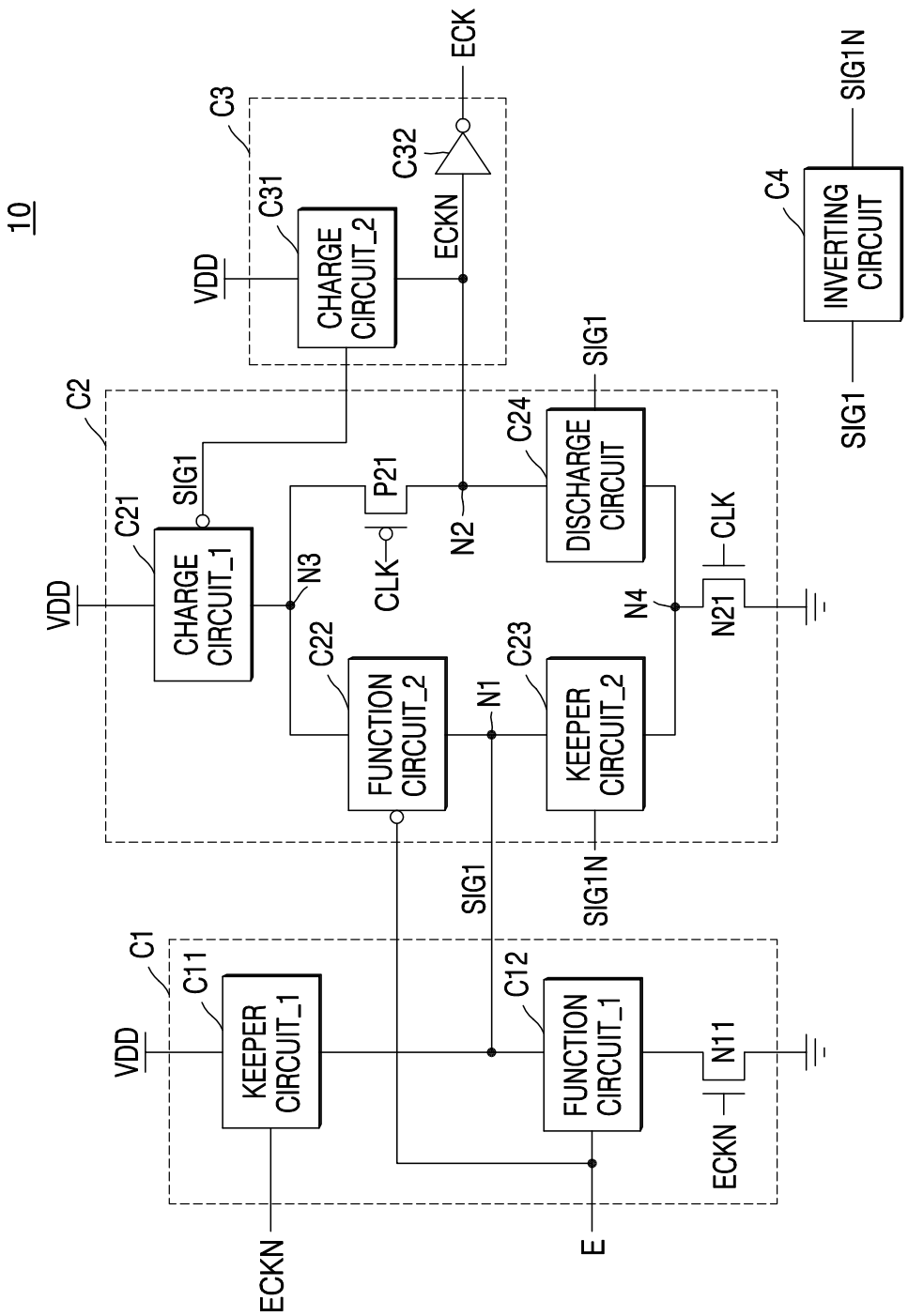

10
C1
C11
KEEPER CIRCUIT_1
VDD
ECKN
C12
FUNCTION CIRCUIT_1
E
N11
ECKN
C2
C21
CHARGE CIRCUIT_1
VDD
SIG1
N3
C22
FUNCTION CIRCUIT_2
P21
CLK
N2
C23
KEEPER CIRCUIT_2
N1
SIG1
SIG1N
C24
DISCHARGE CIRCUIT
SIG1
N4
CLK
N21
C3
C31
CHARGE CIRCUIT_2
VDD
ECKN
C32
ECK
C4
INVERTING CIRCUIT
SIG1
SIG1N

FIG. 3B

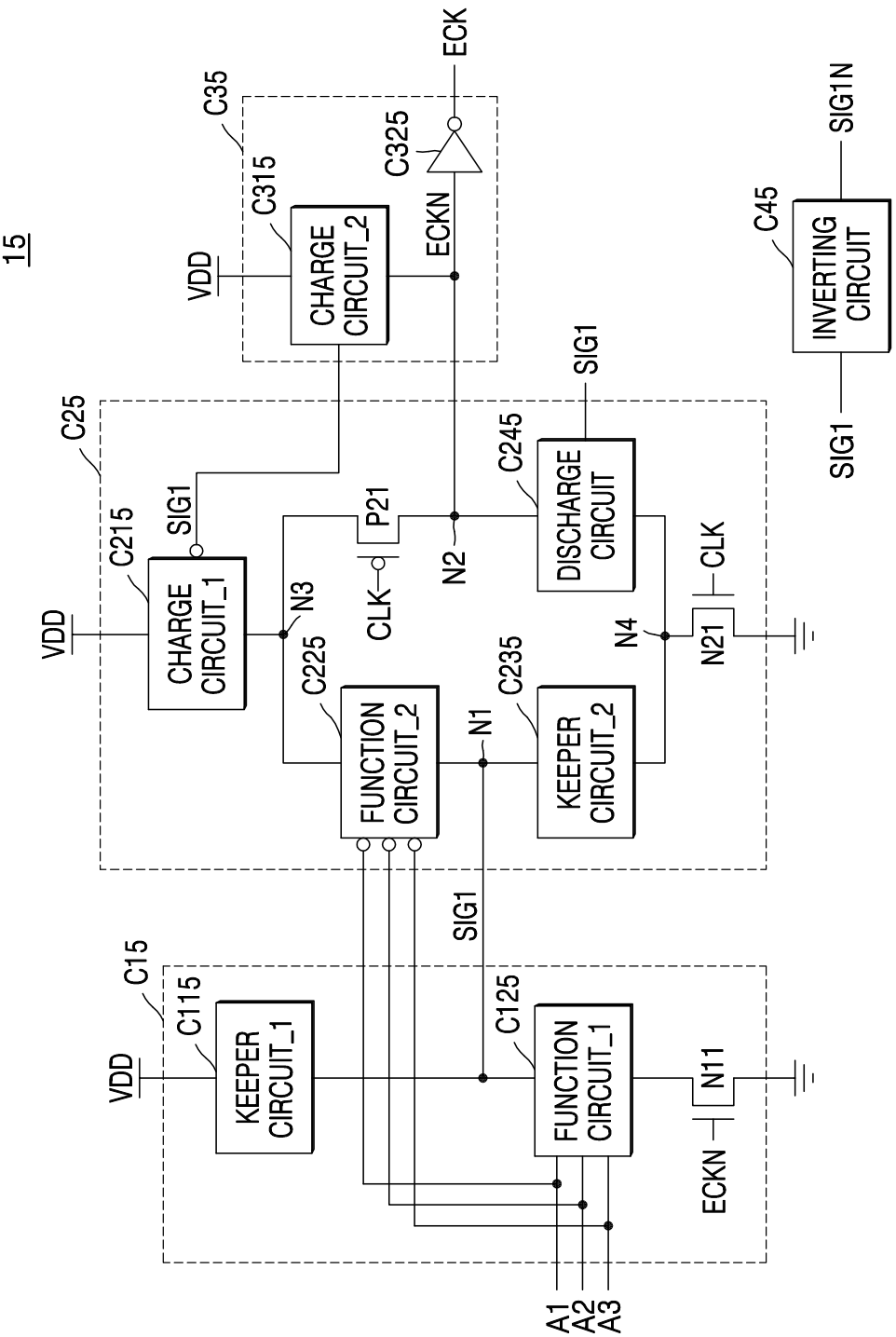

15
C35
C315
CHARGE CIRCUIT_2
VDD
ECK
C325
ECKN
C45
INVERTING CIRCUIT
SIG1N
SIG1
C25
C215
CHARGE CIRCUIT_1
SIG1
P21
CLK
N2
C245
DISCHARGE CIRCUIT
SIG1
VDD
N3
C225
FUNCTION CIRCUIT_2
N1
C235
KEEPER CIRCUIT_2
N4
CLK
N21
C15
C115
KEEPER CIRCUIT_1
VDD
C125
FUNCTION CIRCUIT_1
N11
ECKN
SIG1
A1
A2
A3

FIG. 4

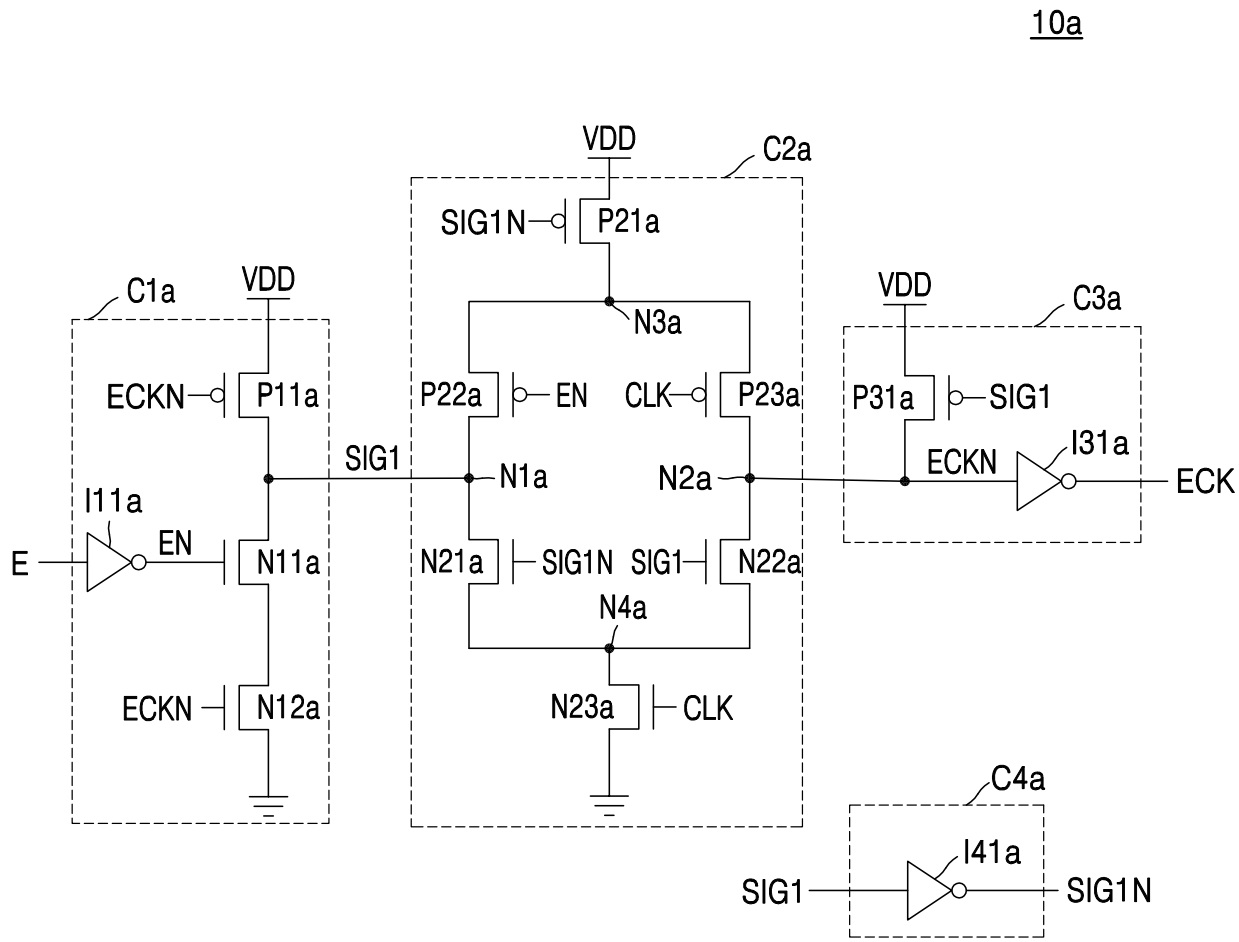

10a
VDD
C2a
SIG1N
P21a
N3a
C1a
VDD
ECKN
P11a
P22a
EN
CLK
P23a
VDD
C3a
P31a
SIG1
SIG1
N1a
N2a
ECKN
I31a
ECK
I11a
E
EN
N11a
N21a
SIG1N
SIG1
N22a
N4a
ECKN
N12a
N23a
CLK
C4a
I41a
SIG1
SIG1N

FIG. 5

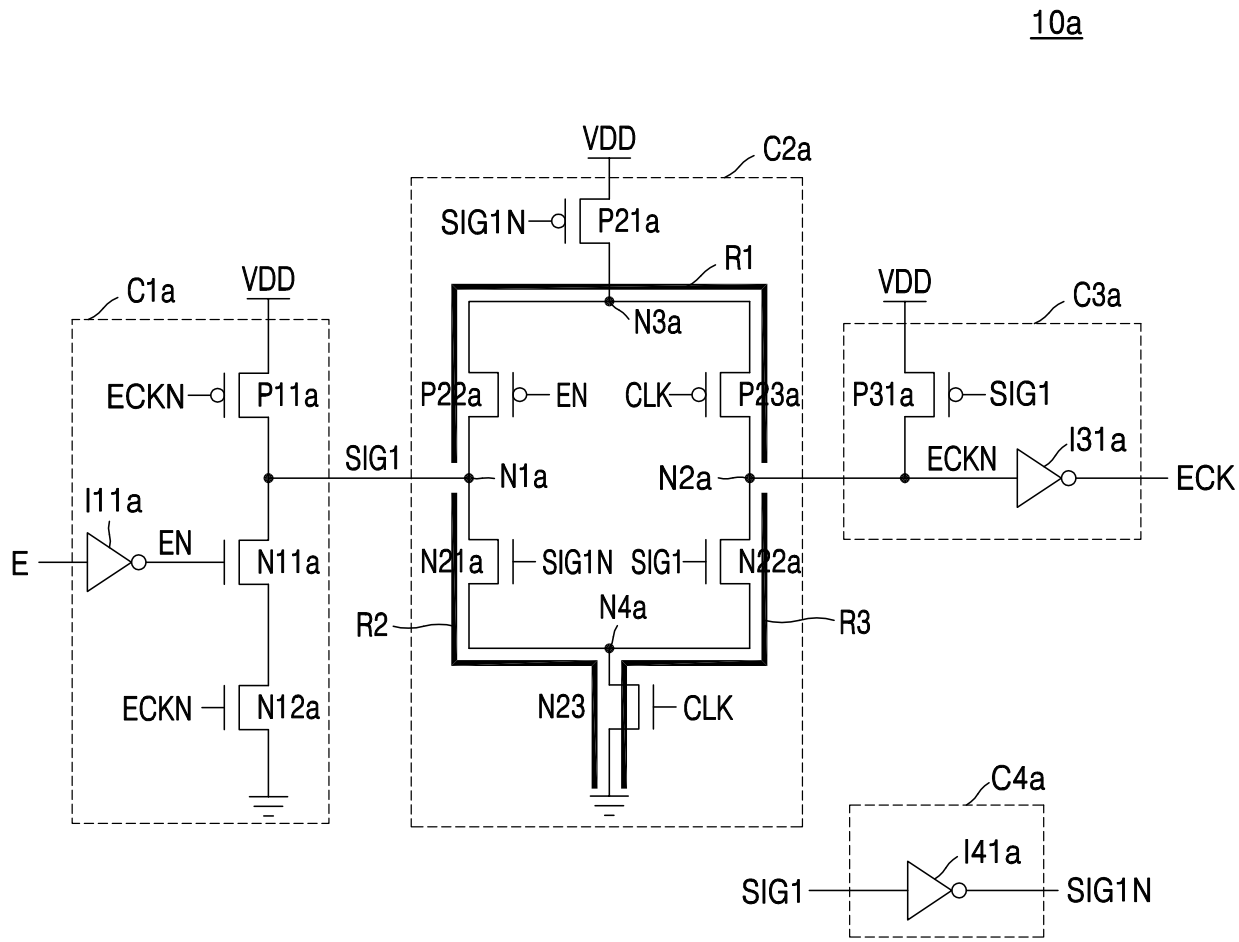

10a
VDD
C2a
SIG1N
P21a
R1
N3a
C1a
VDD
ECKN
P11a
P22a
EN
CLK
P23a
VDD
C3a
P31a
SIG1
SIG1
N1a
N2a
ECKN
I31a
ECK
I11a
E
EN
N11a
N21a
SIG1N
SIG1
N22a
N4a
R2
R3
ECKN
N12a
N23
CLK
C4a
I41a
SIG1
SIG1N

FIG. 6

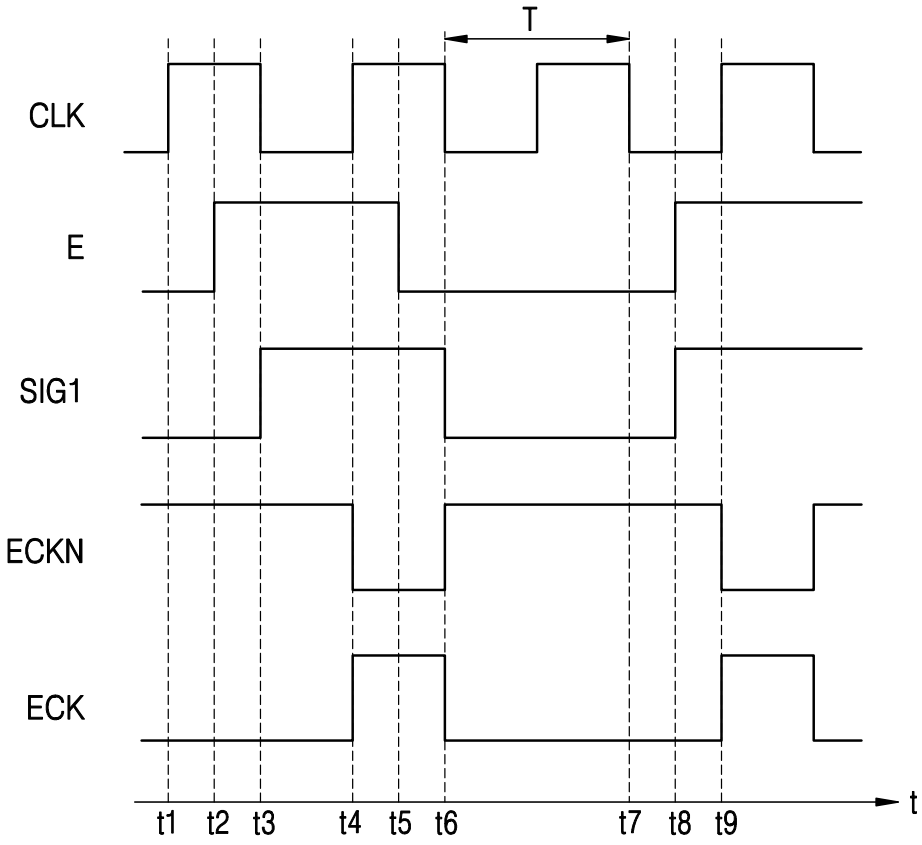


FIG. 7

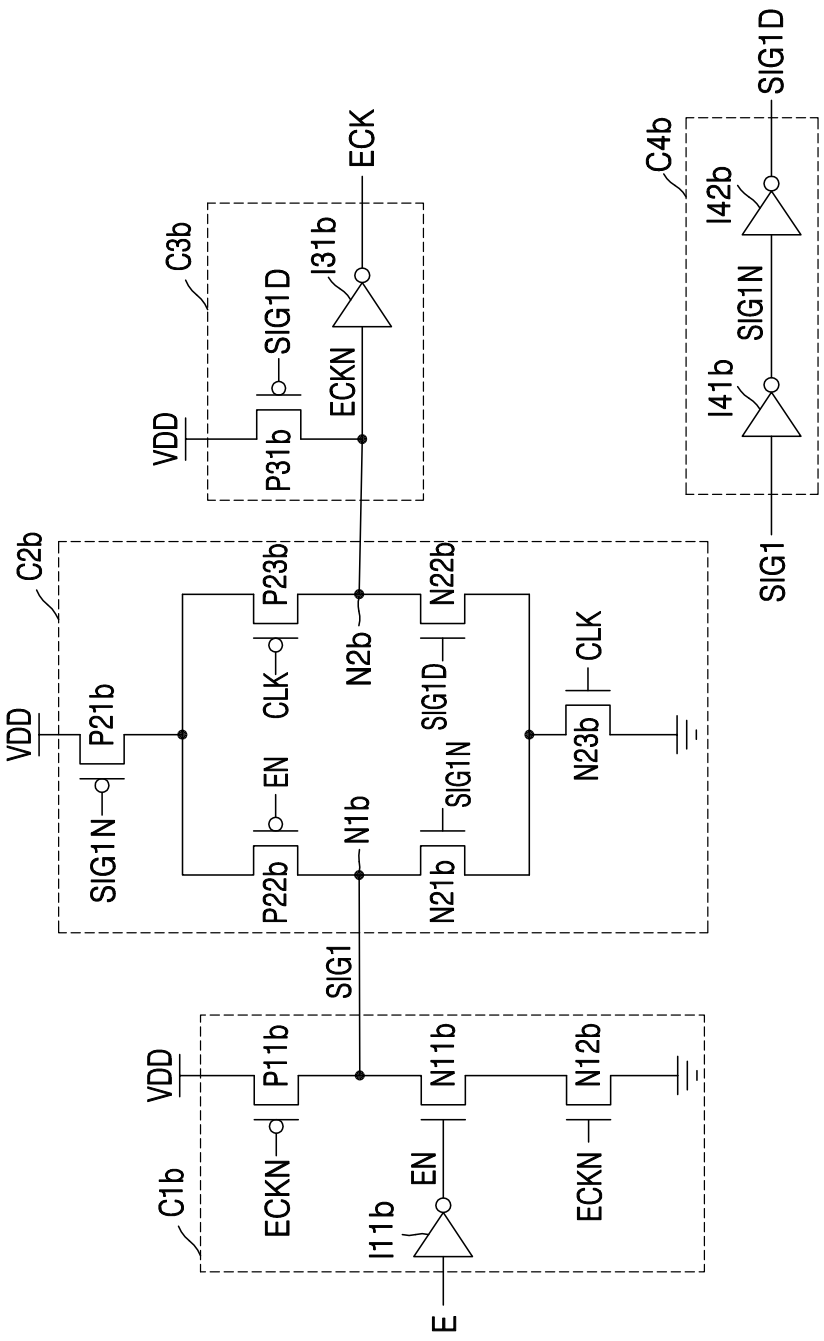

10b
C1b
C2b
C3b
C4b
VDD
ECKN
P11b
N11b
N12b
I11b
EN
E
SIG1
P21b
SIG1N
P22b
N1b
N21b
P23b
CLK
N2b
N22b
SIG1D
N23b
P31b
ECK
I31b
I41b
I42b
SIG1

FIG. 8

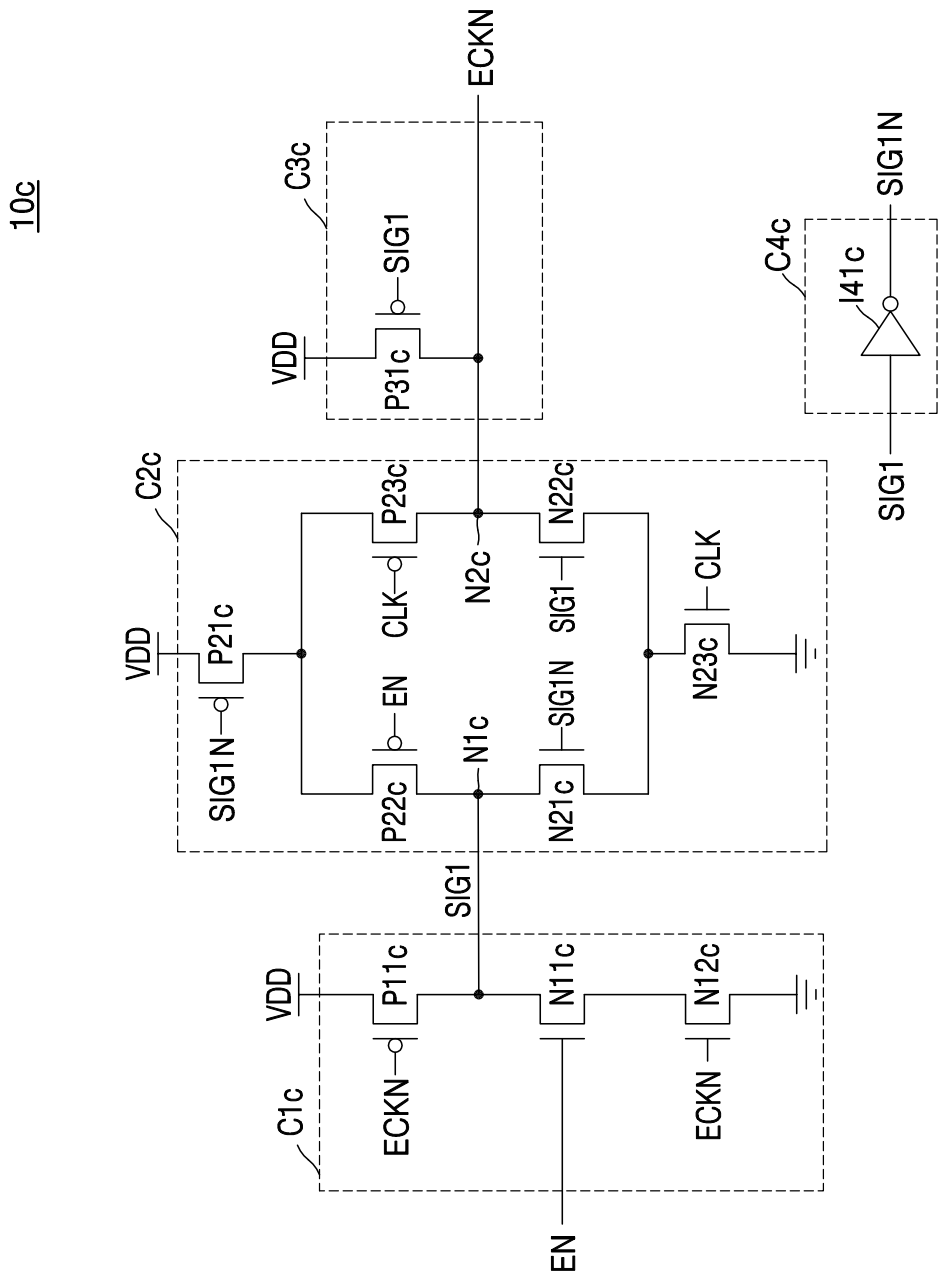

10c
C1c
C2c
C3c
C4c
VDD
ECKN
P11c
N11c
N12c
SIG1
P21c
P22c
P23c
N21c
N22c
N23c
N1c
N2c
EN
CLK
SIG1N
P31c
I41c

FIG. 9

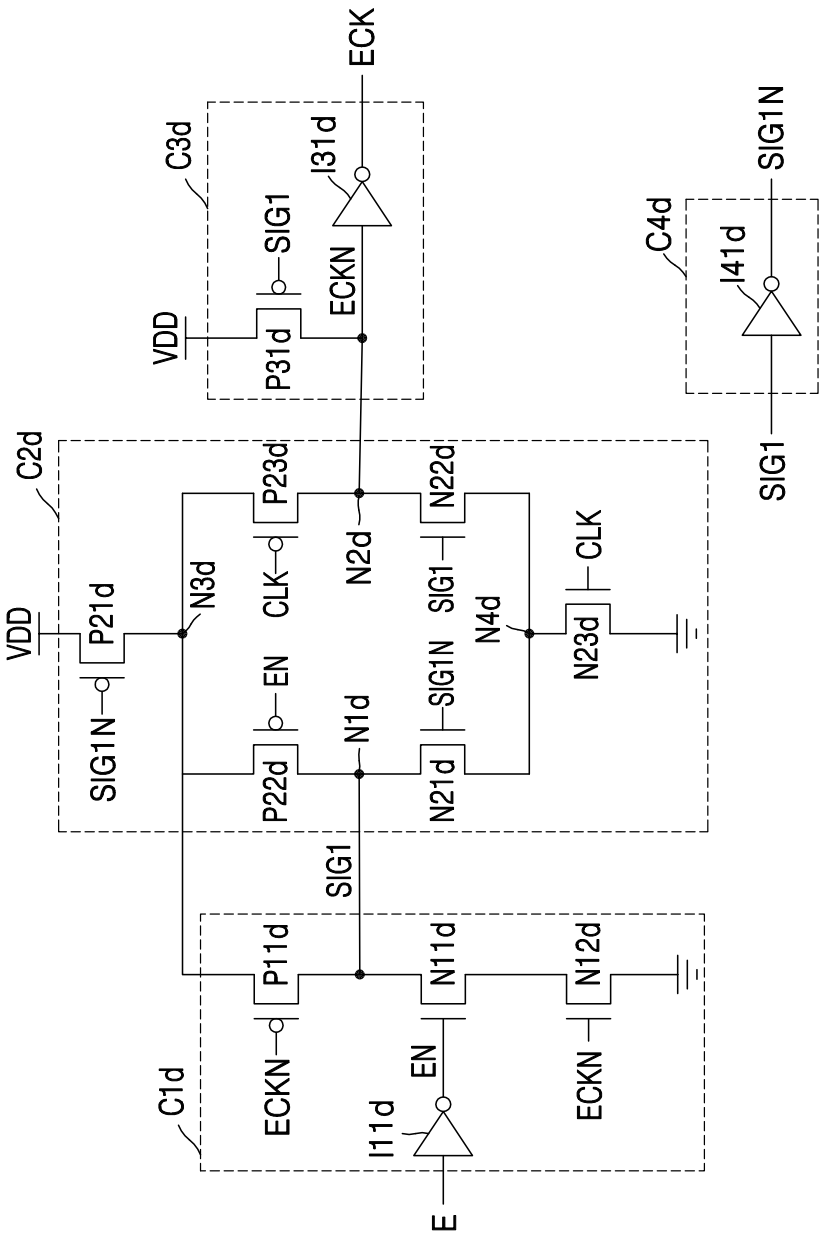

10d
C1d
C2d
C3d
C4d
E
ECKN
EN
I11d
P11d
N11d
N12d
SIG1
P22d
N1d
N21d
SIG1N
P21d
N3d
VDD
P23d
CLK
N2d
N22d
SIG1
N4d
N23d
CLK
P31d
SIG1
ECKN
I31d
ECK
I41d
SIG1N
SIG1

FIG. 10

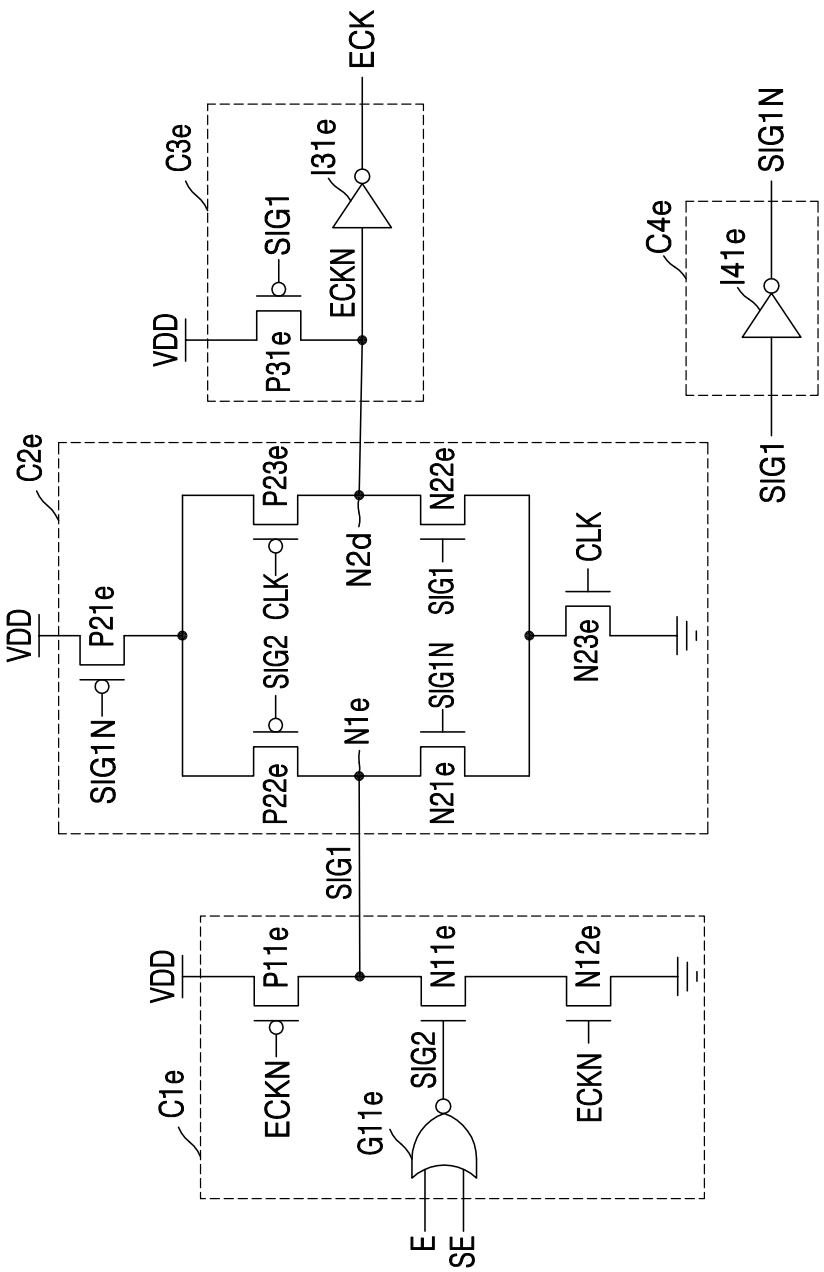

10e
C1e
C2e
C3e
C4e
VDD
ECKN
P11e
N11e
N12e
G11e
SIG2
E
SE
SIG1
P21e
SIG1N
P22e
SIG2
CLK
P23e
N1e
N21e
SIG1N
SIG1
N22e
N2d
N23e
CLK
P31e
SIG1
ECKN
I31e
ECK
I41e
SIG1N
SIG1

FIG. 11A

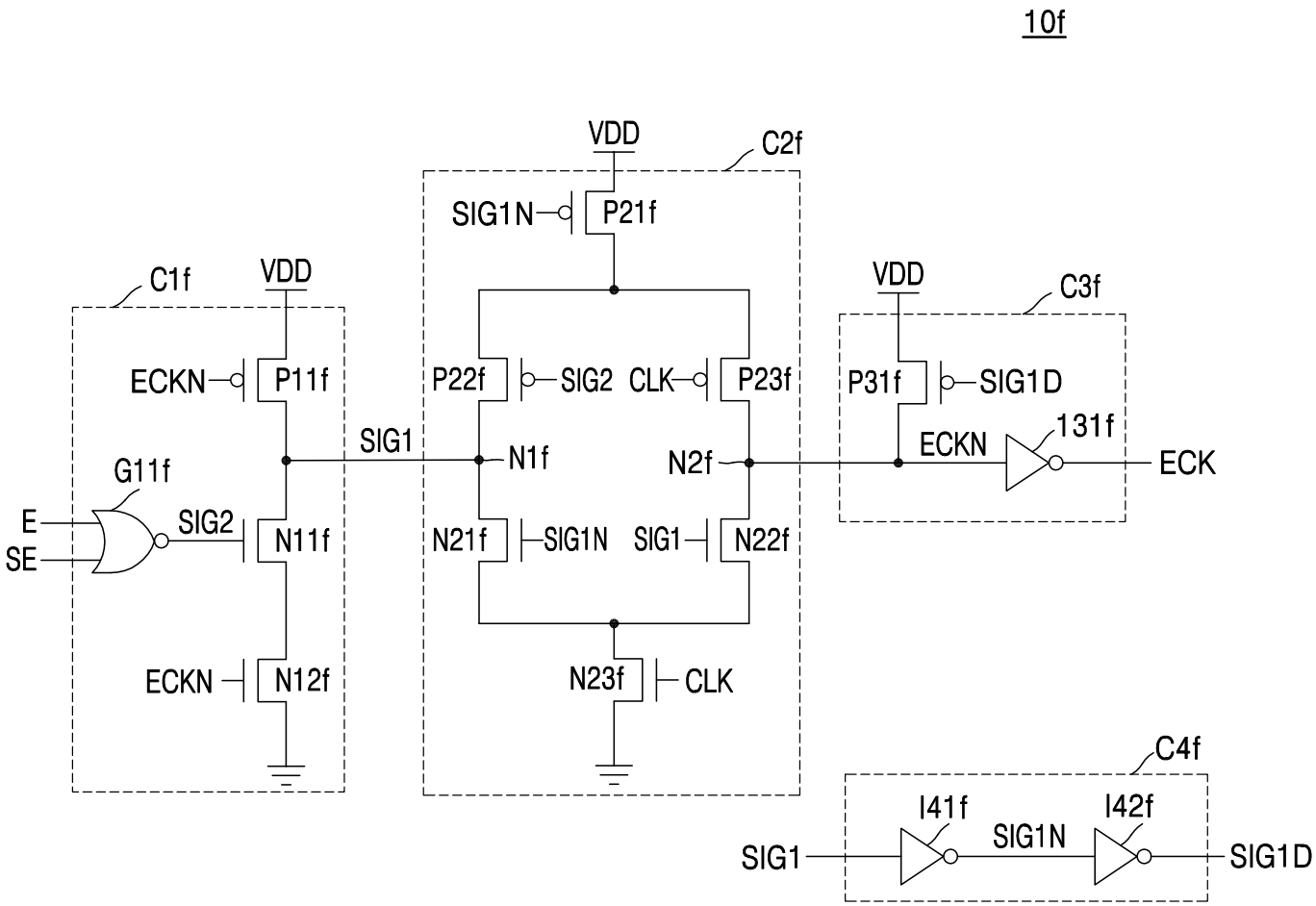

10f
VDD
C2f
SIG1N
P21f
C1f
VDD
ECKN
P11f
P22f
SIG2
CLK
P23f
VDD
C3f
P31f
SIG1D
SIG1
N1f
N2f
ECKN
131f
ECK
G11f
E
SE
SIG2
N11f
N21f
SIG1N
SIG1
N22f
ECKN
N12f
N23f
CLK
C4f
I41f
I42f
SIG1N
SIG1
SIG1D

FIG. 11B

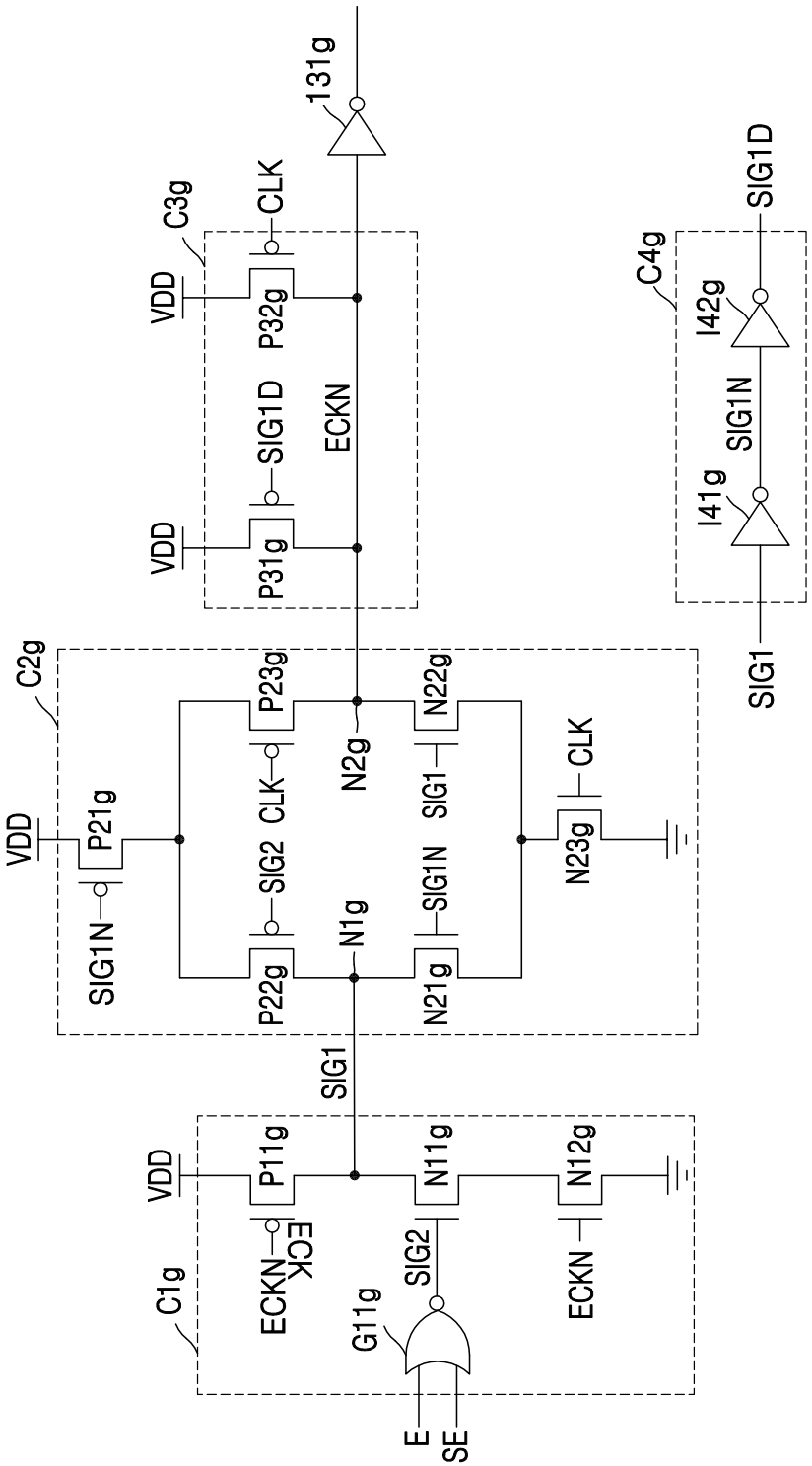

10g
C1g
C2g
C3g
C4g
VDD
P11g
N11g
N12g
ECKN
ECK
G11g
SIG2
E
SE
SIG1
P21g
SIG1N
P22g
P23g
N1g
N21g
N22g
N23g
CLK
N2g
P31g
P32g
SIG1D
131g
I41g
I42g
SIG1D

FIG. 12

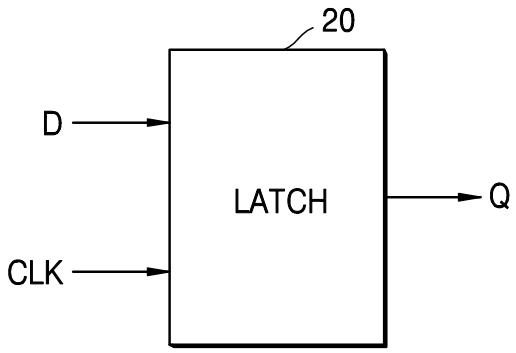


FIG. 13

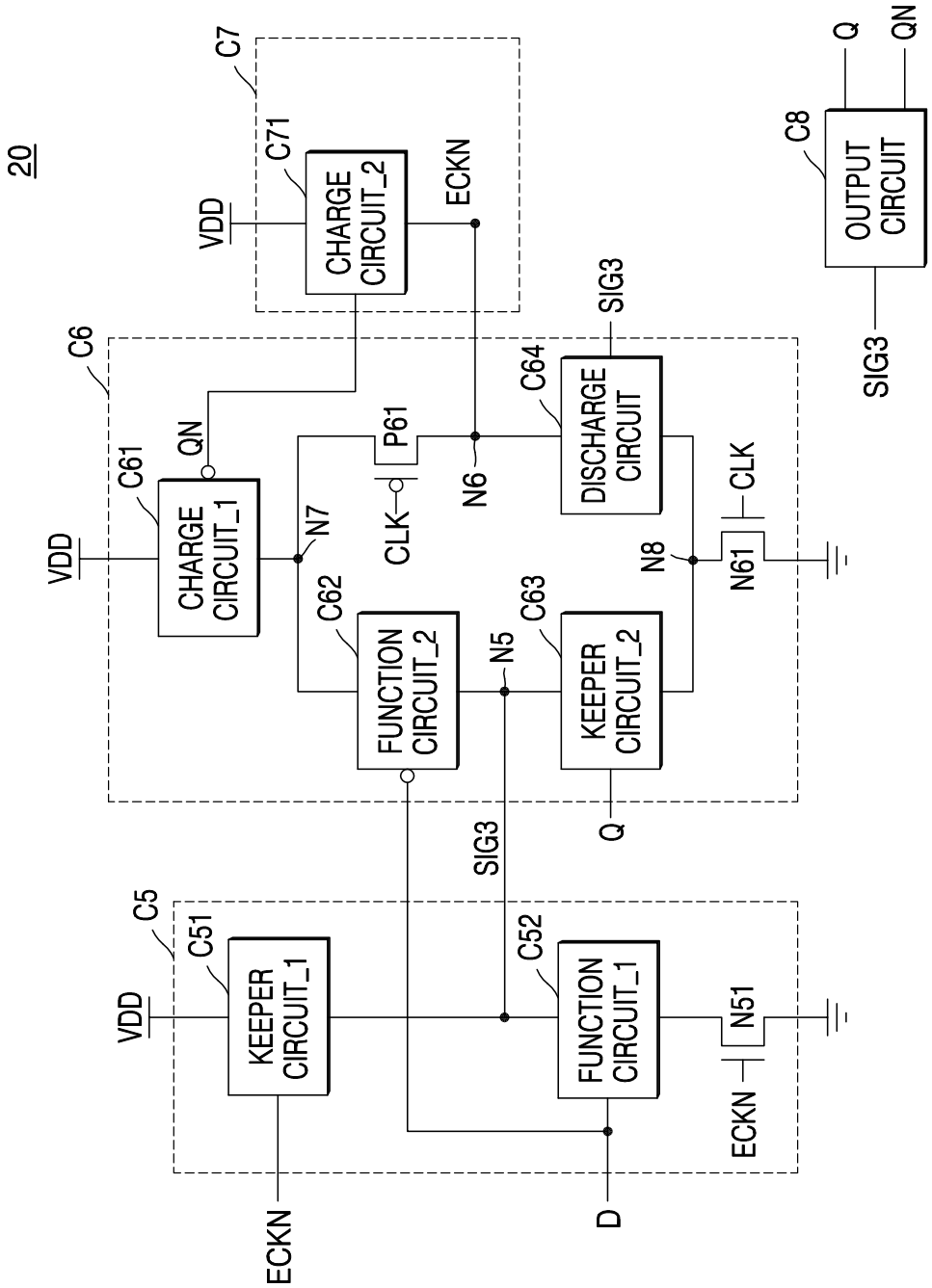

20
C7
C71
CHARGE CIRCUIT_2
VDD
ECKN
C8
OUTPUT CIRCUIT
Q
QN
SIG3
C6
C61
CHARGE CIRCUIT_1
QN
VDD
N7
CLK
P61
N6
C64
DISCHARGE CIRCUIT
SIG3
CLK
N8
N61
C62
FUNCTION CIRCUIT_2
N5
C63
KEEPER CIRCUIT_2
Q
SIG3
C5
C51
KEEPER CIRCUIT_1
VDD
C52
FUNCTION CIRCUIT_1
N51
ECKN
ECKN
D

FIG. 14

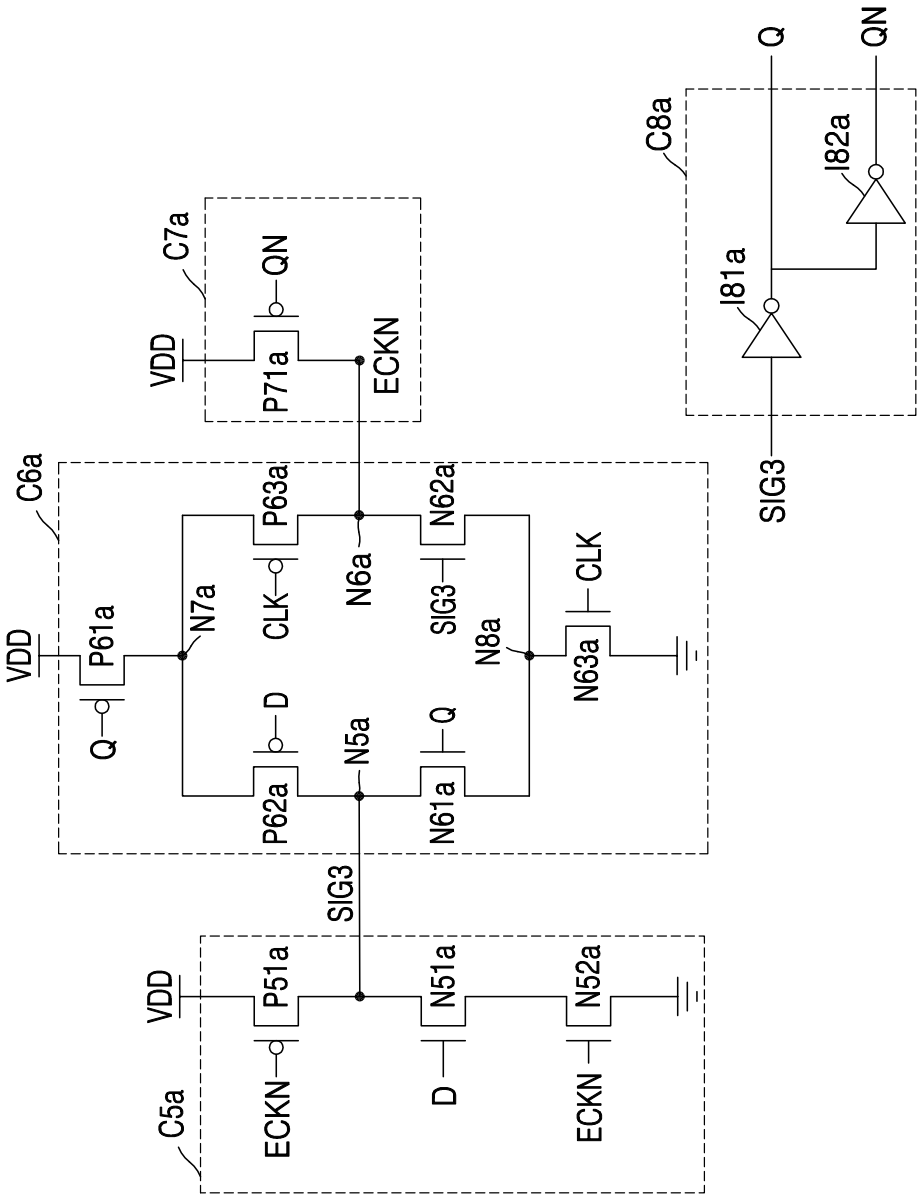

20a
C5a
C6a
C7a
C8a
VDD
ECKN
P51a
N51a
N52a
D
SIG3
P62a
N61a
N5a
Q
P61a
N7a
P63a
N62a
N6a
CLK
N8a
N63a
P71a
QN
I81a
I82a

FIG. 15

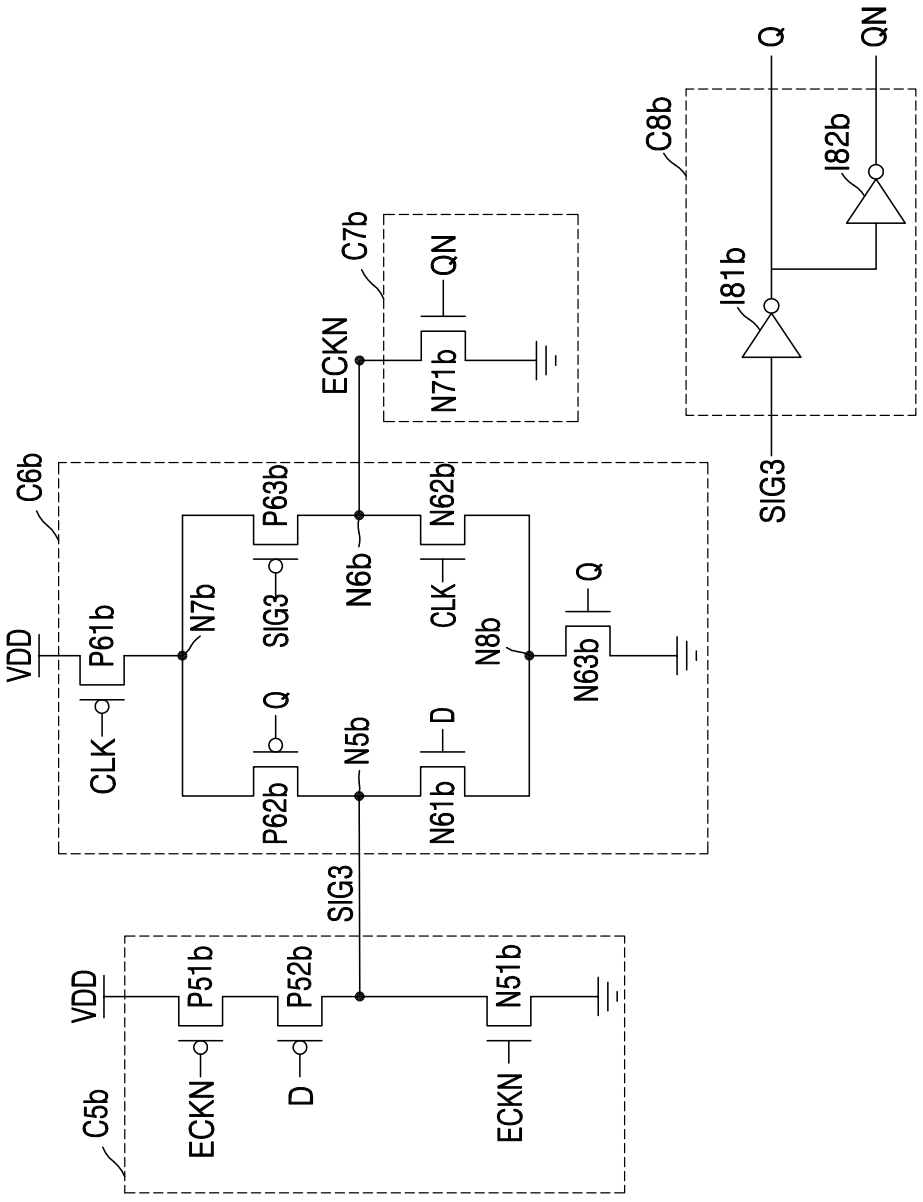

20b
C5b
VDD
P51b
P52b
N51b
ECKN
D
ECKN
SIG3
C6b
VDD
P61b
N7b
P63b
N62b
CLK
Q
SIG3
N6b
CLK
N8b
Q
N63b
P62b
N5b
D
N61b
C7b
ECKN
N71b
QN
C8b
I81b
I82b
Q
QN
SIG3

FIG. 16A

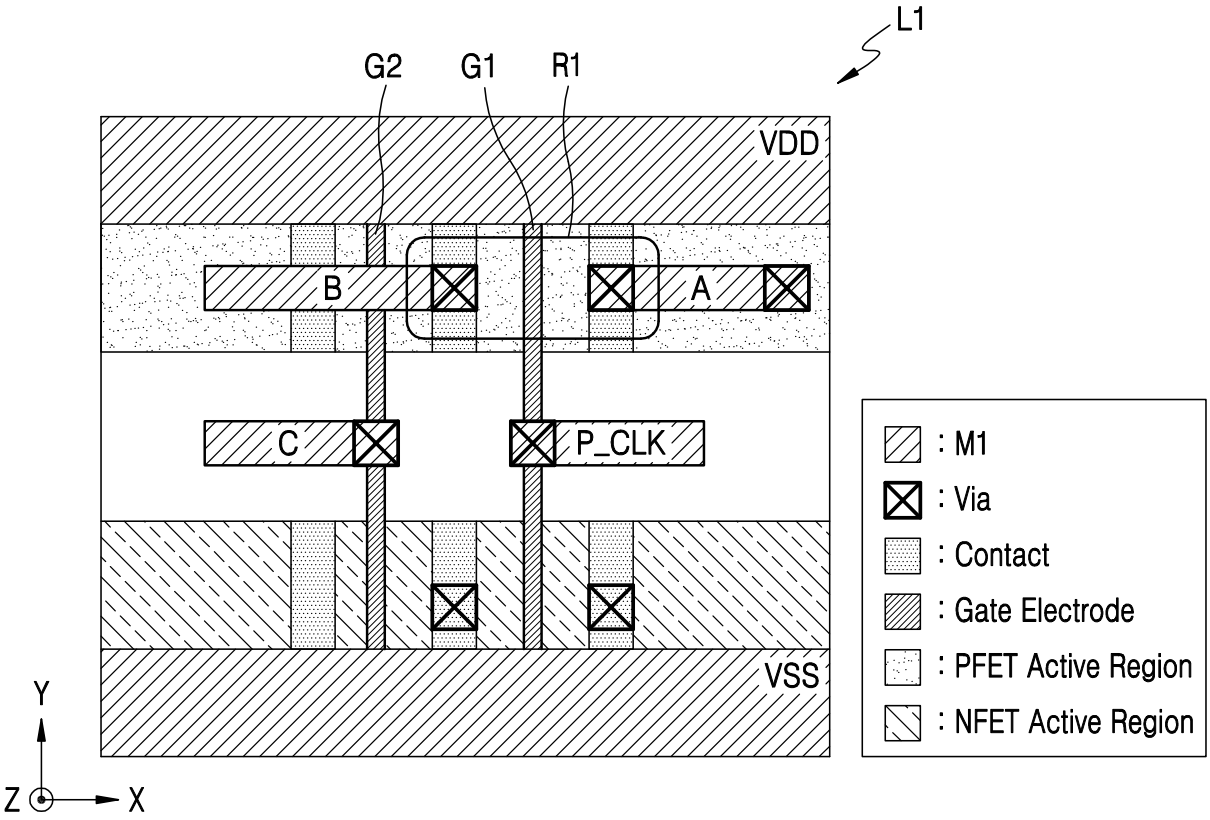

L1
G2
G1
R1
VDD
B
A
C
P_CLK
VSS
Y
Z
X
: M1
: Via
: Contact
: Gate Electrode
: PFET Active Region
: NFET Active Region

FIG. 16B

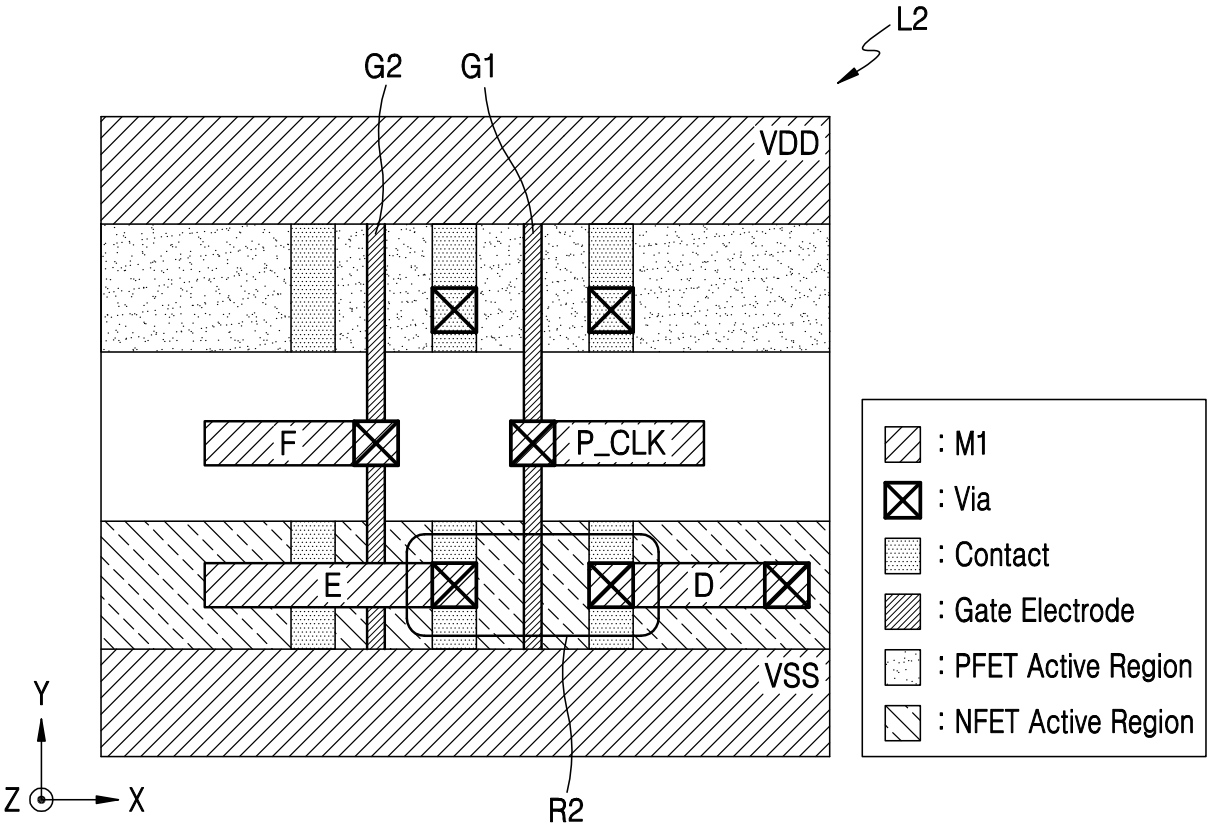

L2
G2
G1
VDD
F
P_CLK
E
D
VSS
R2
Y
Z
X
: M1
: Via
: Contact
: Gate Electrode
: PFET Active Region
: NFET Active Region

FIG. 17

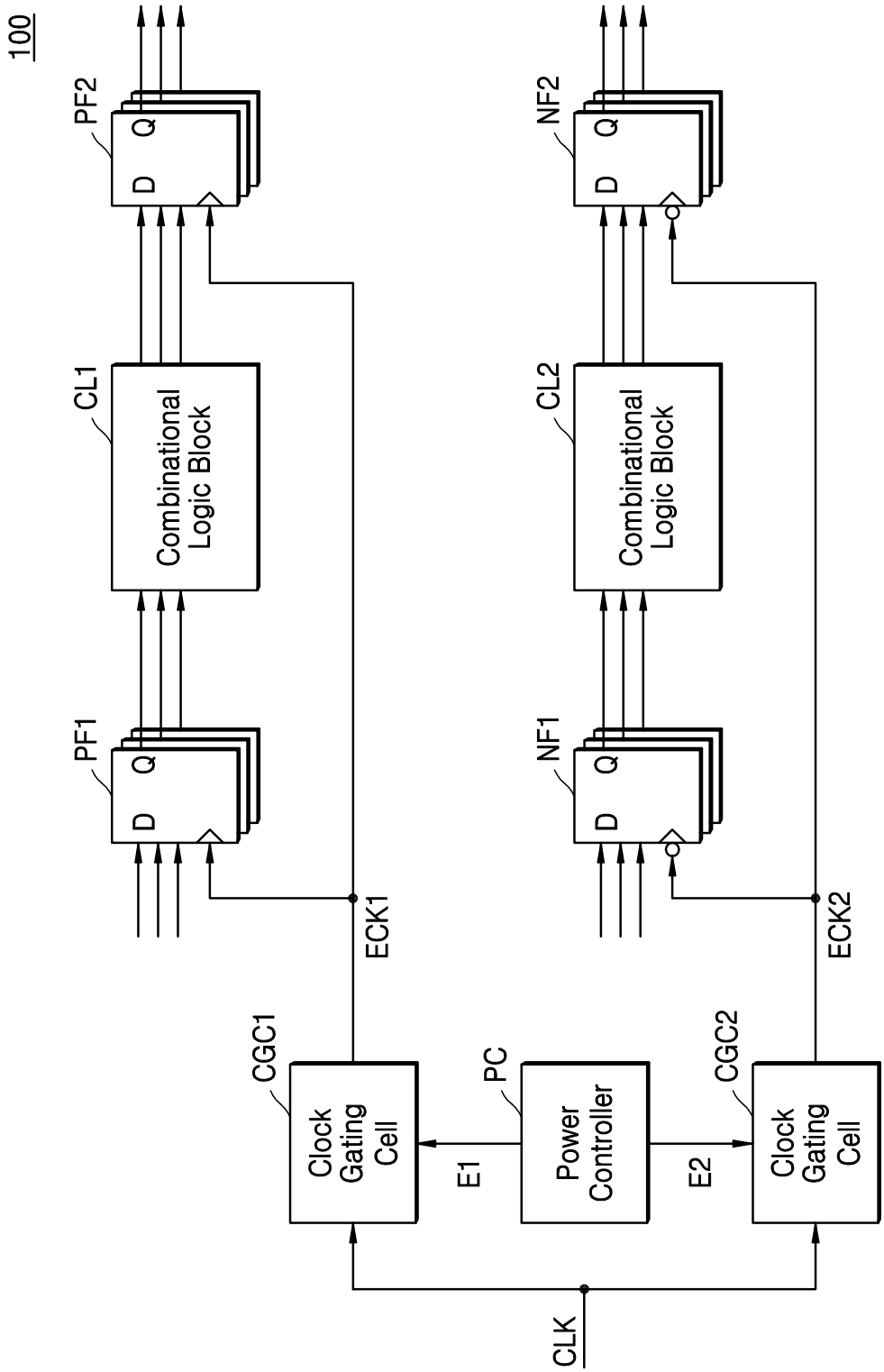
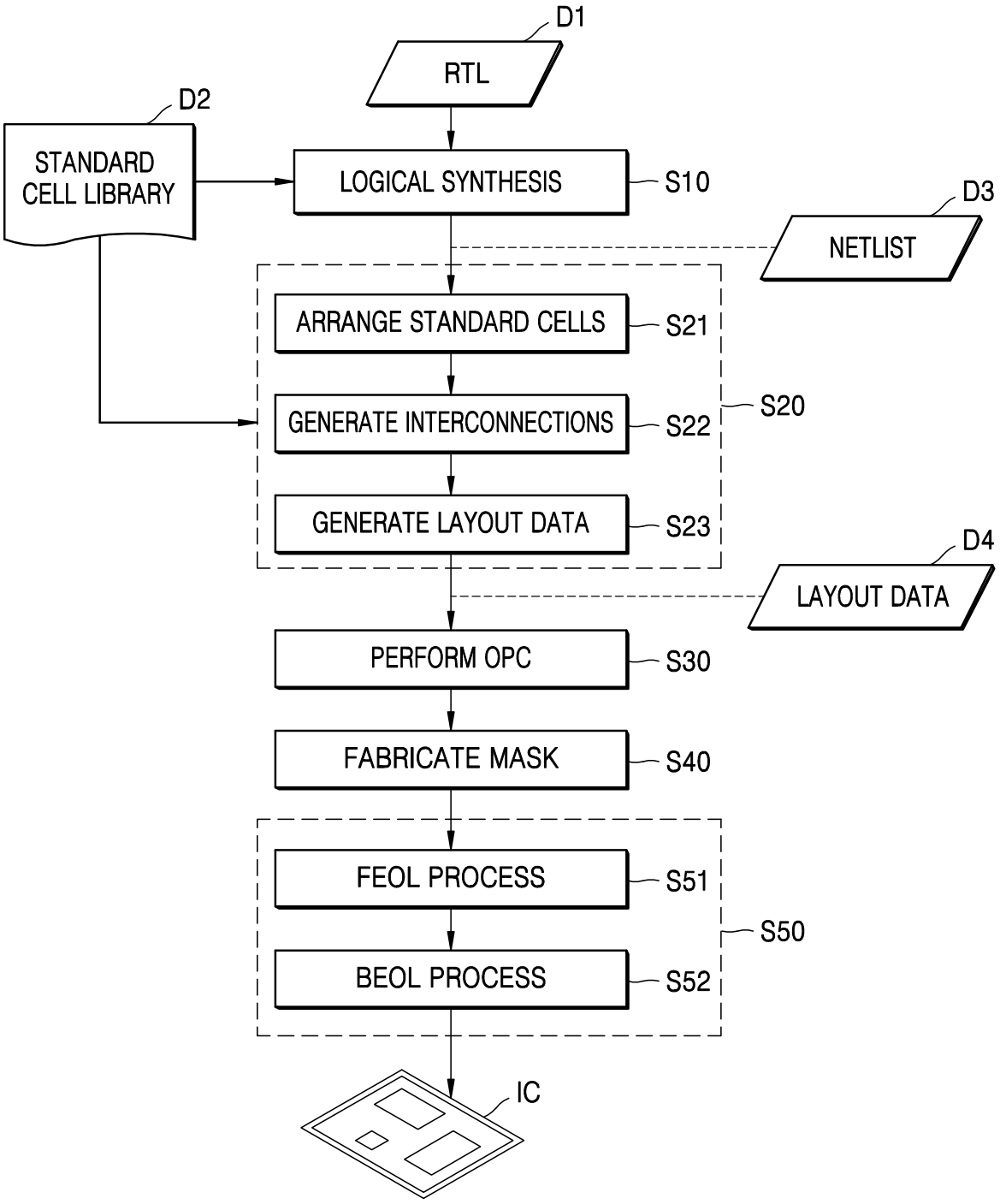

100
PF2
D
Q
CL1
Combinational Logic Block
PF1
D
Q
ECK1
CGC1
Clock Gating Cell
PC
Power Controller
E1
E2
CGC2
Clock Gating Cell
NF2
D
Q
CL2
Combinational Logic Block
NF1
D
Q
ECK2
CLK

FIG. 18


D1
RTL
D2
STANDARD CELL LIBRARY
LOGICAL SYNTHESIS
S10
D3
NETLIST
ARRANGE STANDARD CELLS
S21
GENERATE INTERCONNECTIONS
S22
S20
GENERATE LAYOUT DATA
S23
D4
LAYOUT DATA
PERFORM OPC
S30
FABRICATE MASK
S40
FEOL PROCESS
S51
S50
BEOL PROCESS
S52
IC