

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property
Organization
International Bureau

(43) International Publication Date
08 May 2025 (08.05.2025)



(10) International Publication Number
WO 2025/096170 A1

(51) International Patent Classification:

H01L 21/768 (2006.01) H01L 21/311 (2006.01)

(21) International Application Number:

PCT/US2024/050920

(22) International Filing Date:

11 October 2024 (11.10.2024)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

18/497,096 30 October 2023 (30.10.2023) US

(71) Applicant: **APPLIED MATERIALS, INC.** [US/US];
3050 Bowers Avenue, Santa Clara, California 95054 (US).

(72) Inventors: **DAG, Sefa**; 3050 Bowers Avenue, Santa Clara,
California 95054 (US). **BAZIZI, El Mehdi**; 3050 Bowers
Avenue, Santa Clara, California 95054 (US). **BERKENS,
Martinus Maria**; 3050 Bowers Avenue, Santa Clara, Cali-

fornia 95054 (US). **SHERMAN, Steven**; 3050 Bowers Av-
enue, Santa Clara, California 95054 (US). **REDDY, Vinod**;
3050 Bowers Avenue, Santa Clara, California 95054 (US).

(74) Agent: **BERGSTROM, James T.** et al.; Kilpatrick
Townsend & Stockton LLP, Mailstop: IP Docketing - 22,
1100 Peachtree Street, Suite 2800, Atlanta, Georgia 30309
(US).

(81) Designated States (*unless otherwise indicated, for every
kind of national protection available*): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ,
CA, CH, CL, CN, CO, CR, CU, CV, CZ, DE, DJ, DK, DM,
DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT,
HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG,
KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY,
MA, MD, MG, MK, MN, MU, MW, MX, MY, MZ, NA,
NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO,
RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH,

(54) Title: VIA SHAPING BETWEEN METAL LAYERS FOR CONTROLLED RESISTANCE

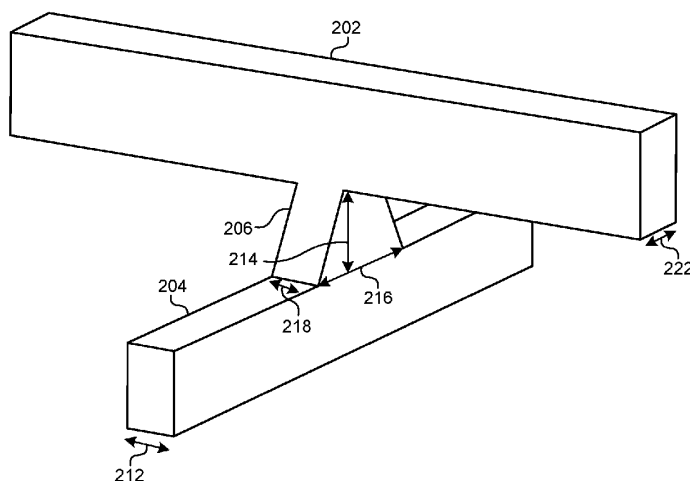


FIG. 2A

(57) Abstract: This disclosure describes structures and methods for forming tapered vias between features in metal layers in semiconductor devices. Instead of straight vias that have 90° vertical sidewalls and a constant cross-sectional area throughout the height of the via, tapered vias may be formed that extend outward from one metal layer to a lower metal layer. The via may be allowed to expand in size in a direction parallel to the feature in the lower metal layer, while remaining a constant width so as not to expand beyond the footprint of the lower feature. This tapered shape results in a larger cross-sectional area at the interface between the via and the lower feature. This lowers the resistance of the via by increasing area for current flow, while also increasing the area of any liners which typically have higher resistances.

[Continued on next page]

TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS,
ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, CV, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SC, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, ME, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))