CLAIMS

1. A vertical high-electron-mobility transistor, HEMT, comprising:

a substrate;

a drain contact, the drain contact being a metal contact via through said substrate;

a pillar layer arranged above the drain contact and comprising at least one vertical pillar and a supporting material laterally enclosing the at least one vertical pillar;

a heterostructure mesa arranged on the pillar layer, the heterostructure mesa comprising an AlGaN-layer and a GaN-layer, together forming a heterojunction;

at least one source contact electrically connected to the heterostructure mesa;

a gate contact arranged on said heterostructure mesa, and above the at least one vertical pillar; and

a current blocking layer arranged on a lateral side of a GaN vertical connection, the GaN vertical connection being an electrical connection between the at least one source contact and the heterostructure mesa of the vertical HEMT, wherein said current blocking layer comprises carbon-doped or iron doped GaN;

wherein the at least one vertical pillar is forming an electron transport channel between the drain contact and the heterojunction.

2. The vertical HEMT according to claim 1, wherein the AlGaN layer of the heterojunction is intrinsically doped, the vertical HEMT further comprising:

an intrinsically doped GaN layer arranged above the intrinsically doped AlGaN layer of the heterojunction, and aligned laterally over the at least one vertical pillar, wherein said GaN layer has a thickness of at least 14 nm and a combined thickness of said GaN layer and the AlGaN layer of the heterojunction is in the range 20-50 nm.

3. The vertical HEMT according to claim 1, further comprising a p-doped GaN layer arranged above the AlGaN-layer of the heterojunction, and underneath the gate contact.

4. The vertical HEMT according to claim 1, wherein a distance between the gate contact and the heterojunction is configured such that a voltage difference of at least 1 V between the gate contact and the at least one source contact opens a conductive channel at the heterojunction, whereby the vertical HEMT has a threshold voltage of at least 1 V.

5. The vertical HEMT according to claim 1, wherein the drain contact is laterally enclosed by an AlN-layer and/or an AlGaN-layer and/or a GaN-layer.

6. The vertical HEMT according to claim 1, wherein the at least one vertical pillar is laterally aligned with the gate contact.

7. The vertical HEMT according to claim 1, wherein the at least one source contact is laterally separated from the at least one vertical pillar.

8. The vertical HEMT according to claim 7, wherein a lateral separation between the at least one source contact and the at least one vertical pillar is at least 200 nm.

9. The vertical HEMT according to claim 1, wherein the supporting material is configured to be a current blocking layer.

10. The vertical HEMT according to claim 1, wherein the at least one vertical pillar comprises n-doped GaN and wherein the supporting material comprises a p-doped nitride semiconductor.

11. The vertical HEMT according to claim 9, wherein the supporting material comprises a superlattice of carbon-doped or iron-doped GaN layers and AlN spacer layers with a thickness less than 5 nm.

12. An electrical circuit comprising a first and a second vertical HEMT, the first and second vertical HEMTs being vertical HEMTs according to claim 1, the electrical circuit comprising an electrical separator configured to block current between the first and second vertical HEMT, the electrical separator comprising one or more of:

a first electrical insulator arranged on a lateral side of the heterostructure mesa of at least one of the first and second vertical HEMT;

a second electrical insulator arranged on a lateral side of the at least one source contact of at least one of the first and second vertical HEMT; and

the current blocking layer arranged on the lateral side of the GaN vertical connection of at least one of the first and second vertical HEMT.

13. A method for producing a vertical HEMT, the method comprising:

providing a base layer wherein the base layer comprises a substrate;

forming a pillar layer on the base layer, wherein the pillar layer comprises at least one vertical pillar and a supporting material laterally enclosing the at least one vertical pillar;

forming a heterostructure mesa on the pillar layer, the heterostructure mesa comprising an AlGaN-layer and a GaN-layer, together forming a heterojunction;

forming at least one source contact electrically connected to the heterostructure mesa;

forming a gate contact above both the heterostructure mesa and the at least one vertical pillar; and

forming a drain contact electrically connected to the at least one vertical pillar, the drain contact being a metal contact via through the substrate;

forming a current blocking layer arranged on a lateral side of a GaN

vertical connection, the GaN vertical connection being an electrical connection between the at least one source contact and the heterostructure mesa of the vertical HEMT, wherein said current blocking layer comprises carbon-doped or iron doped GaN;

wherein the at least one vertical pillar is forming an electron transport channel between the drain contact and the heterojunction.

14. The method according to claim 13, wherein the base layer comprises an $Al_{(1-y)}Ga_{(y)}N$-layer on the substrate, wherein said $Al_{(1-y)}Ga_{(y)}N$-layer is sputtered epitaxially aligned with the crystal orientation of the substrate, wherein said substrate is silicon <111> and said composition y is either 0 or 1, or a value therebetween.

15. The method according to claim 13, wherein forming the drain contact comprises etching through at least part of the substrate by deep reactive ion etching.

16. The vertical HEMT according to claim 10, wherein the supporting material comprises a superlattice of carbon-doped or iron-doped GaN layers and AlN spacer layers with a thickness less than 5 nm.