breaking design rules at the layer level for the first conductive level 116, the third conductive level 118, the second conductive level 120, and/or the fourth conductive level 122. The present embodiments achieve the use of sub-design rule spacing by forming each of the first conductive trace 112 and the second conductive trace 114 vertically and horizontally offset from each other (i.e., each of the horizontally conductive layers are vertically spaced apart from and horizontally offset from the adjacent horizontally conductive layer, so that conductive elements within a conductive layer do not overlap when viewed from above).

[0052] Stated another way, the present embodiments achieve sub-design rule spacing by forming each of the second conductive trace 114 in-between and over each of the first conductive trace 112, wherein the distance between each of the first conductive trace 112 and the second conductive trace 114, as viewed from above, varies with current sub-design rule spacing process techniques. As such, the first conductive trace 112 can be formed at the first conductive level 116 and/or the third conductive level 118 without breaking the design rules for this layer level, while, the second conductive trace 114 can be formed at the second conductive level 120 and/or the fourth conductive level 122 without breaking the design rules for that layer level.

[0053] It will be appreciated by those skilled in the art that the use of sub-design rule spacing permits the distance between the first conductive trace 112 and the second conductive trace 114, when viewed from above, to be smaller than what was previously achieved when using conventional minimum design rule spacing. For example, the distance between the first conductive trace 112 and the second conductive trace 114, when viewed from above, could be less than fifty (50) nanometers at the thirty-two (32) nanometer process node for the present embodiments. It is to be understood that by utilizing the sub-design rule spacing of the present embodiments, the capacitance density (capacitance per unit area) of the integrated circuit system 100 can be increased over that of conventional VPPCAP structures.

[0054] Referring now to FIG. 2, therein is shown a partial cross sectional view of back-end-of-line conductive layers formed within the integrated circuit system 100 during manufacture in accordance with an embodiment of the present invention. The integrated circuit system 100 includes a first region 200, a second region 202, a first dielectric layer 204 and a plug 206.

[0055] In some embodiments, the substrate 104 can include the first region 200 ~~may include~~ with a portion of the integrated circuit system 100 dedicated to the formation of the VPPCAP structure 102, of FIG. 1, and

the substrate 104 can include the second region 202 ~~may include~~ with a portion of the integrated circuit system 100 dedicated to the formation of an interconnect area over a logic region, for example.

[0056] Generally, the first dielectric layer 204 can act as a pre-metal dielectric layer, which separates the devices within the substrate 104 from the first conductive level 116, of FIG. 1. By way of example, the first dielectric layer 204 may include any material that electrically isolates and/or prevents the migration of mobile ionic contaminants between the substrate 104 and the BEOL conductive layers formed above the substrate 104. In some embodiments, the first dielectric layer 204 may include a doped silicon oxide or a glass type material. In other embodiments, the first dielectric layer 204 may also include silicon oxide, silicon nitride, or a combination thereof.

[0057] The plug 206 provides an electrical pathway from one conductive layer to an adjacent conductive layer or layers. The plug 206 can be strategically placed within the first dielectric layer 204 to form the desired electrical circuits or pathways between appropriate conductive layers. In some embodiments, the plug 206 may electrically connect the first conductive level 116 to the substrate 104, for example. Generally, the plug 206 may include any material that offers a low resistance to the passage of electrical current, such as a metal, a semiconducting material, or a combination thereof. By way of example, in some embodiments, the plug 206 may include tungsten.

[0058] It will be appreciated by those skilled in the art that the plug 206 and a top surface 208 of the first dielectric layer 204 can be planarized by a chemical mechanical planarization process, for example.

[0059] Referring now to FIG. 3, therein is shown the structure of FIG. 2 after forming the first conductive level 116. In some embodiments, an additional conductive layer, such as the first conductive level 116 can be formed within a second dielectric layer 300, such as an interlayer dielectric. In such cases, the second dielectric layer 300 may include an oxide, a nitride, or a combination thereof.

[0060] Within the first region 200, the first conductive level 116 can be offset from the plug 206 (e.g., not in contact with the plug 206) and within the second region 202, the first conductive level 116 can be formed over or on the plug 206. In some embodiments, the first conductive level 116 can be made from a material that offers a low resistance to the passage of electrical current, such as a metal, a semiconducting material, or a combination thereof. In

other embodiments, the first conductive level 116 can be made from copper (Cu). It will be appreciated by those skilled in the art that an optional barrier layer can be deposited before

What is claimed is:

1. A method of manufacturing an integrated circuit system comprising:

providing a substrate including front-end-of-line circuitry;

forming a first conductive level including a first conductive trace over the substrate;

forming a second conductive level spaced apart from the first conductive level and including a second conductive trace; and

connecting the first conductive level to a third conductive level with a viabar that passes through the second conductive level without contacting the second conductive trace.

2. The method as claimed in claim 1 wherein:

forming the second conductive level spaced apart from the first conductive level includes offsetting the second conductive trace within the second conductive level vertically and horizontally from the first conductive trace within the first conductive level.

3. The method as claimed in claim 1 wherein:

forming the first conductive trace and the second conductive trace includes forming the first conductive trace of a first polarity and forming the second conductive trace of a second polarity.

4. The method as claimed in claim 1 wherein:

connecting the first conductive level to the third conductive level includes forming a first conductive plate.

5. The method as claimed in claim 1 further comprising:

connecting the second conductive level to a fourth conductive level with a viabar that passes through the third conductive level without contacting the first conductive trace within the third conductive level.

6. A method for manufacturing an integrated circuit system comprising:

providing a substrate including a first region and a second region formed over the substrate;

forming a first conductive level including a first conductive trace over the substrate;

forming a second conductive level spaced apart from the first conductive level and including a second conductive trace;

forming a third conductive level including the first conductive trace over the first conductive level and connected to the first conductive level with an interconnect to form a first conductive plate within the first region; and

forming a fourth conductive level including the second conductive trace over the second conductive level and connected to the second conductive level with an interconnect thereby forming a second conductive plate within the first region.

7. The method as claimed in claim 6 wherein:

forming the first conductive plate and the second conductive plate includes forming the first conductive plate adjacent the second conductive plate.

8. The method as claimed in claim 6 wherein:

forming the first conductive plate and the second conductive plate includes forming the first conductive plate and the second conductive plate of opposite polarities.

9. The system as claimed in claim 6 wherein:

forming the first conductive plate and the second conductive plate includes forming a VPPCAP structure.

10. The system as claimed in claim 6 wherein:

forming the second conductive trace spaced apart from the first conductive trace permits the use of sub-design rule spacing.

11. An integrated circuit system comprising:

a substrate including front-end-of-line circuitry;

a first conductive level including a first conductive trace over the substrate;

a second conductive level spaced apart from the first conductive level and including a second conductive trace; and

the first conductive level connected to a third conductive level with a viabar that passes through the second conductive level without contacting the second conductive trace.

12. The system as claimed in claim 11 wherein:

the second conductive trace within the second conductive level is vertically and horizontally offset from the first conductive trace within the first conductive level.

13. The system as claimed in claim 11 wherein:

the first conductive trace includes a first polarity and the second conductive trace includes a second polarity.

14. The system as claimed in claim 11 wherein:

the first conductive level, the third conductive level and the viabar form a first conductive plate.

15. The system as claimed in claim 14 further comprising:

the second conductive level connected to a fourth conductive level with a viabar that passes through the third conductive level without contacting the first conductive trace within the third conductive level, wherein the second conductive level, the fourth conductive level and the viabar form a second conductive plate.

16. The system as claimed in claim 15 wherein:

the first conductive plate is adjacent the second conductive plate.

17. The system as claimed in claim 15 wherein:

the first conductive plate is a first polarity and the second conductive plate is a second polarity.

18. The system as claimed in claim 15 wherein:

the first conductive plate and the second conductive plate form a VPPCAP structure.

19. The system as claimed in claim 11 wherein:

the second conductive trace spaced apart from the first conductive trace includes sub-design rule spacing.

20. The system as claimed in claim 11 wherein:

the substrate includes front-end-of-line circuitry.

What is claimed is:

1. A method of manufacturing an integrated circuit system comprising:

providing a substrate including front-end-of-line circuitry;

forming a first conductive layer including adjacent first conductive traces over the substrate;

forming a viabar with a horizontal via length at least twice as long as a horizontal via width to separate horizontally the adjacent first conductive traces in the first conductive layer;

forming a second conductive layer spaced apart from and not overlapping the first conductive layer, the second conductive layer including adjacent second conductive traces separated horizontally by another of the viabar;and

connecting third conductive layer to the first conductive layer by one of the viabar separating the adjacent second conductive traces, the viabar connecting the first conductive layer and the third conductive layer passing through the second conductive layer without contacting the adjacent second conductive traces as part of a vertical parallel plate capacitor structure.

2. The method as claimed in claim 1 wherein:

forming the second conductive layer spaced apart from the first conductive layer includes offsetting the second conductive traces within the second conductive layer vertically and horizontally from the first conductive traces within the first conductive layer.

3. The method as claimed in claim 1 wherein:

forming the first conductive traces and the second conductive traces include forming the first conductive traces of a first polarity and forming the second conductive traces of a second polarity.

4. The method as claimed in claim 1 wherein:

connecting the first conductive layer to the third conductive layer includes forming a first conductive plate.

5. The method as claimed in claim 1 further comprising:

connecting the second conductive layer to a fourth conductive by another of the viabar passing through the third conductive layer without contacting the first conductive traces within the third conductive layer.

6. A method for manufacturing an integrated circuit system comprising:

providing a substrate including a first region and a second region formed over the substrate, the substrate including front-end-of-line circuitry;

forming a first conductive layer including adjacent first conductive traces over the substrate;

forming a viabar with a horizontal via length at least twice as long as a horizontal via width to separate horizontally the adjacent first conductive traces in the first conductive layer;

forming a second conductive layer spaced apart from and not overlapping the first conductive layer, the second conductive layer including adjacent second conductive traces separated horizontally by another of the viabar;

forming a third conductive layer including the adjacent first conductive traces over the first conductive layer and connected to the first conductive layer by one of the viabar separating the adjacent second conductive traces to form a first conductive plate within the first region as part of a vertical parallel plate capacitor structure, the viabar connecting the first conductive layer and the third conductive layer passing through the second conductive layer without contacting the adjacent second conductive traces; and

forming a fourth conductive layer including the second conductive traces over the second conductive layer and connected to the second conductive layer by another of a viabar to form a second conductive plate within the first region.

7. The method as claimed in claim 6 wherein:

forming the first conductive plate and the second conductive plate includes forming the first conductive plate adjacent the second conductive plate.

8. The method as claimed in claim 6 wherein:

forming the first conductive plate and the second conductive plate includes forming the first conductive plate and the second conductive plate of opposite polarities.

9. The method as claimed in claim 6 wherein:

forming the first conductive plate and the second conductive plate includes forming the vertical parallel plate capacitor structure.

10. The method as claimed in claim 6 further comprising:

forming the second conductive traces spaced in-between and over two of the first conductive traces.

11. An integrated circuit system comprising:

a substrate including front-end-of-line circuitry;

a first conductive layer including adjacent first conductive traces over the substrate;

a viabar with a horizontal via length at least twice as long as a horizontal via width separating horizontally the adjacent first conductive traces in the first conductive layer;

a second conductive layer spaced apart from and not overlapping the first conductive layer, the second conductive layer including adjacent second conductive traces separated horizontally by another of the viabar; and

a third conductive layer connected to the first conductive layer by one of the viabar separating the adjacent second conductive traces, the viabar connecting the first conductive layer and the third conductive layer passing through the second conductive layer without contacting the adjacent second conductive traces as part of a vertical parallel plate capacitor structure.

12. The system as claimed in claim 11 wherein:

the second conductive traces within the second conductive layer are vertically and horizontally offset from the first conductive traces within the first conductive layer.

13. The system as claimed in claim 11 wherein:

the first conductive traces include a first polarity and the second conductive traces include a second polarity.

14. The system as claimed in claim 11 wherein:

the first conductive layer, the third conductive layer and the viabar separating the adjacent second conductive traces form a first conductive plate.

15. The system as claimed in claim 14 further comprising:

a fourth conductive layer connected to the second conductive layer by another of the viabar passing through the third conductive layer without contacting the first conductive traces within the third conductive layer, wherein the second

conductive layer,the fourth conductive layer and the viabar passing through the third conductive layer form a second conductive plate.

16. The system as claimed in claim 15 wherein:
the first conductive plate is adjacent the second conductive plate.

17. The system as claimed in claim 15 wherein:
the first conductive plate is a first polarity and the second conductive plate is a second polarity.

18. The system as claimed in claim 15 wherein:
the first conductive plate and the second conductive plate form the vertical parallel plate capacitor structure.

19. The system as claimed in claim 11 wherein:
one of the second conductive trace is in-between and over two of the first conductive trace to achieve sub-design rule spacing.

20. The system as claimed in claim 11 wherein:
the substrate includes a first region with the vertical parallel plate capacitor structure and a second region with an interconnect area.