PATENT SPECIFICATION (11) 1340619

1340619

DRAWINGS ATTACHED

(21) Application No. 21832/71 (22) Filed 19 April 1971

(31) Convention Application No. 11541 (32) Filed 16 Feb. 1970

(31) Convention Application No. 47205 (32) Filed 18 June 1970 in

(33) United States of America (US)

(44) Complete Specification published 12 Dec. 1973

(51) International Classification H01L 13/00

(52) Index at acceptance

H1K 21Y 223 22Y 231 238 243 26X 274 275 277 279 304 311 312 315 316 320 323 325 345 34Y 353 413 41Y 422 42X 441 459 482 511 515 51Y 520 523 543 54Y 552 555 55Y 563 579 581 618 61Y

(72) Inventors WILLARD STERLING BOYLE
GEORGE ELWOOD SMITH and
DAWON KAHNG

(54) IMPROVEMENTS IN OR RELATING TO INFORMATION STORAGE DEVICES

(71) We, WESTERN ELECTRIC COMPANY, INCORPORATED, of 195 Broadway, New York City, New York State, United States of America, a Corporation organised and existing under the laws of the State of New York, United States of America, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed to be particularly described in and by the following statement:—

This invention relates to information storage devices.

There are many electrical devices in which information can be stored or represented e.g. by the polarity of magnetic domains in a sheet, hollow core or wire, or in the case of an optical image, in the form of electrostatic charge in a storage medium, as is usual practice in an image pick-up camera. The electrostatic charge pattern may be "read" with a scanning electron beam. Delay lines are also information storage devices and are typically acoustic or electromechanical with the information stored dynamically in a travelling elastic wave.

The present invention seeks to provide an information storage device which shall be versatile and have many of the advantages of the various storage devices mentioned above.

According to one aspect of this invention an information storage device comprises an insulating or semi-insulating storage medium for storing electrical charge carriers at a first storage site at or near a surface of said medium, means for detecting charge carriers at a detection site at or near said surface, and means for causing the transfer, when appropriately energised, within said medium of charge carriers from said first storage site towards said detection site.

The said transfer causing means may comprise a first insulating layer on said surface and a plurality of conductive field plates on said first insulating layer.

There may be included means for providing a voltage on each of said plates such as to produce a predetermined electric field E across said first insulating layer, the following relation being satisfied

$$\frac{\epsilon E}{e} > nt$$

where ϵ is the dielectric constant of said first insulating layer, e is the electron charge, t is the thickness of said storage medium, and n is the concentration of carriers in said medium.

Preferably there is included on the surface opposite said surface a second layer of insulating material, and, on said second layer, a conductive layer.

According to another aspect of this invention an information storage device includes a semiconductive charge carrier storage medium, means for detecting minority charge carriers at a detection site at or near a surface of said medium, and means for forming, when appropriately energised, at or near said surface a localised potential well for storing minority charge carriers and for causing, when appropriately energised, the transfer within said medium of minority charge carriers so stored (if any) towards said detection site.

The said means for forming and for causing may include a layer of piezoelectric material on said surface, and means for creating an acoustic wave in said piezoelectric layer. Preferably there is a conductive electrode on said piezoelectric layer.

According to a further aspect of this invention an information storage device includes a

semiconductive charge carrier storage medium, means for detecting minority charge carriers at a detection site at or near a surface of said medium, and means for forming, when appropriately energised, at or near said surface a plurality of localised potential wells for storing minority charge carriers at a corresponding plurality of storage sites and for causing, when appropriately energised, the transfer within said medium of minority charge carriers so stored (if any) from storage site to storage site towards said detection site.

The said means for forming and for causing may include an insulating layer on said surface, and a plurality of conductive electrodes on said layer, said device being such that when each said electrode in appropriately energised a potential well is formed thereunder in said medium.

The said means for forming and for causing may further include a layer of piezoelectric material overlying each said electrode, and means for creating an acoustic wave in said piezoelectric layer.

The said medium may be such as to produce said minority charge carriers in response to radiation incident thereon.

There may be provided means for introducing minority charge carriers for storage and transfer.

Such means may comprise a p—n junction, or a metal-insulator-semiconductor device energisable to avalanche.

The invention will now be described with reference to the accompanying drawings, in which:

FIGS. 1A to 1D schematically illustrate charge translation or transference;

FIG. 2 is a schematic front sectional view of a shift register;

FIG. 3 shows a pulse program for the shift register of FIG. 2;

FIG. 4 is a schematic front sectional view illustrating a preferred method of charge translation;

FIGS. 5A, 5B and 5C illustrate schematically various means for detecting the presence or absence of charge at an output position;

FIGS. 6A and 6B are provided to explain a preferred technique for enhancing charge translation;

FIG. 7 is a plan view of a multichannel shift register;

FIG. 8 is a plan view of one preferred form of conductor arrangement designed to avoid crossovers in a three-conductor control circuit.

FIG. 9 is a perspective view of a portion of a charge translating device illustrating a preferred electrical contact arrangement;

FIG. 10 is a front sectional view of a charge translating device showing an alternative electrical contact arrangement;

FIG. 11 is a schematic front sectional view of an image storage device;

FIG. 12 is a front sectional view of a device that does not require wire connections to each transfer stage;

FIG. 13 is a front sectional view illustrating a structure alternative to that of FIG. 12;

FIG. 14 is a schematic front sectional view of another device similar in many respects to the shift register of FIG. 2, and

FIG. 15 is a schematic front sectional view of part of the device of FIG. 14 showing a preferred form thereof.

The charge transfer mechanism, whilst basically similar in all embodiments described herein, will be described with reference to FIGS. 1A to 1D. In FIG. 1A a semiconductor substrate 10 is covered with a thin insulating film 11 and two metal electrodes 12 and 13 which form part of an array. Electrode 12 is biased while electrode 13 is not and a depletion region or potential well 14 forms under electrode 12. In FIG. 1B, minority charges 15, created through e.g. hole-electron pair generation from photon absorption, are shown migrating to the depletion region 14 and stored there. When electrode 13 is biased simultaneously with electrode 12, the depletion region extends continuously below both electrodes as shown in FIG. 1C and the charge redistributes across the enlarged layer. As the bias on electrode 12 is removed, as shown in FIG. 1D, the portion of the depletion region under electrode 12 collapses shifting all the charge to the potential well 14′ that is now associated with electrode 13. In a like manner the charge entity represented in FIG. 1D can be shifted to another location in the semiconductor. It will be recognised that the substrate 10 of FIGS. 1A to 1D can be p-type and the charges reversed in sign.

The shift register of FIG. 2 has a structure similar to that shown in FIGS. 1A to 1D. A semiconductor substrate 20 is covered with a dielectric layer 21 on which is formed a sequence of electrodes 22 to 24, in triplets designated *a* and *b* to *n* (being part of a series terminating with 24*n*). Conductors designated 22′, 23′ and 24′ join each third electrode. An input or generating stage 25 is an MIS device driven to avalanche condition. The charge generated at 25 migrates as shown to the potential well 27*a*.

The shift register can be operated in a recirculating mode either for increasing the storage duration, or for regenerating the signal to overcome noise or charge losses, by simply connecting the output signal back to the input stage through an appropriate regeneration circuit 33. Clearly also the shift register will find application in information or signal delay. By sequentially biasing conductors 23′, 24′ and 22′, the charge will shift into pocket 27*b*. In a like manner the charge is translated into pocket 27*n* and then into the depletion region

28 accompanying a p—n junction 29 of the output stage. A pulse output is then detected across a load 30 as shown. A bias source 31 is connected to electrode 32 to bias the junction.

Although the output stage shown utilises a p—n junction to extract charge collected from the terminal stage 24*n*, equally effective is a Schottky barrier device, an appropriate form of which is described in The Bell System Technical Journal, Vol. XLIV, No. 7, Sept. 1965 at pp. 1525—1528. Such charge detecting devices can be characterised by the term "barrier layer".

An exemplary pulse program for the shift register of FIG. 2 is shown in FIG. 3 which illustrates transmission of the binary code 1101. It is clear from FIG. 2 that each element 22*a* to 22*n* is simultaneously pulsed via conductor 22′, likewise for conductors 23′ and 24′. The pulses on each element are timed such that the time period between the initiation of sequential pulses, Δt, is less than three times the pulse width t_p. This ensures that the pulse on each sequential stage overlaps both the former and the subsequent stage; otherwise one potential well may collapse before the next one is accessible to the charge.

Referring back to FIG. 1C, it will be appreciated that the charge transfer time for that portion of charge situated under electrode 12 will be equal to the fall time of the pulse in FIG. 3. Experimental evidence indicates that the transfer time under the conditions outlined is quite fast. However, if the pulse program of FIG. 3 is comparably fast, it may be advantageous to use a pulse shape that gives a longer fall time e.g. a sine wave.

Preferably a continuous uniform bias is present on all conductors so as to maintain at least a shallow depletion layer over the entire surface of the device. This bias should be at least equal to the threshold voltage for producing inversion under steady state conditions. In this way troublesome surface states, which are inevitably present at semiconductor-insulator interfaces (and which cause adverse surface recombination) can be maintained relatively free of majority carriers. Thus by isolating the bulk of the majority carriers from the interface via a space-charge layer, the carriers in the surface states, having once recombined with minority carriers, cannot then be replenished. This technique, which simply requires a prebias on every metal contact, ensures a long lifetime for the minority carriers constituting the signal. In a device having many stages this expedient may be essential.

The modification just described is illustrated in FIG. 4. The device shown corresponds to a middle portion of the shift register of FIG. 2. A semiconductor base layer 40, which again is n-type, an insulating layer 41, and metal contacts 42*a*, 43*a*, 44*a*, 42*b*, 43*b* and 44*b* and the associated conductors 42′, 43′, and 44′ correspond to similar elements in FIG. 2. A continuous bias voltage V′ is present on all conductors to form a uniform depletion region 45 over the entire device. Potential wells 46 are formed under contacts 42*a* and 42*b* as the result of the pulse voltage V_p superimposed on the bias voltage V′.

Although the shift register of FIG. 2 was described as having an avalanche device for creating charge at the input location 25, there are several alternative methods for creating minority charge carriers. For example, if the input stage comprises a p—n junction, minority charge carriers can be injected into the bulk region of the semiconductor by forward bias pulses corresponding to the desired input signal. Alternatively carriers can be injected by MIS surface avalanching as described in Journal of Applied Physics, Vol. 9, No. 12, p. 444. A hybrid structure employing a metal-oxide surface contact on a p—n junction is effective for the same purpose. Another alternative is to generate hole-electron pairs by photon absorption or absorption of other ionising radiation. This is described in copending U.K. patent application No. 25936/69 (Serial No. 1241379). The minority charge carriers will diffuse to a nearby depletion region which in the case of the shift register of FIG. 2 is the first stage 27*a*. A means for achieving this is shown in dotted lines at 33 in FIG. 2 as a light-source—in this case, a schematic representation of an electroluminescent diode.

The output stage can also assume a variety of forms some of which will be described with reference to FIGS. 5A to 5C. These figures show the terminal section of the device of FIG. 2 including the last transfer stage 24*n*. Each of these output stages are charge detection devices constructed according to known principles. In FIG. 5A the detector is an MIS device and is therefore especially convenient, from a processing standpoint, where an MIS array comprises the transfer stages. With the semiconductor depleted, the capacitance associated with detector electrode 50 will indicate the presence or absence of externally introduced charge in the depleted region 51. The capacity across the MIS detector is measured by a standard capacitive bridge as shown and the value indicated at detector 52. The bias source 53 is arranged via switch 54 to intermittently bias that portion of the semiconductor below electrode 50, first to establish the depletion region for attracting the charge to be detected, and then to collapse the depleted region to recombine the charge which may have accumulated.

In the detection stage of FIG. 5B an alternating current source 55 is connected to two adjacent field plates 56 and 57, the latter again comprising MIS devices with semiconductor 20 and insulating layer 21. A bias source 58 maintains a depletion region 59

beneath both electrodes 56 and 57. If charge is present in the terminal transfer stage 24*n* it is transferred to the potential well accompanying plate 56 on its negative half cycle, and then towards the well of electrode 57 on the latter's negative half cycle. This transfer of charge back and forth beneath electrodes 56 and 57 changes the a.c. impedance of the circuit from its value without charge in the depletion region. The presence or absence of charge is thus detectable across an impedance 60 by a potentiometer 61. The switch 62 serves to erase the charge in the manner of switch 54 of FIG. 5A. The speed of erase can be enhanced by providing a switching network to reverse the d.c. bias rather than merely removing the bias.

The detection stage of FIG. 5C relies on a direct voltage measurement to detect interface charge Q_I accumulated between semiconductor 20 and insulator 21. The electrode 63 is biased negatively via source 64 connected in series with a blocking capacitance, shown as a capacitor 65, but may alternatively be a diode. A change in the charge level Q_I is reflected by a change in the equivalent capacitance of the MIS device. This affects the capacitive division between that element and the capacitor 65 resulting in a change in V_D. The voltage V_D can be measured in various ways, e.g. at the gate of a field-effect transistor. Shown in FIG. 5C is a field-effect device integrated with the semiconductor base 20 of the storage device. A p-region 20A provides isolation according to known integrated circuit techniques. The voltage V_D being measured is connected to the gate electrode 66. The insulating layer for the gate is shown as an extension of insulating layer 21. Source and drain regions 67 and 68 are diffused through windows formed in this layer. Source and drain electrodes 69 and 70 are connected through load 71 to bias source 72. Detector 73 indicates the conduction state of the FET which reveals the presence or absence of charge Q_I in the following manner.

A positive pulse delivered by power source 64 recombines any residual charge Q_I and primes the device for detection. A negative pulse places negative charge on plate 63 and depletes the region under that electrode for collecting holes delivered (or not delivered) from terminal stage 24*n*. The gate 66 is biased at the same potential leaving the FET in an "ON" condition indicated at 73. If charge Q_I enters the region below plate 63, the negative potential on the plate will be reduced. The corresponding reduction in potential at the gate electrode 66 will place the FET in an "OFF" condition. If there is no charge Q_I the FET remains "ON".

The device of FIG. 5C is shown partly integrated. The FET device can be used separately or the device can be further integrated, e.g. the elements 65, 71 and the electrical connections can be integrated.

The charge translating mechanism described in connection with FIG. 1 relies on thermal diffusion to transport carriers from potential well 14 to potential well 14'. While this transport mechanism will often be adequate, the response time of devices using this mechanism can be significantly reduced by using an electric field to drive the charge to the new location. In many cases the use of the drive field will also improve the collection efficiency. One way of achieving this is to shape the potential well so that a field gradient exists between adjacent wells. This, which for the purpose of this description will be termed "field enhancement", will be described by way of example with reference to FIGS. 6A and 6B.

FIG. 6A shows two conductors 72 and 73 situated on insulating layer 74 which in turn covers semiconductor substrate 75. With the conductors 72 and 73 biased, their respective depletion layers appear to have shapes indicated by dashed lines 76 and 77. These lines, which represent the boundaries of the depleted region of the semiconductor also are a function of the field potential at the semiconductor-insulator interface. Thus it is convenient to consider these boundary lines as field profiles along the surface of the semiconductor where the charge is stored. As a consequence of making the dimensions of the electrode comparable to, or less than, the thickness of the insulator, the field approaches the situation where it appears to emanate as if from a point rather than a plate (as in FIG. 1) and produces a continuous field gradient along the surface. This field gradient is aptly described as a potential well and tends to confine the charge at its centre. When these wells are made to overlap (a condition implicit from the previous discussion, e.g. the pulse program of FIG. 3) the composite field profile is described by the chain-dotted line 78. Now it is intuitively obvious that the charges will transport from the region directly under electrode 72 toward electrode 73. After the depletion field represented by line 76 collapses, the charges will be swept to the surface region of highest potential in the well represented by line 77, or directly under electrode 73.

Field enhancement can be made more effective by using a shaped pulse as will be described with reference to FIG. 6B. For example, if a saw-tooth pulse is applied to electrodes 72 and 73, then at a time t_1 during the period of pulse overlap (the charge translating period), electrode 72 will be biased at a lower voltage than electrode 73. This is indicated adjacent the respective pulse forms. The separate field profiles at t_1 are described by dashed lines 79 and 80 with the composite profile appearing as dotted line 89. The field

gradient in the direction of desired charge translation extends instantaneously all the way to the region immediately below electrode 73.

Other ways of producing a field gradient or drive field for the charge (or absence of charge) accumulated at the initial storage location will occur to those skilled in the art.

The one dimension shift register shown in FIG. 2 can advantageously be incorporated in a multichannel register as shown in FIG. 7. It is evident that the linear array of FIG. 2 requires at least n crossovers (the figure shows $3n$—3 crossovers but a straightforward modification reduces this number to n). Crossovers are used more economically in the arrangement of FIG. 7 wherein the same number of crossovers may provide a large number of channels. FIG. 7 shows four channels but this number can be extended without adding additional crossover connections. The conductor arrangement of conductors 81′, 82′ and 83′ is the same as that in FIG. 2 with conductor 81′ connected to contacts 81*a* to 81*n* in sheet 86 and likewise with conductors 82′, 83′ and electrodes 82*a* to 82*n* and 83*a* to 83*n*. Input stages 84 and output stages 85 have been discussed previously.

An electrode configuration requiring a minimum number of crossovers is shown in FIG. 8 which shows a portion of a device which may, for example, be a plan view of a device similar to that of FIG. 4 and in which the conductors are so arranged as to avoid the necessity of crossover connections. Using numbers preceded by "1" to indicate elements corresponding with those of FIG. 4, the three conductors 142′, 143′ and 144′ are deposited directly upon a raised portion of the insulating layer 140 and interconnect electrodes 142*a*, 142*b*, 143*a*, 143*b* and 144*a*, 144*b*, respectively. The path followed by the charge as it is stepped through this section is indicated by the dashed line 145. In this connection it should be appreciated that the charge is being translated under conductor wires and thus forms a convenient "cross-under" arrangement.

Other arrangements similar to that of FIG. 8 will occur to those skilled in the art. Such arrangements can be described broadly as having a plurality of electrodes in which every third electrode is connected to one of three conductors and is adjacent to two electrodes, each of which is connected to a separate conductor of the remaining two, with all of the conductors and electrodes deposited on a single substrate surface. The disposition of the conductors along the surface of the device can be an important consideration. In a large array it is impractical to bond each lead to its associated electrode. Consequently the charge transfer circuit would ordinarily be printed directly on the insulator covering the substrate. However, the effectiveness of the invention often relies on careful control of the field profile at the semiconductor insulator interface and if the conductors are in direct contact with the insulator, the field from each lead will perturb the desired field profile. To overcome this a dual thickness oxide can be formed over the semiconductor. Such an arrangement is shown in FIG. 9 in which the semiconductor substrate 110 is first coated with a thin insulating layer 111. Next a thicker layer of another insulating material is formed on layer 111 and etched to form a grid 112 with openings for the metal field plates 113 which can be deposited along with interconnections 114 in a single photolithographic operation. Some overlap is shown in the figure to ensure complete covering of the site. The conductor paths 114 to the electrodes 113 are isolated from the substrate by the thick insulator 112. The dual thickness insulating layer may be made from two different insulating materials, such as SiO_2 and Si_2N_3 that have different etching characteristics. Thus when the second layer is etched to form windows for the electrodes an etch can be selected which does not attack the first insulating layer. An alternate procedure known in the art for forming a dual thickness layer is to deposit a continuous first layer, etch the windows, and deposit another uniform layer.

An especially convenient fabricating technique is illustrated in FIG. 10 which is a front sectional view of a portion of a planar processed device. The semiconductor substrate 120 is again covered with a suitable thin insulating layer 121. A continuous metal layer is deposited on layer 121 and etched to form discrete metal electrodes 122—124. A continuous insulating layer 125 is then deposited over the electrodes 122—124. Windows 127 are etched in layer 125 to the underlying metal and a ribbon or beam lead conductor 128 is then deposited so as to contact electrodes 122—124. The procedure has the advantage that it is devoid of any critical photoresist alignment steps.

The production of minority charge carriers in the semiconductor by photon absorption, as mentioned previously, and as described in United States Patent No. 3,403,284, makes possible another category of device in accordance with the invention, e.g. an image pick-up device, one form of which is illustrated schematically in FIG. 11. As will be appreciated, information is read into the device in parallel. Light in the form of the optical image being recorded is incident on the side of the semiconductor 130 opposite to the storage control elements. The latter again comprise metal-insulator-semiconductor devices as in FIG. 2 but they could take any of a variety of suitable forms, e.g. other types of depletion layer devices such as transistor-type structures. The array shown contains

three bit locations comprising three electrodes designated 132*a* to 134*a*, 132*b* to 134*b*, and 132*c* to 134*c* connected to conductors 132′, 133′ and 134′ in a manner similar to the arrangement of FIG. 2. Apart from the parallel read-in of information, the charge translation and readout operation can be as described above. The linear array shown in FIG. 11 may represent one raster line in a video system. The charge is stored at locations 132*a*—132*c* during the optical integration period and is read out serially by translating the charge to the readout section (refer to FIG. 2). By sequentially reading each raster line, the video frame is constructed.

As will now be appreciated, the charge translation mechanism involves a potential well travelling along the surface of the semiconductor. The use of electrical connections to achieve this has already been described but other means of producing a travelling potential may offer distinct advantages. For example, the field accompanying an acoustic wave travelling in a piezoelectric medium is an attractive alternative. FIG. 12 shows a portion of the shift register of FIG. 2 with semiconductor 159, insulator 160, and a series of metal contacts 161 corresponding essentially to similar elements in FIG. 2. A piezoelectric layer 162 is deposited over the metal contacts. This layer may be composed of a suitable piezoelectric material such as zinc oxide or cadmium sulphide, and may be evaporated or sputtered onto the device. A piezoelectric transducer (not shown) or other suitable means creates an ultrasonic wave which propagates through the layer 162 parallel to the surface of the device. The electric field accompanying the elastic deformation in the piezoelectric layer sequentially biases the electrodes 161 and creates potential wells 163 that travel along the surface of semiconductor 159.

The discrete electrodes of FIG. 12 can be eliminated. For example, FIG. 13 shows a device in which the semiconductor 170 is coated directly with a piezoelectric layer 171. In this device the field propagated in association with the elastic wave in medium 171 (initiated by an appropriate ultrasonic generator not shown) is used to form travelling potential wells 172. A metal electrode 173 may be used to create a uniform depletion layer over the entire charge translating surface for the purpose described in connection with FIG. 4.

Materials suitable for the manufacture of the devices described are available and well understood. For example, the devices can be fabricated of silicon and silicon dioxide in accordance with well-established principles. Combinations of insulators such as

SiO_2—SiN, SiO_2—Al_2O_3, etc.

are especially useful in certain circumstances as the insulating layer. Known electrode materials are gold, aluminium and doped-silicon. A useful structure for the device of FIG. 2 could employ 10 ohm/cm. n-type silicon as the base layer 20, and 1,000 Å to 2,000 Å of thermally grown SiO_2 as the layer 21. The oxide which has given the best results so far is a dry oxide 1,200 Å thick grown in oxygen at 1,100°C for one hour and annealed in a nitrogen atmosphere for one hour at 400°C. The flatband potential for this oxide is typically −5 V. and the surface state density is of the order of 10^{10} states/cm^2. Electrodes 22—24 may be gold in any typical thickness, e.g. 0.1 to a few microns. An appropriate charge generator is a p-region, having a boron concentration of 10^{18} atoms/cm^3, driven at avalanche, i.e. a few volts. The detector may be a similar p—n junction. The creation and detection of minority carriers in semiconductors can be accomplished by well-known techniques.

The dimensions of the transfer array can vary widely. The spacing between electrodes depends upon the extent of the space charge region permitted. For example if the semiconductor is 10 ohm/cm. silicon and a voltage of 10 volts is used, the depletion region will extend approximately 5 μ. This would suggest an electrode spacing of the order of a few microns for the necessary overlap. It is to be understood, however, that the invention is in no way limited to silicon or its associated technology.

The devices described so far are essentially minority carrier devices, that is, the charge carriers that represent the information are minority carriers in the semiconductor. As will be appreciated however, the invention is not so limited. The invention can be carried into effect with a storage medium in which the active regions or storage sites are inherently depleted of carriers. Such a storage medium can be one of several known insulating or semi-insulating semiconductors. These materials have been of interest for some time, often in connection with piezoelectric and photoelectric effects. Examples of some semi-insulating materials which may be used for carrying out this invention are the II—VI compounds, especially ZnO, CdS, ZnS, ZnSe and CdSe. These materials are ionic semiconductors with large bandgaps and generally low charge carrier density. Other suitable materials having these properties are $KTaO_3$ and $BaTiO_3$. These materials normally occur as n-type semiconductors although this property is not essential of indeed important for the purpose of the invention. In n-type material the charges injected, translated and detected would advantageously be electrons. There are certain advantages in the use of these materials. The electrical field required to store and translate the charge representing information can be comparatively small. The

tolerances on the spacing between storage sites are in some cases less severe than in "minority carrier" charge coupled devices.

Since certain of these materials have large bandgaps, thermal generation of carriers or "noise" is characteristically low. This permits longer carrier lifetime and consequently longer storage times. Preferably the material has a bandgap exceeding 1.5 volts but less than 8 volts.

Considerable freedom exists in the selection of materials in terms of their surface or interface properties. With the present state of the art, the surface state density is characteristic of the materials forming the interface. A reduction in the number of surface states (recombination sites) made possible through the use of new combinations of materials may result in longer carrier lifetime and more efficient transfer. A further advantage is that the carriers representing the information can be injected directly into the device through an ohmic contact. The detection stage can also comprise an ohmic contact.

Referring now to Fig. 14, the storage medium 180 is of insulating or semi-insulating material. This means that during operation the material is depleted of free carriers that could combine with charge being translated between storage sites. Specific materials that can conveniently be prepared with this property and that are considered advantageous are ZnO, ZnS, CdS and $KTaO_3$.

An insulating layer 181 of a high quality dielectric material has properties suitable for the intermediate layer of an MIS device. SiO_2 and Al_2O_3 are exemplary materials. Metal field plates 182*a*, 182*b*, 182*n*, 183*a*, 183*b*, 183*n*, 184*a*, 184*b* and 184*n* are connected to a three wire drive system including conductors 182, 183 and 184 which in operation are sequentially biased to create an apparent travelling field along the surface of the semi-insulating body 180. Carriers injected through an input stage 185 will be carried by this field to an output stage 186 where the presence or absence of charge is detected in the manner described previously.

The material 180 can be defined more specifically by the expression

$$\frac{\epsilon E}{e} > nt \qquad (1)$$

where ϵ is the dielectric constant of the insulating layer 181, E is the electric field across that layer, e is the electron charge (1.6×10^{-9}), t is the thickness of medium 180, and n is the free carrier concentration of the medium 180.

The product ϵ E defines the polarisation P of the insulator 181. The observed polarisation for an insulator of exceptional quality is 10×10^{-6} coulombs cm^{-2}. Thus a practical maximum for the quantity P/e is of the order of 6×10^{13}, so that Equation (1) can be reduced to:

$$nt < 6 \times 10^{13} \qquad (2)$$

While these expressions serve to distinguish such materials from the more conventional semiconductors discussed previously, the material shown should not be so highly insulating that the mobility is so low that hole or electron conduction is not practical. For this purpose the material should have a mobility of at least $10^{-4} cm^2$/volt sec. While typical materials which may be employed have bandgaps of the order of a few volts, there is no theoretical maximum since the storage medium itself does not have to supply carriers. It is however necessary to have a barrier difference, e.g. at least one volt, between the storage medium and the adjacent insulator. Thus for example, if the storage medium is a high bandgap material, such as SiO_2, the insulator should have a higher bandgap (e.g. BeO).

Although the input and output stages, or either of them, can comprise ohmic contacts for direct injection and/or collection of carriers, in some cases it may be advantageous to include a rectifying barrier at either site, e.g. as part of a pulse-forming or pulse-detection network. In such cases input stage 185 or output stage 186 may comprise a Schottky barrier contact.

Preferably, as shown in FIG. 15, there is provided an MIS layer consisting of an insulating layer 187 and a metal layer 188 on the opposite side of the semi-insulating body 180. This allows a field to be impressed on the body 180, without injecting carriers, to restrict the charge being transferred to the active surface region of the device thereby increasing the charge transfer efficiency. This expedient is also useful when the body 180 is very thin as, for example, in the case where it is a deposited thin film. A bias means 189 is made negative with respect to the injecting contact 185 in the case where the material 180 is n-type. The layer 187 can be conveniently formed in the same operation as layer 181.

Reference is directed to our copending patent application no. 21830/71 (Serial No. 1340617) which relates to semiconductor devices in which information is storable in the form of charge carriers.

WHAT WE CLAIM IS:—

1. An information storage device comprising an insulating or semi-insulating storage medium for storing electrical charge carriers at a first storage site at or near a surface of said medium, means for detecting charge carriers at a detection site at or near said surface, and means for causing the transfer,

tolerances on the spacing between storage sites are in some cases less severe than in "minority carrier" charge coupled devices.

Since certain of these materials have large bandgaps, thermal generation of carriers or "noise" is characteristically low. This permits longer carrier lifetime and consequently longer storage times. Preferably the material has a bandgap exceeding 1.5 volts but less than 8 volts.

Considerable freedom exists in the selection of materials in terms of their surface or interface properties. With the present state of the art, the surface state density is characteristic of the materials forming the interface. A reduction in the number of surface states (recombination sites) made possible through the use of new combinations of materials may result in longer carrier lifetime and more efficient transfer. A further advantage is that the carriers representing the information can be injected directly into the device through an ohmic contact. The detection stage can also comprise an ohmic contact.

Referring now to Fig. 14, the storage medium 180 is of insulating or semi-insulating material. This means that during operation the material is depleted of free carriers that could combine with charge being translated between storage sites. Specific materials that can conveniently be prepared with this property and that are considered advantageous are ZnO, ZnS, CdS and $KTaO_3$.

An insulating layer 181 of a high quality dielectric material has properties suitable for the intermediate layer of an MIS device. SiO_2 and Al_2O_3 are exemplary materials. Metal field plates 182*a*, 182*b*, 182*n*, 183*a*, 183*b*, 183*n*, 184*a*, 184*b* and 184*n* are connected to a three wire drive system including conductors 182, 183 and 184 which in operation are sequentially biased to create an apparent travelling field along the surface of the semi-insulating body 180. Carriers injected through an input stage 185 will be carried by this field to an output stage 186 where the presence or absence of charge is detected in the manner described previously.

The material 180 can be defined more specifically by the expression

$$\frac{\epsilon E}{e} > nt \qquad (1)$$

where ϵ is the dielectric constant of the insulating layer 181, E is the electric field across that layer, e is the electron charge (1.6×10^{-9}), t is the thickness of medium 180, and n is the free carrier concentration of the medium 180.

The product ϵ E defines the polarisation P of the insulator 181. The observed polarisation for an insulator of exceptional quality is 10×10^{-6} coulombs cm^{-2}. Thus a practical maximum for the quantity P/e is of the order of 6×10^{13}, so that Equation (1) can be reduced to:

$$nt < 6 \times 10^{13} \qquad (2)$$

While these expressions serve to distinguish such materials from the more conventional semiconductors discussed previously, the material shown should not be so highly insulating that the mobility is so low that hole or electron conduction is not practical. For this purpose the material should have a mobility of at least $10^{-1} cm^2/volt\ sec$. While typical materials which may be employed have bandgaps of the order of a few volts, there is no theoretical maximum since the storage medium itself does not have to supply carriers. It is however necessary to have a barrier difference, e.g. at least one volt, between the storage medium and the adjacent insulator. Thus for example, if the storage medium is a high bandgap material, such as SiO_2, the insulator should have a higher bandgap (e.g. BeO).

Although the input and output stages, or either of them, can comprise ohmic contacts for direct injection and/or collection of carriers, in some cases it may be advantageous to include a rectifying barrier at either site, e.g. as part of a pulse-forming or pulse-detection network. In such cases input stage 185 or output stage 186 may comprise a Schottky barrier contact.

Preferably, as shown in FIG. 15, there is provided an MIS layer consisting of an insulating layer 187 and a metal layer 188 on the opposite side of the semi-insulating body 180. This allows a field to be impressed on the body 180, without injecting carriers, to restrict the charge being transferred to the active surface region of the device thereby increasing the charge transfer efficiency. This expedient is also useful when the body 180 is very thin as, for example, in the case where it is a deposited thin film. A bias means 189 is made negative with respect to the injecting contact 185 in the case where the material 180 is n-type. The layer 187 can be conveniently formed in the same operation as layer 181.

Reference is directed to our copending patent application no. 21830/71 (Serial No. 1340617) which relates to semiconductor devices in which information is storable in the form of charge carriers.

WHAT WE CLAIM IS:—

1. An information storage device comprising an insulating or semi-insulating storage medium for storing electrical charge carriers at a first storage site at or near a surface of said medium, means for detecting charge carriers at a detection site at or near said surface, and means for causing the transfer,

when appropriately energised, within said medium of charge carriers from said first storage site towards said detection site.

2. A device as claimed in claim 1 wherein said medium has a bandgap in the range 1.5 volts to 8.0 volts.

3. A device as claimed in claim 1 or 2 wherein said medium is of ZnO, ZnS, CdS, CdSe, ZnSe, $BaTiO_3$ or $KTaO_3$.

4. A device as claimed in any one preceding claim wherein said transfer causing means comprises a first insulating layer on said surface, and a plurality of conductive field plates on said first insulating layer.

5. A device as claimed in claim 4 including means for providing a voltage on each of said plates such as to produce a predetermined electric field E across said first insulating layer, and wherein the following relation is satisfied

$$\frac{\epsilon E}{e} > nt$$

where ϵ is the dielectric constant of said first insulating layer, e is the electron charge, t is the thickness of said storage medium, and n is the concentration of carriers in said medium.

6. A device as claimed in claim 5 wherein $nt < \times 10^{13}$.

7. A device as claimed in any one preceding claim including on the surface opposite said surface a second layer of insulating material, and, on said second layer, a conductive layer.

8. An information storage device including a semiconductive charge carrier storage medium, means for detecting minority charge carriers at a detection site at or near a surface of said medium, and means for forming, when appropriately energised, at or near said surface a localised potential well for storing minority charge carriers and for causing, when appropriately energised, the transfer within said medium of minority charge carriers so stored (if any) towards said detection site.

9. A device as claimed in claim 8 wherein said means for forming and for causing includes a layer of piezoelectric material on said surface, and means for creating an acoustic wave in said piezoelectric layer.

10. A device as claimed in claim 9 including a conductive electrode on said piezoelectric layer.

11. An information storage device including a semiconductive charge carrier storage medium, means for detecting minority charge carriers at a detection site at or near a surface of said medium, and means for forming, when appropriately energised, at or near said surface a plurality of localised potential wells for storing minority charge carriers at a corresponding plurality of storage sites and for causing, when appropriately energised, the transfer within said medium of minority charge carriers so stored (if any) from storage site to storage site towards said detection site.

12. A device as claimed in claim 11 wherein said means for forming and for causing includes an insulating layer on said surface, and a plurality of conductive electrodes on said layer, said device being such that when each said electrode is appropriately energised a potential well is formed thereunder in said medium.

13. A device as claimed in claim 12 wherein said means for forming and for causing further includes a layer of piezoelectric material overlying each said electrode, and means for creating an acoustic wave in said piezoelectric layer.

14. A device as claimed in claim 12 or 13 wherein said medium is silicon and said insulating layer is silicon-dioxide.

15. A device as claimed in any one of claims 8 to 14 wherein said medium is such as to produce said minority charge carriers in response to radiation incident thereon.

16. A device as claimed in any one of claims 8 to 14 including means for introducing minority charge carriers for storage and transfer.

17. A device as claimed in claim 16 wherein said means for introducing minority charge carriers comprises a p—n junction.

18. A device as claimed in claim 16 wherein said means for introducing minority charge carriers comprises a metal-insulator-semiconductor device energisable to avalanche.

19. A device as claimed in any one of claims 16 to 18 wherein said detecting means is coupled to said means for introducing minority charge carriers.

20. A device as claimed in any one of claims 8 to 19 wherein said detecting means comprises a metal-insulator-semiconductor device.

21. Information storage devices substantially as herein described with reference to FIGS. 1 to 13 of the accompanying drawings.

22. An information storage device substantially as herein described with reference to FIG. 14 or 15 of the accompanying drawings.

C. S. T. BUCKLEY,
Chartered Patent Agent,
5 Mornington Road,
Woodford Green, Essex.
Agent for the Applicants.

Printed for Her Majesty's Stationery Office, by the Courier Press, Leamington Spa, 1973.
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.