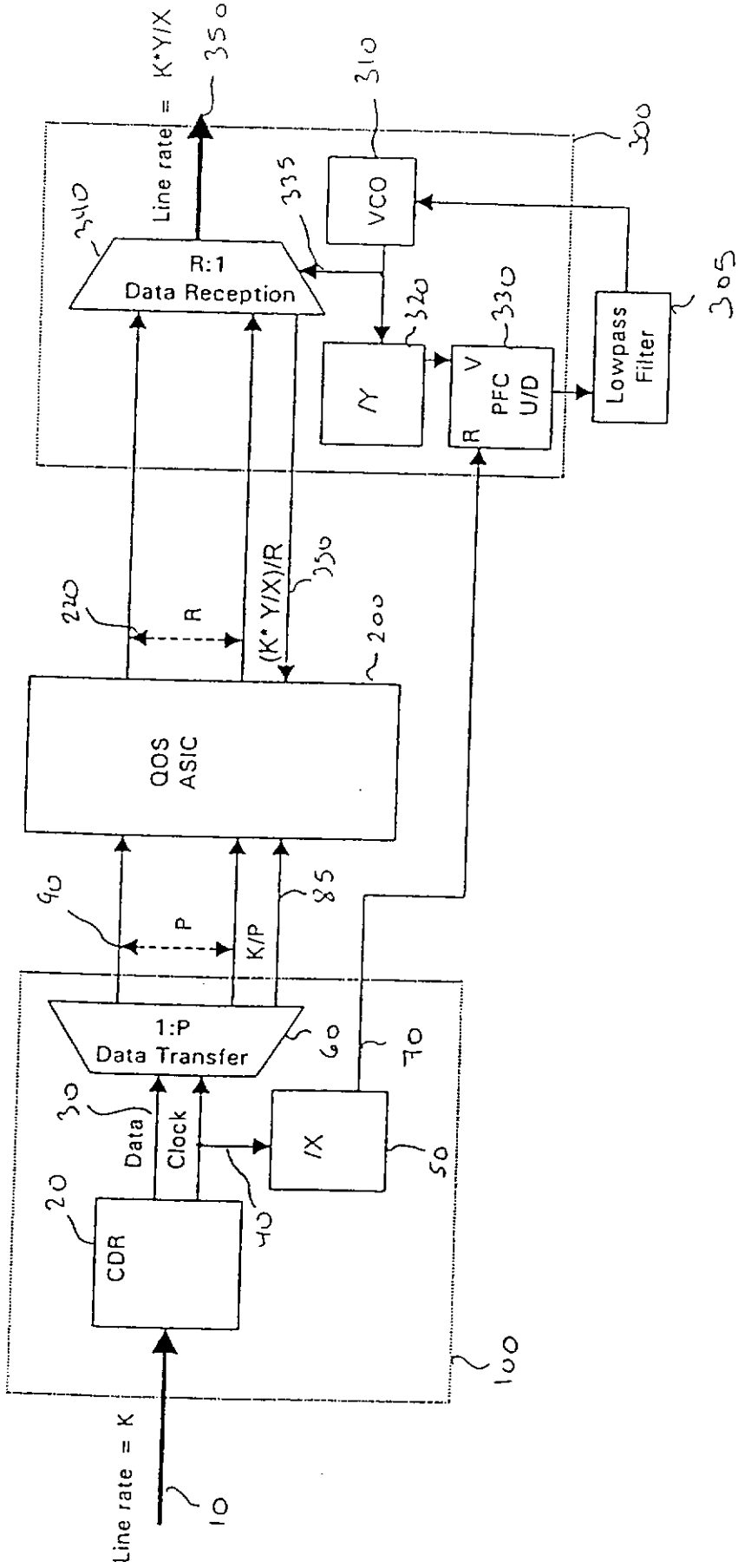

Line rate = K*Y/X
350
310
300
Line rate
335
VCO
340
R:1
Data Reception
320
330
305
/Y
V
PFC
U/D
R
Lowpass
Filter
220
R
(K*Y/X)/R
350
200
QOS
ASIC
40
P
K/P
85
1:P
Data Transfer
60
70
30
Data
Clock
/X
50
20
CDR
40
100
Line rate = K
10

Fig. 1

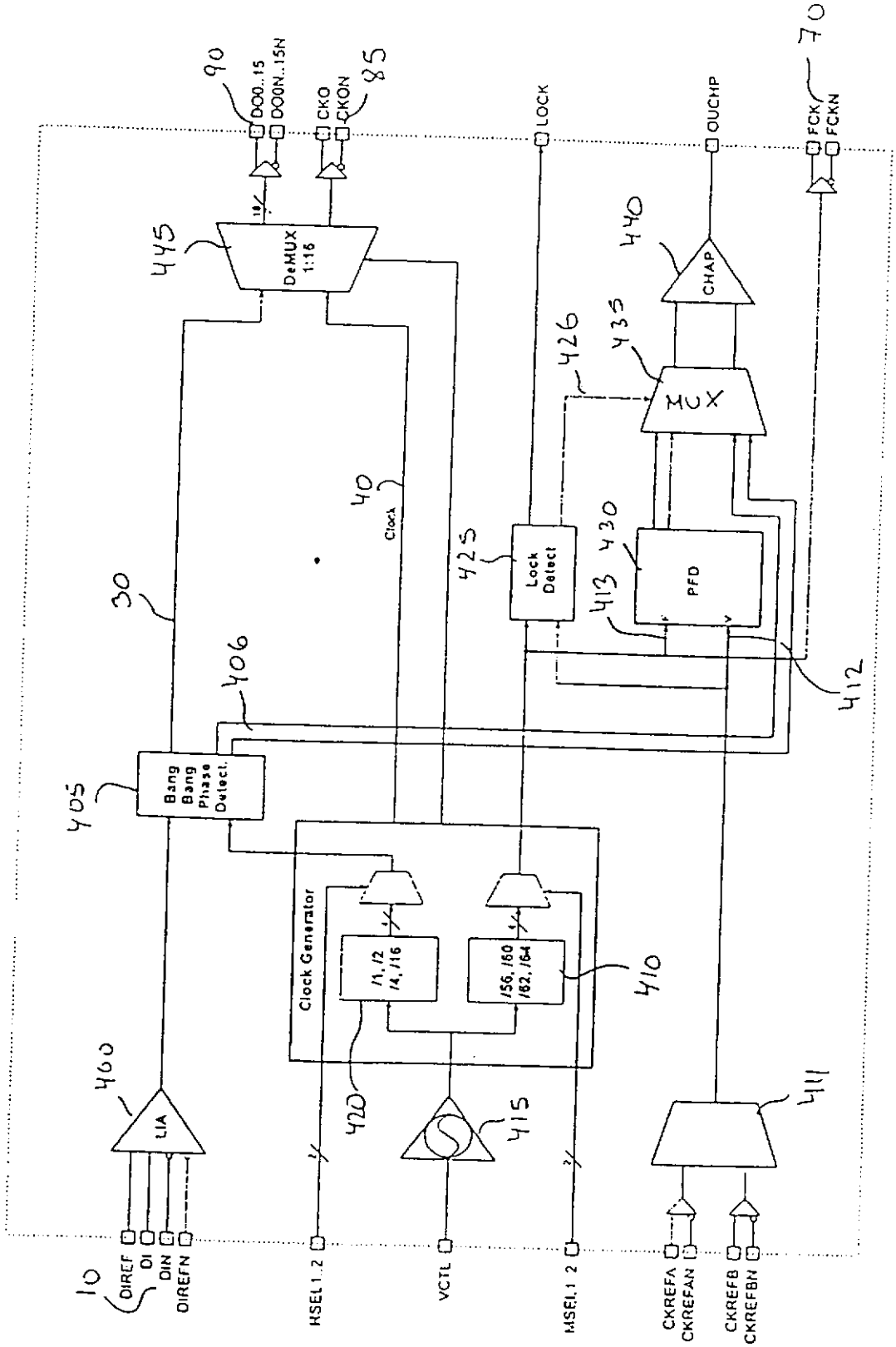

90
D00..15
D00N..15N
CKO
CKON
85
LOCK
OUCHP
70
FCK
FCKN
445
DeMUX 1:16
440
CHAP
426
435
MUX
40
Clock
425
Lock Detect
430
PFD
413
412
30
406
405
Bang Bang Phase Detect.
Clock Generator
11, 12 14, 16
156, 160 162, 164
410
460
LIA
420
415
411
10
DIREF
DI
DIN
DIREFN
HSEL1..2
VCTL
HSEL1..2
CKREFA
CKREFAN
CKREFB
CKREFBN

Fig. 2

Fig. 2

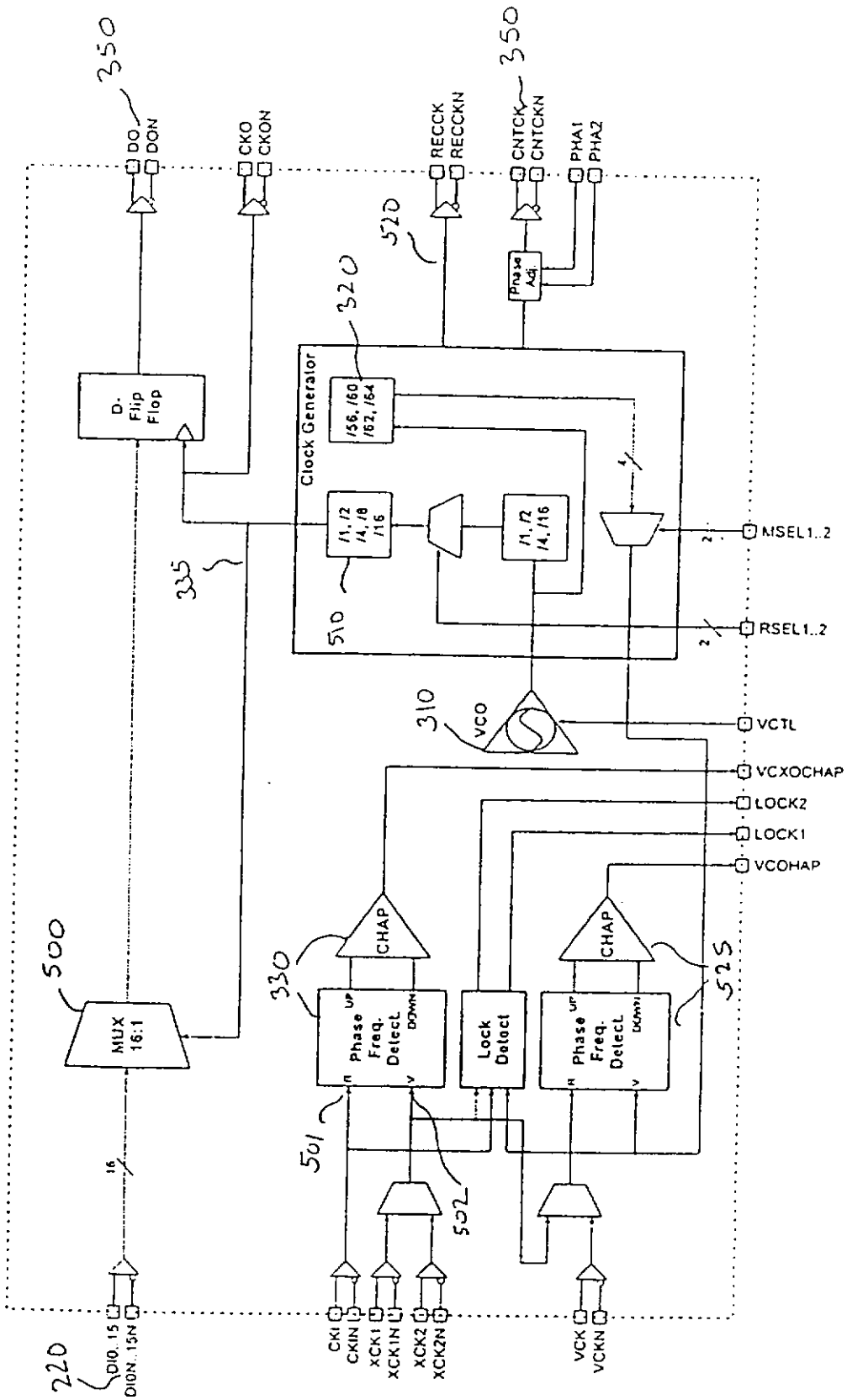

350
DO
DON
CKO
CKON
RECCK
RECCKN
350
CNTCK
CNTCKN
PHA1
PHA2
520
Phase Adj.
320
Clock Generator
D-Flip Flop
/56, /60 /62, /64
/1, /2 /4, /8 /16
/1, /2 /4, /16
MSEL1..2
RSEL1..2
335
510
310
VCO
VCTL
VCXOCHAP
LOCK2
LOCK1
VCOHAP
CHAP
CHAP
500
330
525
MUX 16:1
Phase Freq. Detect
Lock Detect
Phase Freq. Detect
501
502
16
DIO..15
DION..15N
220
CKI
CKIN
XCK1
XCK1N
XCK2
XCK2N
VCK
VCKN

Fig. 3