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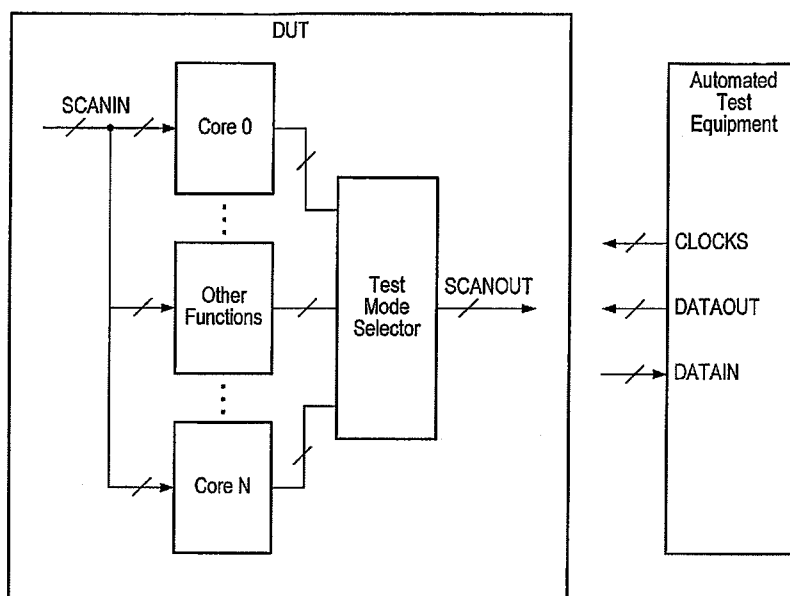
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(54) Title: SIMULTANEOUS CORE TESTING IN MULTI-CORE INTEGRATED CIRCUITS



(57) Abstract: Various embodiments of methods and systems for simultaneously testing multiple cores included in an integrated circuit are disclosed. In one embodiment, an integrated circuit may include two or more logic cores. The IC may also include structural scan test hardware coupled to the cores. This structural scan test hardware may be capable of inputting scan test vector data into scan registers associated with each of the logic cores, simultaneously executing a scan test on the logic cores included in the IC, and outputting the results of the scan tests for multiple cores to automated test equipment (ATE) simultaneously. In one embodiment, elements of the results of testing for multiple cores may be interleaved on a single output line such that an element of test result data from each core is present on an input channel to the ATE during each strobe window.