

**CIRCUIT BOARD ASSEMBLY WITH
REDUCED CAPACITIVE COUPLING**

FIELD

5 The circuit board assembly disclosed herein relates generally to printed circuit board (PCB) technology, and more specifically to substrate configurations that minimize capacitive coupling on signal paths.

BACKGROUND

10 Modern printed circuit board technology typically employs a multi-layered approach to efficiently distribute large groups of signal paths. For example, and referring to Figure 1, an electronic assembly 10 often includes a flip-chip bonded semiconductor device 12 mounted within a ball grid array (BGA) package 14 that in-
15 turn, interfaces with a PCB assembly 16. While different in size and scale, both the package and the PCB assembly employ multi-layer circuit board technology.

 Multi-layer circuit boards, whether large PCBs or small micro-boards, typically utilize a plurality of stacked layers 20 for efficient signal routing. The layers 20, as shown in Figure 2A, each generally include a flat dielectric substrate 22 and a thin conductor 24. The conductor provides a ground/power plane, and is often
20 deposited on the substrate. The layers are laminated in a stacked arrangement with relative precision to preserve strict planarity specifications. Vias 26 formed transverse to the substrate and conductor portion enable layer-to-layer signal routing. The vias are electrically isolated from the conductive plane by a dielectric-filled and metallization-free area known generally as an anti-pad 28.

25 Typically, the entire structure is fabricated according to design rules appropriate for the specific process. Deviating from the standard design rules for a given process often results in additional cost, and/or unexpected problems. One design rule governing the formation of anti-pads constrains the diameter of the anti-pad in an effort to minimize sagging, or non-planarity in the area of the anti-pad
30 (illustrated in phantom in Figure 2B). We have found that enlarging the anti-pads enhances performance for high speed signals. Unfortunately, to do this conventionally by customizing the design outside of the conventional design rules would add undue cost.

What is needed and as yet unavailable is a circuit board structure that allows for the expansion of anti-pads without violating standard fabrication design rules. The circuit board structure described herein satisfies this need.

SUMMARY

The circuit board structure described herein provides a unique way to enlarge anti-pad structures with minimal effects on overall board planarity. This allows for a significant reduction in capacitive coupling between signal paths and power/ground planes. As a result, optimal signal performance and fidelity is available for high-bandwidth applications.

To realize the foregoing advantages, the circuit board structure in one form comprises a circuit board structure. The structure includes a flat substrate having oppositely disposed planar surfaces and a conductor. The conductor is formed on at least one of the planar surfaces and defines a conductor plane. The structure further includes an oversized-in-diameter anti-pad formed through the substrate layer and the conductor layer. The anti-pad further includes a spacer formed substantially coplanar with the conductor plane.

In another form, the circuit board structure is employed in a multi-layered circuit board assembly for routing a plurality of signal paths. The multi-layered circuit board assembly comprises a plurality of layers, with each layer comprising a flat substrate having oppositely disposed planar surfaces and a conductor formed on at least one of the planar surfaces. The conductor defines a conductor plane. An oversized-in-diameter anti-pad is formed through the substrate and the conductor, and includes a conductive via oriented transverse to the substrate and the conductor layer. The anti-pad further includes a spacer disposed substantially coplanar with the conductor plane.

In yet another form, the circuit board structure is employed in a ball-grid-array package for housing at least one semiconductor device. The package has a contact interface adapted for interfacing to a circuit board, the contact interface comprising an array of solder ball pads disposed across an interface layer. The package further comprises a circuit board assembly coupled to the contact interface, the circuit board assembly including a flat substrate having oppositely disposed planar surfaces and a conductor formed on at least one of the planar surfaces. The conductor defines a conductor plane. An oversized-in-diameter anti-pad is formed through the substrate and the conductor and includes a spacer disposed substantially coplanar with the conductor plane.

In yet another form, a method of manufacturing a circuit board structure is described herein. The method comprises the steps forming a flat substrate having oppositely disposed planar surfaces; establishing an opening through the substrate

- transverse to the planar surfaces; filling the opening with a dielectric to form an anti-pad having an outer diameter; depositing a conductor on the substrate to form a conductor plane; and removing portions of the conductor to expose the anti-pad, the removing step further including forming electrically isolated spacers coplanar with the
- 5 conductor plane within the anti pad outer diameter.

Other features and advantages of the present invention will be apparent from the following detailed description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The circuit board structure described herein will be better understood by reference to the following more detailed description and accompanying drawings in which

5 FIG. 1 is a high level diagram, not to scale, of a ball-grid-array package mounted to a printed circuit board assembly;

 FIG. 2A is a partial transverse view of a conventional circuit board layer;

 FIG. 2B is a view similar to Figure 2A, and illustrates the non-planar sagging associated with conventional anti-pads having overly expanded diameters;

10 FIG. 3 is a partial transverse view of an improved circuit board structure;

 FIG. 4 is a flow chart illustrating a method of manufacturing the circuit board structure of Figure 3;

 FIG. 5 is a partial perspective view of a circuit board structure of Figure 3 applied to a printed circuit board having signal vias; and

15 FIG. 6 is a partial perspective view of a circuit board structure of Figure 3 applied to a BGA package scheme with solder ball pads.

DETAILED DESCRIPTION

The circuit board structure described herein provides a high performance solution for minimizing capacitive coupling acting on a signal path due to undesirably small anti-pad diameters. This is accomplished by employing a spacer in the anti-pad
5 such that an expanded diameter may be realized with minimal deviations to overall planarity due to sag.

Referring now to Figure 3, an improved circuit board structure, generally designated 30, comprises a substrate layer 32 and a conductor layer 34 deposited on the substrate. The substrate preferably takes the form of a dielectric material, such as
10 FR-4, or _____, for example. Copper foil provides an acceptable conductor layer. A cylindrical area free of metallization and filled with a dielectric is formed transverse to the substrate layer and conductor layer to define an anti-pad 36. The anti-pad diameter is oversized with respect to predefined process design rules.

For the general structure described above, design rules would typically
15 constrain the size of the anti-pad. We have discovered several applications where an enlarged anti-pad provides enhanced signal propagation performance. We have also discovered a way to minimize sag while expanding the effective diameter of the anti-pad to enable our high-performance objectives.

To do this, and further referring to Figure 3, the anti-pad 36 is supplemented
20 with an electrically isolated spacer 38. The spacer preferably takes the form of a ring, or a plurality of concentric rings (not shown) disposed at one axial end of the anti-pad, substantially coplanar with the conductor layer 34, and fabricated out of a similar electrically conductive material as that of the conductor layer. A dielectric fills in any gaps associated with the spacer and its positioning with respect to the conductive layer
25 such that a flat planar surface is maintained.

Manufacturing the structure is a straightforward process that differs little from conventional practices. Generally, as shown in Figure 4, a suitable substrate is first formed, at step 50. An opening is then established through the substrate, at step 52, by a mechanical drilling process to define the anti-pad opening. The opening is then
30 filled with dielectric, at step 54. The metallization or conductive layer is then deposited, at step 56, then etched, at step 58, using a masking process at the locations corresponding to the anti-pads. During this step, the isolated spacers are defined. Additional dielectric is then applied, at step 60, to fill the anti-pad, thereby completing the general circuit board structure. Further steps in the basic method may be

performed, such as via formation, depending on the application. The process may be repeated several times, depending on the number of layers desired.

In operation, the spacer 38 provides a rigid structure to cooperate with the dielectric and prevent sagging of the oversized-in-diameter anti-pad 36. However, since the spacer comprises a conductive material matching that of the conductor layer, the design rule diameter is satisfied by the diameter dimension "d" (Figure 3), while the effective diameter for high-performance purposes, defined by the dimension "D", is maximized.

One specific application for the basic structure described above is employed for multiple layers in chip/multi-chip modules (MCM), or printed circuit boards (PCBs). Figure 5 illustrates the application, where a conductive via 70 is formed through the anti-pad defined by the opening at 72, and electrically isolated from both the conductor layer 74 and a plurality of concentric spacers 76 and 78. Under conventional design rules, the ratio of the anti-pad diameter to the via diameter is approximately three (3). As explained above, one of the primary purposes of this constraint is to minimize sagging (from an enlarged anti-pad) which would lead to layer-to-layer planarity problems. However, while the close proximity of the via 70 to the anti-pad 72 helps reduce sagging, it also contributes to parasitic capacitive coupling, which degrades signal performance.

We have discovered that by enlarging the anti-pad diameter, and employing the spacer structure described above, parasitic capacitance acting on the signal via 70 coupled from the conductor layer 74 (power or ground plane) is greatly reduced. Moreover, by making the ratio of the anti-pad diameter versus via diameter within the range of five (5) to eight (8), the impedance of the via structure approaches fifty (50) ohms, which is highly desirable.

Figure 6 illustrates an additional application for the general circuit board structure described above involving ball-grid-array (BGA) interface connections. BGA and microBGA packages allow for efficient electrical connections between packaged semiconductor devices and PCBs. The package includes solder ball pads that couple to a BGA-packaged circuit board 82 through a plurality of solder balls 84 that are precisely registered with oppositely confronting solder ball pads 86 disposed on a supporting PCB assembly 88. Both the BGA-packaged circuit board and the PCB assembly have respective power/ground planes 90 and 92.

One of the problems faced by the conventional BGA interface scheme involves a parasitic parallel plate capacitance between the solder ball pad 80 and an

adjacent power/ground plane 82. The problem may manifest itself both at the BGA-packaged circuit board and the PCB assembly 88.

We have discovered that by employing the circuit board structure described above, the parallel plate capacitance between the solder ball pads 80, 86 and the
5 respective power/ground planes 90 and 92 for both the BGA package and the PCB can be minimized. This is done by forming anti-pads proximate the solder ball pad locations at 94 and 96, thereby removing one side of the parallel plate capacitor. To minimize any sagging in the anti-pad, ring-shaped spacers 100 similar to those described in the previous examples are employed. As a result, signals propagating
10 through the BGA package and out through the PCB retain high fidelity.

At a higher level, the circuit board structure disclosed herein optimally enhances signal fidelity at several levels of routing. An electronic assembly comprising an MCM/BGA package interface (such as that in Figure 5) mounted to a printed circuit board (such as that in Figure 4) achieves optimal performance by
15 consistently employing the anti-pad spacer configuration throughout the assembly. The overall assembly is shown generally by the illustration in Figure 1.

Those skilled in the art will recognize the many benefits and advantages afforded by the circuit board structure described herein. Of significant importance is the use of enlarged anti-pads to minimize parasitic capacitance acting on signals
20 propagating through the circuit board structure. The anti-pads are complemented by unique spacers that help to maintain planarity where the oversized antipads are employed.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art
25 that various changes in form and detail may be made therein without departing from the spirit and scope of the invention. For instance, while specific applications concerning printed circuit boards and BGA packaging schemes have been described in detail, the board structure described herein may be advantageously applied to any form of layered circuit board structure, whether at the macro or micro level.

30 Further, while preferred spacer configurations have been described herein, a wide variety of shapes and materials may be employed to provide the benefits and advantages discussed above. For example, spacers taking the form of non-circular shapes, non-continuous shapes, and the like may be used with acceptable results. Additionally, the spacers may be formed of a rigid dielectric rather than a conductive
35 material.

WHAT IS CLAIMED IS:

1. A circuit board structure, the structure comprising:
a flat substrate having oppositely disposed planar surfaces;
a conductor formed on at least one of the planar surfaces, the conductor
layer defining a conductor plane;
5 an oversized-in-diameter anti-pad formed through the substrate and the
conductor, the anti-pad further formed with a spacer disposed substantially coplanar
with the conductor plane.
2. A circuit board structure according to claim 1 wherein:
the spacer is electrically isolated from the conductor.
3. A circuit board structure according to claim 1 wherein:
the spacer comprises the same material as the conductor.
4. A circuit board structure according to claim 1 wherein the spacer
comprises a dielectric.
5. A circuit board structure according to claim 1 and further comprising:
a conductive via formed in the anti-pad, the via oriented transverse to
the substrate and the conductor.
6. A circuit board structure according to claim 5 wherein:
the spacer is coaxially interposed between the via and the conductor.
7. A circuit board structure according to claim 6 wherein:
the spacer is electrically isolated from the via and the conductor.
8. A circuit board structure according to claim 1 wherein the spacer
comprises:
a ring.

9. A circuit board structure according to claim 1 wherein the spacer comprises:
a plurality of concentric spaced-apart rings.
10. A circuit board structure according to claim 1 wherein:
the substrate is further formed with a conductive pad, the conductive ball pad coupled to a signal path, the signal path routed through the substrate.
11. A circuit board structure according to claim 10 wherein the conductive pad comprises a solder ball pad.
12. A multi-layered circuit board assembly for routing a plurality of signal paths, the multi-layered circuit board assembly comprising a plurality of layers, each layer comprising:
a flat substrate having oppositely disposed planar surfaces;
5 a conductor formed on at least one of the planar surfaces, the conductor layer defining a conductor plane;
an oversized-in-diameter anti-pad formed through the substrate and the conductor, the anti-pad further including a conductive via oriented transverse to the substrate and the conductor; and
10 a spacer formed in the anti-pad, the spacer disposed substantially coplanar with the conductor plane.
13. A multi-layered circuit board assembly according to claim 12 wherein:
the spacer is electrically isolated from the conductor.
14. A multi-layered circuit board assembly according to claim 12 wherein:
the spacer comprises the same material as the conductor.
15. A multi-layered circuit board assembly according to claim 12 wherein
the spacer comprises a dielectric.
16. A multi-layered circuit board assembly according to claim 12 wherein:
the spacer is coaxially interposed between the via and the conductor.

17. A multi-layered circuit board assembly according to claim 12 wherein:
the spacer is electrically isolated from the via and the conductor.
18. A multi-layered circuit board assembly according to claim 12 wherein
the spacer comprises:
a ring.
19. A multi-layered circuit board assembly according to claim 12 wherein
the spacer comprises:
a plurality of concentric spaced-apart rings.
20. A ball-grid-array package for housing at least one semiconductor
device, the package having a contact interface adapted for interfacing to a multi-
layered circuit board assembly, the contact interface comprising an array of solder ball
pads disposed across an interface layer, the package further comprising a circuit board
5 structure coupled to the contact interface, the circuit board structure comprising
a flat substrate having oppositely disposed planar surfaces;
a conductor formed on at least one of the planar surfaces, the conductor
layer defining a conductor plane;
an oversized-in-diameter anti-pad formed through the substrate and the
10 conductor; and
a spacer formed in the anti-pad, the spacer disposed substantially
coplanar with the conductor.
21. A ball-grid-array package according to claim 20 wherein:
the spacer is electrically isolated from the conductor.
22. A ball-grid-array package according to claim 20 wherein:
the spacer comprises the same material as the conductor.
23. A ball-grid-array package according to claim 20 wherein the spacer
comprises a dielectric.

24. A ball-grid-array package according to claim 20 wherein the spacer comprises:

a ring.

25. A ball-grid-array package according to claim 20 wherein the spacer comprises:

a plurality of concentric spaced-apart rings.

26. An electronic assembly comprising:

a multi-layered circuit board assembly for routing a plurality of signal paths, the multi-layered circuit board assembly comprising a plurality of layers, each layer comprising:

5 a flat substrate having oppositely disposed planar surfaces;

a conductor formed on at least one of the planar surfaces, the conductor layer defining a conductor plane;

10 an oversized-in-diameter anti-pad formed through the substrate and the conductor, the anti-pad further including a conductive via oriented transverse to the substrate and the conductor;

a spacer formed in the anti-pad, the spacer disposed substantially coplanar with the conductor plane; and

15 a ball-grid-array package for housing at least one semiconductor device, the package having a contact interface coupled to the multi-layered circuit board assembly, the contact interface comprising an array of solder ball pads disposed across an interface layer, the package further comprising a circuit board structure coupled to the contact interface, the circuit board structure comprising

a flat substrate having oppositely disposed planar surfaces;

20 a conductor formed on at least one of the planar surfaces, the conductor layer defining a conductor plane;

an oversized-in-diameter anti-pad formed through the substrate and the conductor; and

a spacer formed in the anti-pad, the spacer disposed substantially coplanar with the conductor.

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27. A method of minimizing parasitic capacitance in a circuit board structure, the circuit board structure having a flat substrate and a planar conductor formed on the substrate, the method comprising the steps:

- 5 providing a signal path proximate an anti-pad, the anti-pad formed into the substrate and conductor and comprising a spacer formed substantially co-planar with the conductor; and
routing a signal along the signal path.

28. A method according to claim 27 wherein the anti-pad is formed with a signal via, and the signal is routed along the signal via.

29. A method according to claim 27 wherein the anti-pad is formed proximate a solder ball pad, and the signal is routed through the solder ball pad.

30. A method of manufacturing a circuit board structure, the method comprising the steps:

- 5 forming a flat substrate having oppositely disposed planar surfaces;
establishing an opening through the substrate transverse to the planar surfaces;
filling the opening with a dielectric to form an anti-pad having an outer diameter;
depositing a conductor on the substrate to form a conductor plane; and
removing portions of the conductor to expose the anti-pad, the
10 removing step further including forming electrically isolated spacers coplanar with the conductor plane within the anti pad outer diameter.