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(21) International Application Number: PCT/US99/30719 (22) International Filing Date: 21 December 1999 (21.12.99) (30) Priority Data: 09/226,965 8 January 1999 (08.01.99) US (71) Applicant (for all designated States except US): INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US). (72) Inventors; and (75) Inventors/Applicants (for US only): CLOHSET, Steve, J. [US/US]; 2816 Regina Way, Sacramento, CA 95818 (US). DIEP, Trung, A. [US/US]; 103 Mannock Court, Folsom, CA 95630 (US). GANDHI, Wishwesh [IN/US]; 406 Canyon Terrace, Folsom, CA 95630 (US). PIAZZA, Thomas, A. [US/US]; 5046 Chelshire Downs Road, Granite Bay, CA 95746 (US). SREENIVAS, Aditya [IN/US]; 4215 Flushing Place, El Dorado Hills, CA 95762 (US). TRIEU, Tuong, P. [US/US]; 119 Demurrage Way, Folsom, CA 95630 (US). (74) Agents: MILLIKEN, Darren, J. et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 12400 Wilshire Boulevard, 7th Floor, Los Angeles, CA 90025 (US).			(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG). Published Without international search report and to be republished upon receipt of that report.

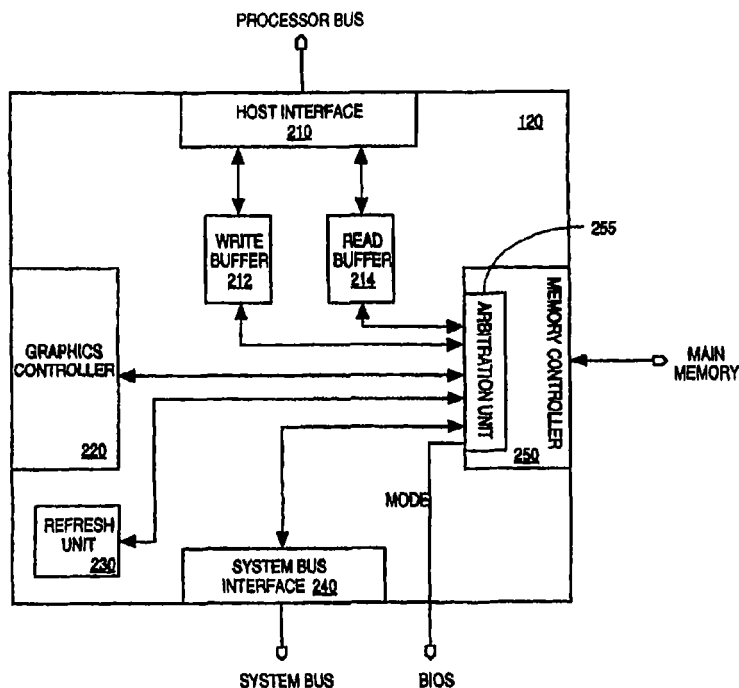


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(54) Title: METHOD AND APPARATUS FOR ARBITRATION IN A UNIFIED MEMORY ARCHITECTURE

(57) Abstract

According to one embodiment, a computer system is disclosed that includes a memory and a memory controller coupled to the memory. The memory controller includes an arbitration unit that may be programmed to operate according to a first arbitration mode or a second arbitration mode. The computer system also includes a first device and a second device coupled to the arbitration unit. According to a further embodiment, the first device is assigned a higher priority classification than the second device for accessing the memory while the arbitration unit is operating according to the first arbitration mode. In addition, the first device and the second device are assigned equal priority classifications for accessing the memory while the arbitration unit is operating according to the second arbitration mode.



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