CLAIMS

1. A word-line drive circuit, comprising:

at least two sub word-line drivers (SWD), each of the SWDs being connected to a main word line (MWL) for providing an enable signal and a sub word line, wherein

each of the SWDs comprises a holding transistor, a first end and a second end of the holding transistor are respectively connected to different sub word lines, and a gate of the holding transistor receives a second drive signal; and

each of the SWDs is configured to provide a first drive signal to a selected sub word line in response to the first drive signal and the enable signal, the selected sub word line being a sub word line connected to the first end or the second end of the holding transistor, and conduct the first end and the second end of the holding transistor in response to the first drive signal, the enable signal and the second drive signal;

wherein the same MWL is connected to at least two SWDs, the same MWL corresponding to at least two sub word lines, and the two sub word lines connected to the first end and the second end respectively correspond to the same MWL.

2. The word-line drive circuit according to claim 1, wherein at least two MWL drivers are respectively connected to different MWLs, different MWLs corresponding to different sub word lines, and the two sub word lines connected to the first end and the second end respectively correspond to different MWLs.

3. The word-line drive circuit according to any one of claims 1 to 2, wherein the holding transistor comprises an N-type Metal Oxide Semiconductor (NMOS) transistor.

4. The word-line drive circuit according to any one of claims 1 to 3, wherein each of the SWDs comprises:

a pull-up transistor, comprising a gate connected to the MWL, a source receiving the first drive signal, and a drain connected to the sub word line and the first end or the second end of the holding transistor; and

a pull-down transistor, comprising a gate connected to the MWL, a drain connected to the drain of the pull-up transistor, and a source receiving a third drive signal.

5. The word-line drive circuit according to claim 4, wherein the pull-up transistor comprises a P-type Metal Oxide Semiconductor (PMOS) transistor, and the pull-down transistor comprises an NMOS transistor.

6. A word-line driver, comprising:

a P-type Metal Oxide Semiconductor (PMOS) area, comprising multiple first active areas extending along a first direction, each first active area comprising a first channel area and a first source area and a first drain area respectively located at two opposite sides of the first channel area;

an N-type Metal Oxide Semiconductor (NMOS) area arranged along a second direction with the PMOS area and comprising multiple second active areas extending along the first direction, each second active area comprising a second channel area and a second source area and a second drain area respectively located at two opposite sides of the second channel area, the second active area further comprising a third channel area and a third source area and a third drain area respectively located at two opposite sides of the third channel area;

first gates, each of the first gates extending along the second direction and covering the

multiple first channel areas and the multiple second channel areas, the first gate being electrically connected to a main word line (MWL), the first gates, the first source areas and the first drain areas constituting pull-up transistors, and the first gates, the second source areas and the second drain areas constituting pull-down transistors; and

multiple second gates, each of the second gates covering a corresponding third channel area, the second gates, the third source areas and the third drain areas constituting holding transistors,

wherein a first drain area of one of the pull-up transistors is electrically connected to a second drain area of one of the pull-down transistors, and is electrically connected to a corresponding sub word line; and

a third drain area of the same holding transistor is electrically connected to the second drain area of one of the pull-down transistors, and a third source area is electrically connected to a second drain area of another pull-down transistor;

wherein each of the first gates comprises:

at least two extending portions spaced apart in the first direction, the extending portions extending along the second direction and covering the multiple first channel areas and the multiple second channel areas; and

connection portions, connecting the extending portions arranged adjacently in the first direction.

7. The word-line driver according to claim 6, wherein the connection portions cover an area between the adjacent first active areas and further cover an area between the first active area and the second active area.

8. The word-line driver according to claim 6, wherein a distance between adjacent extension

portions of the NMOS area is greater than a distance between adjacent extension portions of part of the PMOS area in the first direction, and each second gate is located between the adjacent extension portions.

9. The word-line driver according to claim 8, wherein the PMOS area comprises:

a first PMOS area and a second PMOS area arranged along the second direction, the second PMOS area being located between the first PMOS area and the NMOS area,

wherein two extension portions of the same first gate cover the same first active area of the first PMOS area, and the two extension portions further respectively cover two first active areas of the second PMOS area which are arranged along the first direction; and

a distance between adjacent extension portions of the first PMOS area is less than a distance between adjacent extension portions of the second PMOS area in the first direction.

10. The word-line driver according to claim 6, wherein a distance between adjacent extension portions of the NMOS area is less than a distance between adjacent extension portions of part of the PMOS area in the first direction, and each second gate is located outside an area surrounded by two of the extension portions.

11. The word-line driver according to claim 9, wherein the PMOS area comprises:

a first PMOS area and a second PMOS area arranged along the second direction, the second PMOS area being located between the first PMOS area and the NMOS area,

wherein the two extension portions of the same first gate cover the same first active area of the second PMOS area, and the two extension portions further respectively cover two first active areas of the first PMOS area which are arranged along the first direction; and

a distance between the adjacent extension portions of the first PMOS area is greater than a distance between the adjacent extension portions of the second PMOS area in the first direction.

12. The word-line driver according to claim 6, wherein the third channel area and at least one of the second channel areas belong to the same second active area.

13. The word-line driver according to claim 12, wherein a second drain area of one of the pull-down transistors corresponding to the same first gate is shared with a third drain area of a holding transistor, and a second drain area of another pull-down transistor corresponding to the same first gate is shared with a third source area of the holding transistor.

14. The word-line driver according to claim 12, wherein a second drain area of one of the pull-down transistors corresponding to one of the first gates is shared with a third drain area of a holding transistor, and a second drain area of one of the pull-down transistors corresponding to another first gate is shared with a third source area of the holding transistor.

15. The word-line driver according to claim 6, wherein each of the first gates covers 4×N first channel areas and 4×N second channel areas, and the pull-up transistors and the pull-down transistors constituted by each of the first gates are electrically connected to 2×N holding transistors, N being a positive integer greater than or equal to 1.

16. The word-line driver according to claim 6, wherein the multiple first active areas comprise: at least two first active areas arranged close to the NMOS area, two of the first active areas are spaced apart along the first direction and have a spaced area, and the second gate directly faces the spaced

area in the second direction.

17. A storage device, comprising:

a storage unit array comprising multiple storage units connected to multiple sub word lines and multiple bit lines; and

the word-line drive circuit according to any one of claims 1 to 5, or the word-line driver according to any one of claims 6 to 16.