

A FREQUENCY DIVIDER

Field

5 The invention relates to a frequency divider.

Background to the Invention

Many signal processing systems require multiple clocks to process, for
10 example, high and low frequency signals. To avoid having multiple clocks, frequency dividers are used to divide high frequency clock signals to lower frequency clock signals. There is a need for an alternative frequency divider.

Summary of the Invention

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In a first aspect, there is provided a frequency divider, comprising:

- a clock input adapted to receive a clock signal;
- a reset input adapted to receive a reset signal;
- a division circuit adapted to divide the clock signal by a factor to
20 produce an output signal;
- an output adapted to output the output signal,
- a clock disable circuit connected to the reset input and the clock input, the clock disable circuit being controlled by the reset signal to disable the clock signal to the division circuit; and
- 25 a setting circuit connected to the reset input and the output, the setting circuit being controlled by the reset signal to set the output signal to a designated state.

In an embodiment, the reset input is adapted to receive a reset signal and an
30 inverted reset signal;

- the clock disable circuit is controlled by the reset signal together with the inverted reset signal to disable the clock signal to the division circuit; and
- the setting circuit is controlled by the reset signal together with the inverted reset signal to set the output signal to a designated state.

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In an embodiment, the division circuit is adapted to produce an output signal and an inverted output signal;

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the output is adapted to output the output signal and the inverted output signal; and

the setting circuit is controlled by the reset signal together with the inverted reset signal to set the output signal to a designated state and the
5 inverted output signal to a another designated state.

In an embodiment, the clock input is adapted to receive a clock signal and an inverted clock signal;

the division circuit is adapted to receive the clock signal and the
10 inverted output signal; and

the clock disable circuit is adapted to disable the clock signal and the inverted clock signal.

In an embodiment, the setting circuit comprises

15 a first transistor adapted to receive the inverted reset signal to set the inverted output signal; and

a second transistor adapted to receive the reset signal to set the output signal.

20 In an embodiment, the second transistor is complementary to the first transistor.

In an embodiment, the first transistor is a N-channel Metal Oxide Semiconductor Field Effect Transistor (NMOS) and the second transistor is a
25 P-channel Metal Oxide Semiconductor Field Effect Transistor (PMOS).

In an embodiment, the division circuit further comprises a first latch circuit adapted to receive the clock signal and a second latch circuit adapted to receive the inverted clock signal, the first latch circuit being connected to the
30 second latch circuit in a master/slave configuration.

In an embodiment, the clock disable circuit comprises

a first clock disengage circuit for disengaging the clock signal from the first latch circuit; and

35 a first discharge circuit for discharging residual charges from the first latch circuit.

In an embodiment, the clock disable circuit further comprises
a second clock disengage circuit for disengaging the inverted clock
signal from the second latch circuit; and
a second discharge circuit for discharging residual charges from the
5 second latch circuit.

In an embodiment, the first clock disengage circuit comprises
a third transistor adapted to receive the reset signal;
a fourth transistor adapted to receive the inverted reset signal; and
10 a fifth transistor connected to the third and fourth transistors, the fifth
transistor being driven by the third and fourth transistors to disengage the
clock signal from the first latch circuit.

In an embodiment, the second clock disengage circuit comprises
15 a sixth transistor adapted to receive the reset signal;
a seventh transistor adapted to receive the inverted reset signal; and
an eighth transistor connected to the sixth and seventh transistor, the
eighth transistor being driven by the sixth and seventh transistors to
disengage the inverted clock signal from the second latch circuit.

20 In an embodiment, the fourth transistor is complementary to the third and fifth
transistors.

In an embodiment, the third transistor is a N-channel Metal Oxide
25 Semiconductor Field Effect Transistor (NMOS), the fourth transistor is a P-
channel Metal Oxide Semiconductor Field Effect Transistor (PMOS), and the
fifth transistor is a N-channel Metal Oxide Semiconductor Field Effect
Transistor (NMOS).

30 In an embodiment, the seventh transistor is complementary to the sixth and
eighth transistors.

In an embodiment, the sixth transistor is a N-channel Metal Oxide
Semiconductor Field Effect Transistor (NMOS), the seventh transistor is a P-
35 channel Metal Oxide Semiconductor Field Effect Transistor (PMOS), and the
eighth transistor is a N-channel Metal Oxide Semiconductor Field Effect
Transistor (NMOS).

In an embodiment, the first discharge circuit comprises a ninth transistor controlled by the reset signal for discharging residual charges from the first latch circuit.

- 5 In an embodiment, the second discharge circuit comprises an tenth transistor controlled by the inverted reset signal for discharging residual charges from the second latch circuit.

- 10 In an embodiment, the ninth transistor is a N-channel Metal Oxide Semiconductor Field Effect Transistor (NMOS).

In an embodiment, the tenth transistor is a P-channel Metal Oxide Semiconductor Field Effect Transistor (PMOS).

- 15 In an embodiment, the reset input is adapted to receive differential input signals; and the output is adapted to output differential signals.

Brief Description of the Drawings

- 20 Embodiments, incorporating one or more of the aspects of the invention, will now be described by way of example with reference to the accompanying drawings in which:

- Figure 1 is a circuit diagram of a frequency divider according to an
25 embodiment of the invention;

Figure 2 is a more detailed circuit diagram of the frequency divider of Figure 1, illustrating a division circuit and a clock disable circuit;

- 30 Figure 3 is a partial circuit diagram of the clock disable circuit of Figures 1 and 2, illustrating a first clock disengage circuit and a first discharge circuit;

- Figure 4 is a partial circuit diagram of the clock disable circuit of Figures 1 and 2, illustrating a second clock disengage circuit and a second discharge
35 circuit;

Figure 5 is a circuit diagram of the latch circuit of Figure 1;

Figure 6 is a circuit diagram of the latch circuit according to an alternative embodiment of the invention; and

Figure 7 is a schematic view of an alternative embodiment of the invention.

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Description of Exemplary Embodiments

Referring to Figure 1, there is shown a frequency divider 900 comprising a reset input adapted to receive a reset signal RST and an inverted reset
10 signal RST', a clock input adapted to receive a clock signal CLK and an inverted clock signal CLK', and an output adapted to output an output signal OUTPUT and an inverted output signal OUTPUT'.

Persons skilled in the art will appreciate that the inverted signals RST', CLK',
15 OUTPUT' can be generated relatively simply using inverters or other suitable components as part of the frequency divider. Thus, in an alternative frequency divider embodiment, the reset and clock inputs are adapted to receive only the reset signal and the clock signal, and the output is adapted to output only the output signal.

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In Figure 1, the illustrated frequency divider 900 is a differential circuit; that is, the reset input is adapted to receive differential input signals and the output is adapted to output differential output signals. It is however envisaged that a frequency divider in an alternative embodiment may not be
25 a differential circuit.

The frequency divider further comprises two circuits 30, 40 connected to each other. Each circuit 30 or 40 comprises an input adapted to receive a D input signal and an inverted D input signal, and an output adapted to output
30 a Q output signal and an inverted Q output signal.

In addition, the first circuit 30 is adapted to receive the clock signal CLK and the reset signals RST, RST', and the second circuit 40 is adapted to receive the inverted clock signal CLK' and the reset signals RST, RST'.

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The two circuits 30 and 40 are arranged in a master/slave configuration whereby the Q output signals of the first circuit 30 are received as the D input

signals of the second circuit 40, and the Q output signals of the second circuit 40 are feedback as the D input signals to the first circuit 30.

Accordingly, herein the first circuit 30 is sometimes referred to as the master circuit and the second circuit 40 is sometimes referred to as the slave circuit. In this master/slave configuration, when the Q output signal of the master circuit 30 is in one state (for example, HIGH state), the Q output signal of the slave circuit 40 will be in the complement state (for example, LOW state).

The first and second circuits 30 and 40 together form a division circuit and a clock disable circuit. The role of the division circuit is to process the clock signal CLK and the inverted clock signal CLK' to produce two divided signals: the output signal OUTPUT and the inverted output signal OUTPUT'. The role of the clock disable circuit is to act as gate switch to the division circuit, so that the reset signal RST and the inverted reset signal RST' can disable the clock signal CLK and the inverted clock signal CLK' to the division circuit.

In addition to the two circuits 30, 40, the frequency divider further comprises a setting circuit comprising two transistors 10, 20. The first transistor 10 is adapted to receive the inverted reset signal RST' and the second transistor 20 is adapted to receive the reset signal RST.

The setting circuit is configured to allow the reset signal RST and the inverted reset signal RST' to set the output signal OUTPUT to a designated state and to set the inverted output signal OUTPUT' to a state complementary to the designated state.

In this embodiment, the first and second transistors 10, 20 are complementary to each other and are implemented using Complementary Metal Oxide Semiconductor (CMOS) technology; the first transistor is a N-channel Metal Oxide Semiconductor Field Effect Transistor (NMOS) and the second transistor is a P-channel Metal Oxide Semiconductor Field Effect Transistor (PMOS). However, besides using CMOS technology, it is envisaged that the setting circuit can be implemented using other complementary transistor technologies or using logic gates.

The frequency divider 900 is capable of operating in two modes: In the first

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mode, the division circuit divides the clock signal CLK by a factor (in the illustrated example, the factor is two) to produce the output signal OUTPUT. In the second mode, the output signal OUTPUT is set by the setting circuit to a designated state and the clock disable circuit disables the clock signal
5 OUTPUT to the division circuit.

In practice, the first mode represents the division mode of operation of a frequency divider - which is to divide high frequency clock signals to lower frequency clock signals (persons skilled in the art will recognize that the
10 illustrated first mode is a divide-by-2 operation) – and the second mode represents a mode of operation whereby the frequency divider is set or reset to a designated state.

It will be appreciated by persons skilled in the art that the second mode is
15 advantageous in many situations; for example, when a data signal arrives, the frequency divider can be set or reset to align the phase of the data signal to the clock signal or the divided signal.

Figure 2 is a more detailed circuit diagram of the first and second circuits 30,
20 40 of Figure 1, illustrating in greater detail a division circuit and a clock disable circuit.

The division circuit comprises a first latch circuit 50 and a second latch circuit 60. Both latch circuits 50, 60 are connected to the clock disable circuit 70
25 comprising a first clock disengage circuit 80, a first discharge circuit 100, a second clock disengage circuit 90, and a second discharge circuit 110.

The first clock disengage circuit 80 is adapted to receive the clock signal CLK, the reset signal RST and the inverted reset signal RST'. This first clock
30 disengage circuit 80 acts as a gate circuit for the first latch circuit 50 in the sense that it is adapted to pass the clock signal CLK to the first latch circuit 50 in the first mode and also to disengage the first latch circuit 50 from the clock signal CLK in the second mode.

35 The second clock disengage circuit 90 is adapted to receive the inverted clock signal CLK', the reset signal RST and the inverted reset signal RST'. It acts as a gate circuit for the second latch circuit 60. In the first mode, the

second clock disengage circuit 90 is adapted to pass the inverted clock signal CLK' to the second latch circuit 60. In the second mode, the second clock disengage circuit 90 disengages the second latch circuit 60 from the inverted clock signal CLK'.

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The first discharge circuit 100 is adapted to receive the reset signal RST. The reset signal RST is used to control the first discharge circuit 100 to discharge residual charges from the first latch circuit 50. In a similar manner, the second discharge circuit 110 is adapted to receive the inverted reset signal RST' and the inverted reset signal RST' is used to control the second discharge circuit 110 to discharge residual charges from the second latch circuit 60.

When operating in the first mode, the clock signal CLK is used to drive the first latch circuit 50 and the inverted clock signal CLK' is used to drive the second latch circuit 60. When in use, the two latch circuits 50, 60 cooperate to perform the division function, each of them changing state at the toggling of the clock signal CLK or the inverted clock signal CLK'.

When operating in the second mode, upon arrival of the reset signal RST, the first clock disengage circuit 80 disengages the clock signal CLK from the first latch circuit 50 and the first discharge circuit 100 discharges residual charges in the first latch circuit 50 and forces the Q output signal of the first latch circuit 50 to a designated state despite the current state of the first latch circuit 50. In an embodiment, this designated state is LOW. Similarly, upon arrival of the inverted reset signal RST', the second clock disengage circuit 90 disengages the inverted clock signal CLK' from the second latch circuit 60 and the second discharge circuit 110 discharges residual charges in the second latch circuit 60 and forces the Q output signal of the second latch circuit 60 to a state complementary to the designated state, despite the current state of the second latch circuit 60.

By disengaging the clock signal CLK and the inverted clock signal CLK', the clock disable circuit 70 performs its function as a pass-gate and cuts off the clock input from influencing the Q output signals of the first and second latch circuits 50, 60.

Figure 3 illustrates on the left a circuit diagram view of a first clock disengage circuit 80 and on the right a circuit diagram of a first discharge circuit 110.

The first clock disengage circuit 80 comprises three transistors; a third transistor 120 adapted to receive the reset signal, a fourth transistor 130 adapted to receive the inverted reset signal, and a fifth transistor 140 connected to the third and fourth transistors 120, 130. This arrangement allows reset signal RST and the inverted reset signal RST' to control respectively the third and fourth transistors 120, 130 to drive the fifth transistor 140 to disengage the clock signal CLK from the first latch circuit 50.

The first discharge circuit 100 comprises only one transistor, a ninth transistor 150 adapted to receive the reset signal RST. This allows the reset signal RST to control the ninth transistor 150 to allow residual charges to discharge from the first latch circuit 50.

The fourth transistor 130 is complementary to the third transistor 120, the fifth transistor 140, and the ninth transistor 150. In this embodiment, the third, fifth and ninth transistors 120, 140, 150 are NMOS transistors and the fourth transistor 130 is a PMOS transistor.

Similar to Figure 3, Figure 4 illustrates on the left a circuit diagram of a second clock disengage circuit 90 and on the right a circuit diagram of a second discharge circuit 110.

The second clock disengage circuit 90 also comprises three transistors and is arranged in a similar manner to the first clock disengage circuit 80. The second clock disengage circuit 90 comprises a sixth transistor 160 adapted to receive the reset signal, a seventh transistor 170 adapted to receive the inverted reset signal, and an eighth transistor 180 connected to the sixth and seventh transistors 160, 170.

As with the first clock disengage circuit 80, the second clock disengage circuit 90 allows the reset signal RST and the inverted reset signal RST' to control respectively the sixth and seventh transistors 160, 170 to drive the eighth transistor 180 to disengage the inverted clock signal CLK' from the

second latch circuit 60.

Similar to the first discharge circuit 100, the second discharge circuit 110 also comprises only one transistor, a tenth transistor 190 controlled by the
5 inverted reset signal RST' to discharge residual charges from the second latch circuit 60.

The seventh and tenth transistors 170, 190 are complementary to the sixth and eighth transistors 160, 180. In this embodiment, the sixth and eighth
10 transistors are NMOS transistors 160, 180, and the seventh and tenth transistors 170, 190 are PMOS transistors.

Although the clock disable circuit 70 shown in this embodiment is implemented using CMOS transistors, it is envisaged that this need not be
15 the case. The clock disable circuit can be implemented using other types of circuitry (such as using other complementary transistor technologies or using logic gates) to force the output signals of the master latch circuit 50 and the slave latch circuit 60 to their designated states.

20 Figure 5 illustrates how a latch circuit 50 or 60 is implemented according to an embodiment of the invention using four CMOS transistors 200, 210, 220, 230. Person skilled in the art will appreciate that this latch circuit is commonly referred to as a D-latch.

25 Figure 6 illustrates how a latch circuit 50 or 60 is implemented according to an alternative embodiment using two CMOS transistors 200, 220 together with two NPN-type Bipolar Junction Transistor (BJT) transistors 215, 235.

Figure 7 is a schematic view of a frequency divider according to an
30 alternative embodiment of the invention.

This alternative frequency divider 300 is an extension of the one described above 900. It is formed by a plurality of frequency dividers described above 900 when cascaded, or connected in series. As will be appreciated by
35 persons skilled in the art, this system is a divide-by- 2^n frequency divider, where n is the number of divide-by-2 frequency divider circuits.

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It will be understood to persons skilled in the art of the invention that many modifications may be made without departing from the spirit and scope of the invention, in particular that various features of the above embodiments can be combined to form further embodiments.

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It is to be understood that any prior art publication referred to herein does not constitute an admission that the publication forms a part of the common general knowledge in any country.

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In the claims which follow and in the preceding description of the invention, except where the context requires otherwise due to express language or necessary implication, the word "comprise" or variations such as "comprises" or "comprising" is used in an inclusive sense, that is to specify the presence of the stated features but not to preclude the presence or addition of further

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features in various embodiments of the invention.

THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:

1. A frequency divider, comprising:
 - a clock input adapted to receive a clock signal;
 - 5 a reset input adapted to receive a reset signal;
 - a division circuit adapted to divide the clock signal by a factor to produce an output signal;
 - an output adapted to output the output signal,
 - a clock disable circuit connected to the reset input and the clock input,
 - 10 the clock disable circuit being controlled by the reset signal to disable the clock signal to the division circuit; and
 - a setting circuit connected to the reset input and the output, the setting circuit being controlled by the reset signal to set the output signal to a designated state.
- 15 2. A frequency divider as claimed in claim 1, wherein
 - the reset input is adapted to receive a reset signal and an inverted reset signal;
 - the clock disable circuit is controlled by the reset signal together with
 - 20 the inverted reset signal to disable the clock signal to the division circuit; and
 - the setting circuit is controlled by the reset signal together with the inverted reset signal to set the output signal to a designated state.
3. A frequency divider as claimed in claim 2, wherein
 - 25 the division circuit is adapted to produce an output signal and an inverted output signal;
 - the output is adapted to output the output signal and the inverted output signal; and
 - the setting circuit is controlled by the reset signal together with the
 - 30 inverted reset signal to set the output signal to a designated state and the inverted output signal to a another designated state.
4. A frequency divider as claimed in claim 3, wherein
 - the clock input is adapted to receive a clock signal and an inverted
 - 35 clock signal;
 - the division circuit is adapted to receive the clock signal and the inverted output signal; and

the clock disable circuit is adapted to disable the clock signal and the inverted clock signal.

- 5 5. A frequency divider as claimed in claims 3 or 4, wherein the setting circuit comprises
 a first transistor adapted to receive the inverted reset signal to set the inverted output signal; and
 a second transistor adapted to receive the reset signal to set the output signal.

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6. A frequency divider as claimed in claim 5, wherein the second transistor is complementary to the first transistor.

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7. A frequency divider as claimed in claims 5 or 6, wherein the first transistor is a N-channel Metal Oxide Semiconductor Field Effect Transistor (NMOS) and the second transistor is a P-channel Metal Oxide Semiconductor Field Effect Transistor (PMOS).

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8. A frequency divider as claimed in claim 4, wherein the division circuit further comprises a first latch circuit adapted to receive the clock signal and a second latch circuit adapted to receive the inverted clock signal, the first latch circuit being connected to the second latch circuit in a master/slave configuration.

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9. A frequency divider as claimed in claim 8, wherein the clock disable circuit comprises
 a first clock disengage circuit for disengaging the clock signal from the first latch circuit; and

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- a first discharge circuit for discharging residual charges from the first latch circuit.

10. A frequency divider as claimed in claim 9, wherein the clock disable circuit further comprises

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- a second clock disengage circuit for disengaging the inverted clock signal from the second latch circuit; and
 a second discharge circuit for discharging residual charges from the second latch circuit.

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11. A frequency divider as claimed in claim 9, wherein the first clock disengage circuit comprises
a third transistor adapted to receive the reset signal;
a fourth transistor adapted to receive the inverted reset signal; and
5 a fifth transistor connected to the third and fourth transistors, the fifth transistor being driven by the third and fourth transistors to disengage the clock signal from the first latch circuit.
12. A frequency divider as claimed in claim 10, wherein the second clock disengage circuit comprises
10 a sixth transistor adapted to receive the reset signal;
a seventh transistor adapted to receive the inverted reset signal; and
an eighth transistor connected to the sixth and seventh transistor, the eighth transistor being driven by the sixth and seventh transistors to
15 disengage the inverted clock signal from the second latch circuit.
13. A frequency divider as claimed in claim 11, wherein the fourth transistor is complementary to the third and fifth transistors.
- 20 14. A frequency divider as claimed in claims 11 or 13, wherein the third transistor is a N-channel Metal Oxide Semiconductor Field Effect Transistor (NMOS), the fourth transistor is a P-channel Metal Oxide Semiconductor Field Effect Transistor (PMOS), and the fifth transistor is a N-channel Metal Oxide Semiconductor Field Effect Transistor (NMOS).
- 25 15. A frequency divider as claimed in claim 12, wherein the seventh transistor is complementary to the sixth and eighth transistors.
16. A frequency divider as claimed in claims 12 or 15, wherein the sixth
30 transistor is a N-channel Metal Oxide Semiconductor Field Effect Transistor (NMOS), the seventh transistor is a P-channel Metal Oxide Semiconductor Field Effect Transistor (PMOS), and the eighth transistor is a N-channel Metal Oxide Semiconductor Field Effect Transistor (NMOS).
- 35 17. A frequency divider as claimed in claim 9, wherein the first discharge circuit comprises a ninth transistor controlled by the reset signal for discharging residual charges from the first latch circuit.

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18. A frequency divider as claimed in claim 10, wherein the second discharge circuit comprises an tenth transistor controlled by the inverted reset signal for discharging residual charges from the second latch circuit.
- 5 19. A frequency divider as claimed in claim 17, wherein the ninth transistor is a N-channel Metal Oxide Semiconductor Field Effect Transistor (NMOS).
- 10 20. A frequency divider as claimed in claim 18, wherein the tenth transistor is a P-channel Metal Oxide Semiconductor Field Effect Transistor (PMOS).
- 15 21. A frequency divider as claimed in any one of the preceding claims, wherein the reset input is adapted to receive differential input signals; and the output is adapted to output differential signals.