MICROELECTRONICS FABRICATION FORMED WITH SPIN-ON PLANARIZING LAYER HAVING A BUCKMINSTERFULLERENE INCORPORATED THEREIN

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to planarizing layers formed within microelectronics fabrications. More particularly, the present invention relates to spin-on planarizing layers formed within microelectronics fabrications.

2. Description of the Related Art

Microelectronics fabrications are formed from microelectronics substrates upon which are formed patterned conductor layers which are separated by dielectric layers. As microelectronics fabrication integration levels have increased, it has become increasingly common to form microelectronics fabrications with substantial surface topography which is desired to be planarized such that additional microelectronics layers formed within a microelectronics fabrication with substantial surface topography may be formed with enhanced microelectronics fabrication manufacturability and reliability.

When fabricating a microelectronics fabrication with substantial surface

topography, it is common in the art of microelectronics fabrication to attempt global planarization of the microelectronics fabrication with a spin-on planarizing material which forms a spin-on planarizing layer upon the microelectronics fabrication. Typical spin-on planarizing materials include but are not limited to spin-on-glass (SOG) materials (such as but not limited to silicate spin-on-glass (SOG) materials and siloxane spin-on-glass (SOG) materials) aerogel spin-on materials, nanogel spin-on materials and spin-on polymer materials (such as but not limited to polyimide polymer materials and cyclotene polymer materials).

While the use of spin-on materials is common in the art of microelectronics fabrication when attempting to planarize microelectronics fabrications having substantial surface topography, the use of spin-on materials when attempting to planarize microelectronics fabrications having substantial surface topography is not entirely without problems within the art of microelectronics fabrication. In particular, while spin-on materials typically do assist in planarizing microelectronics fabrications having substantial surface topography, spin-on materials often typically do not substantially completely planarize microelectronics fabrications having substantial surface topography.

A schematic cross-sectional diagram of such an incompletely planarized microelectronics fabrication having a substantial surface topography is shown in Fig. 1. Shown in Fig. 1 is a substrate 10 employed within a microelectronics fabrication, where the substrate 10 has formed thereupon a series of high step height microelectronics structures 12a, 12b and 12c. Typically, each high step height microelectronics structure 12a, 12b or 12c within the series of high step height microelectronics structures 12a, 12b and 12c has a width upon the substrate of from about 0.2 to about 100 microns, as aspect ratio of from about 1:100 to about 40:1 and a pitch of from about 0.4 to about 200 microns separating it from an adjoining microelectronics

structure 12a, 12b or 12c within the series of high step height microelectronics structures 12a, 12b and 12c. Formed upon the substrate 10 and the series of high step height microelectronics structures 12a, 12b and 12c is a spin-on planarizing layer 14. As is illustrated in Fig. 1, the spin-on planarizing layer 14 is typically formed to a greater height over the high step height microelectronics structures 12a, 12b and 12c than over portions of the substrate 10 other than those over the high step height microelectronics structures 12a, 12b or 12c.

In order to provide a more complete planarization of the spin-on planarizing layer 14 within the microelectronics fabrication whose schematic cross-sectional diagram is illustrated in Fig. 1, there is typically employed an additional planarizing process step such as a reactive ion etch (RIE) etchback planarizing process step employing a reactive ion etch (RIE) etchback planarizing method, or more particularly, a chemical mechanical polish (CMP) planarizing process step employing a chemical mechanical polish (CMP) planarizing method. While reactive ion etch (RIE) etchback planarizing methods and chemical mechanical polish (CMP) planarizing methods do provide from the microelectronics fabrication whose schematic cross-sectional diagram is illustrated in Fig. 1 a more planar spin-on planarizing layer 14 upon which may be formed additional microelectronics layers within the microelectronics fabrication whose schematic cross-sectional diagram is illustrated in Fig. 1, such reactive ion etch (RIE) etchback planarizing methods and chemical mechanical polish (CMP) planarizing methods typically provide microelectronics fabrication processes inherently of additional complexity and manufacturing cost.

It is thus desirable within the art of microelectronics fabrication to provide spin-on planarizing methods and materials through which there may efficiently be formed upon a microelectronics fabrication having substantial surface topography a spin-on planarizing layer which provides a substantially planarized microelectronics fabrication requiring minimal, if any,

processing prior to forming additional microelectronics layers upon the substantially planarized microelectronics fabrication. It is towards that goal that the present invention is directed.

Various novel methods and materials have been disclosed in the art for forming or modifying substrates or layers which may be formed within microelectronics fabrications.

For example, Mirkin et al., in U.S. Patent No. 5,338,571, discloses a method for forming a self-assembled mono-layer fullerene layer or a self-assembled multi-layer fullerene layer upon a substrate. The self-assembled mono-layer fullerene layer is formed by modifying at least the substrate to provide chemical functionality for covalently bonding from solution a mono-layer fullerene layer to the substrate. The self-assembled multi-layer fullerene layer requires modification of the self-assembled mono-layer fullerene layer to provide additional chemical functionality for covalently bonding from solution a second mono-layer fullerene layer onto the mono-layer fullerene layer.

In addition, Gilton, in U.S. Patent No. 5,597,444, discloses a plasma etch method for etching integrated circuit layers within integrated circuit microelectronics fabrications. The plasma etch method employs an etchant gas composition comprising: (1) a saturated or unsaturated carbon compound selected from the group consisting of acetylene, benzene, graphite and buckminsterfullerene; and (2) a halogen compound selected from the group consisting of fluorine, chlorine, bromine, hydrogen fluoride, hydrogen chloride, hydrogen bromide, sulfur hexafluoride and nitrogen trifluoride. Through the method there is avoided the use of chlorofluorocarbons (CFCs) when etching integrated circuit layers within integrated circuit microelectronics fabrications.

Finally, Chen et al., in "Adsorption and decomposition of C_{60} molecules on Si(111) surfaces," J. Vac. Sci. Technol. B, vol. 14(2), Mar./Apr. 1996, pp. 979-81, discloses a method for selectively forming a silicon carbide layer upon a silicon semiconductor substrate masked with a silicon oxide layer. The method employs thermal decomposition of fullerene molecules adsorbed on unmasked portions of the silicon semiconductor substrate. The method is predicated upon a strong interaction of fullerene molecules with silicon semiconductor substrates, but weak interactions of fullerene molecules with silicon oxide layers formed upon silicon semiconductor substrates.

Desirable within the art of microelectronics fabrication are methods through which a spin-on planarizing material may be formed upon a microelectronics fabrication having a substantial surface topography to provide a substantially planar spin-on planarizing layer yielding a substantially planar microelectronics fabrication which requires minimal, if any, processing prior to forming an additional microelectronics layer within the substantially planar microelectronics fabrication within which is formed the substantially planar spin-on planarizing layer. It is towards that goal that the present invention is directed.

SUMMARY OF THE INVENTION

A first object of the present invention is to provide a method through which a spin-on planarizing material may be formed upon a microelectronics fabrication having substantial surface topography to provide a substantially planar spin-on planarizing layer yielding a substantially planar microelectronics fabrication which requires minimal, if any, processing prior to forming an additional microelectronics layer within the substantially planar microelectronics

fabrication within which is formed the substantially planar spin-on planarizing layer.

A second object of the present invention is to provide a method in accord with the first object of the present invention, which method is readily manufacturable.

In accord with the objects of the present invention, there is provided by the present invention a method for forming a microelectronics fabrication. To form a microelectronics fabrication in accord with the method of the present invention, there is first provided a substrate employed within a microelectronics fabrication. There is then formed over the substrate a spin-on layer, where the spin-on layer has a buckminsterfullerene incorporated therein. The buckminsterfullerene enhances the planarization properties of the spin-on layer. The method of the present invention contemplates a microelectronics fabrication formed in accord with the method of the present invention.

The present invention provides a method through which a spin-on planarizing material may be formed upon a microelectronics fabrication having substantial surface topography to provide a substantially planar spin-on planarizing layer yielding a substantially planar microelectronics fabrication which requires minimal, if any, processing prior to forming an additional microelectronics layer within the substantially planar microelectronics fabrication within which is formed the substantially planar spin-on planarizing layer. The method of the present invention realizes the foregoing object by incorporating a buckminsterfullerene within the spin-on material from which is formed the spin-on planarizing layer. Due to lubricant like properties of the buckminsterfullerene incorporated within the spin-on planarizing material from which is formed the spin-on planarizing layer, the planarizing properties of the spin-on planarizing layer are enhanced.

The method of the present invention is readily manufacturable. Methods through which discrete quantities of buckminsterfullerene materials may be fabricated are known in the art of buckminsterfullerene materials fabrication. Similarly, methods through which various additives may be incorporated into spin-on planarizing materials prior to forming spin-on planarizing layers from those spin-on planarizing materials are also known in the art of spin-on planarizing materials fabrication. Thus, the method of the present invention is readily manufacturable.

BRIEF DESCRIPTION OF THE DRAWINGS

The objects, features and advantages of the present invention are understood within the context of the Description of the Preferred Embodiment, as set forth below. The Description of the Preferred Embodiment is understood within the context of the accompanying drawings, which form a material part of this disclosure, wherein:

Fig. 1 shows a schematic cross-sectional diagram illustrating incomplete planarization of a spin-on planarizing layer formed over a series of patterned microelectronics structures within a microelectronics fabrication in absence of the present invention.

Fig. 2 to Fig. 3 show a pair of schematic cross-sectional diagrams illustrating the results of progressive stages in forming within a microelectronics fabrication a substantially planarized spin-on planarizing layer formed over a series of patterned microelectronics structures within a microelectronics fabrication in accord with a general preferred embodiment of the present invention which comprises a first preferred embodiment of the present invention.

Fig. 4 to Fig. 6 show a series of schematic cross-sectional diagrams illustrating the results of progressive stages in forming within an integrated circuit microelectronics fabrication several spin-on planarizing layers formed over several corresponding series of patterned integrated circuit microelectronics structures in accord with a more specific preferred embodiment of the present invention which comprises a second preferred embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention provides a method through which a spin-on planarizing material may be formed upon a microelectronics fabrication having substantial surface topography to provide a substantially planar spin-on planarizing layer yielding a substantially planar microelectronics fabrication which requires minimal, if any, processing prior to forming an additional microelectronics layer within the substantially planar microelectronics fabrication within which is formed the substantially planar spin-on planarizing layer. The method of the present invention realizes the foregoing object by incorporating a buckminsterfullerene within the spin-on planarizing material from which is formed the spin-on planarizing layer. Due to lubricant like properties of the buckminsterfullerene incorporated within the spin-on planarizing layer, the planarizing properties of the spin-on planarizing layer are enhanced.

The method of the present invention may be employed in forming spin-on planarizing layers within microelectronics fabrications including but not limited to integrated circuit microelectronics fabrications, solar cell microelectronics fabrications, ceramic substrate microelectronics fabrications and flat panel display microelectronics fabrications.

First Preferred Embodiment

Referring now to Fig. 2 to Fig. 3, there is shown a pair of schematic cross-sectional diagrams illustrating the results of progressive stages in forming a substantially planarized spin-on layer planarizing layer formed over a series of patterned microelectronics structures within a microelectronics fabrication in accord with a general preferred embodiment of the present invention which comprises a first preferred embodiment of the present invention. Shown in Fig. 2 is a schematic cross-sectional diagram of the microelectronics fabrication at an early stage in its fabrication in accord with the method of the present invention.

Shown in Fig. 2 is a microelectronics substrate 20 having formed thereupon a series of microelectronics structures 22a, 22b and 22c. Within the first preferred embodiment of the present invention, the microelectronics substrate 20 may be a microelectronics substrate employed within a microelectronics fabrication including but not limited to an integrated circuit microelectronics fabrication, a solar cell microelectronics fabrication, a ceramic substrate microelectronics fabrication or a flat panel display microelectronics fabrication. Although not specifically illustrated within the schematic cross-sectional diagram of Fig. 1, the microelectronics substrate 20 may include the microelectronics substrate itself, or the microelectronics substrate 20 may in addition to the microelectronics substrate itself also include additional microelectronics layers which are conventionally formed upon or over the microelectronics substrate. Such additional microelectronics layers may include, but are not limited to, microelectronics dielectric layers, microelectronics semiconductor layers and microelectronics conductor layers.

With respect to the microelectronics structures 22a, 22b and 22c, the microelectronics structures 22a, 22b and 22c may be formed from any of several microelectronics

materials which are conventionally employed in forming microelectronics structures within microelectronics fabrications. Such microelectronics materials may include, but are not limited to, microelectronics dielectric materials, microelectronics semiconductor materials and microelectronics conductor materials to form microelectronics structures including but not limited to microelectronics dielectric structures, microelectronics semiconductor structures and microelectronics conductor structures.

Although not specifically illustrated by the schematic cross-sectional diagram of Fig. 2, each of the microelectronics structures 22a, 22b or 22c preferably has a linewidth of from about 0.2 to about 100 microns upon the microelectronics substrate 20, an aspect ratio of from about 1:100 to about 40:1 and a pitch of from about 0.4 to about 200 microns separating each microelectronics structure 22a, 22b or 22c from an adjoining microelectronics structure 22a, 22b or 22c.

Referring now to Fig. 3, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the microelectronics fabrication whose schematic cross-sectional diagram is illustrated in Fig. 2. Shown in Fig. 3 is a schematic cross-sectional diagram of a microelectronics fabrication otherwise equivalent to the microelectronics fabrication whose schematic cross-sectional diagram is illustrated in Fig. 2, but wherein there is formed upon the microelectronics substrate 20 and the microelectronics structures 22a, 22b and 22c a spin-on planarizing layer 24. Consistent with the Description of the Related Art within the above Background of the Invention, within the first preferred embodiment of the present invention the spin-on planarizing layer 24 is formed from a spin-on planarizing material chosen from the group of spin-on planarizing materials consisting of spin-on-glass (SOG) materials, aerogel spin-on materials, nanogel spin-on materials and spin-on polymer materials. In distinction with the

Description of the Related Art within the above Background of the Invention, within the first preferred embodiment of the present invention the spin-on planarizing layer 24 has incorporated therein a concentration of a buckminsterfullerene material in order to provide the spin-on planarizing layer 24 within the first preferred embodiment of the present invention with enhanced planarizing properties in comparison with the spin-on planarizing layer 14 as disclosed within the Description of the Related Art within the Background of the Invention and shown in Fig. 1.

In order to provide within the first preferred embodiment of the present invention enhanced planarizing properties of the spin-on planarizing layer 24 in comparison with the spin-on planarizing layer 14 as shown within Fig. 1, there is incorporated into the spin-on planarizing material from which is formed the spin-on planarizing layer 24 the concentration of the buckminsterfullerene material selected from the group of buckminsterfullerene materials including but not limited to a C_{60} buckminsterfullerene material, a C_{70} buckminsterfullerene material and a C_{84} buckministerfullerene material. Preferably, the concentration of the buckminsterfullerene material is incorporated into the spin-on planarizing material from which is formed the spin-on planarizing layer 24 at a level of from about 1 to about 50 weight percent.

The spin-on planarizing layer 24 may be formed within the schematic cross-sectional diagram of Fig. 3 through conventional rotary spin coating methods or closed cup rotary spin coating methods, where the latter methods completely cover the substrate to attenuate solvent evaporation when spin coating a spin-on planarizing layer such as the spin-on planarizing layer 24.

As is illustrated within the schematic cross-sectional diagram of Fig. 3, the spin-on planarizing layer 24 is sufficiently planarized such that there may be typically formed upon the

spin-on planarizing layer 24 additional microelectronics layers without need for additional microelectronics fabrication processing. However, due to its superior lubricating capabilities, the concentration of the buckminsterfullerene incorporated within the spin-on planarizing layer 24 will also allow the spin-on planarizing layer 24, when formed of an appropriate spin-on planarizing material, to be more readily additionally planarized through thermal reflow at reduced thermal reflow temperatures in the range of from about 80 to about 250 degrees centigrade.

Second Preferred Embodiment

Referring now to Fig. 4 to Fig. 6, there is shown a series of schematic cross-sectional diagrams illustrating the results of progressive stages in forming within an integrated circuit microelectronics fabrication several planarized spin-on layers formed over several corresponding series of patterned integrated circuit microelectronics structures in accord with a more specific preferred embodiment of the present invention which comprises a second preferred embodiment of the present invention. Shown in Fig. 4 is a schematic cross-sectional diagram of the integrated circuit microelectronics fabrication at an early stage in its fabrication in accord with the second preferred embodiment of the present invention.

Shown in Fig. 4 is a semiconductor substrate 30 having formed within and upon its surface a pair of isolation regions 32a and 32b which define an active region of the semiconductor substrate 30. Although it is known in the art of integrated circuit microelectronics fabrication that semiconductor substrates are available with either dopant polarity, various dopant concentrations and several crystallographic orientations, for the second preferred embodiment of the present invention, the semiconductor substrate 30 is preferably a (100) silicon semiconductor substrate

having an N- or P- doping.

Similarly, although it is also known in the art of integrated circuit microelectronics fabrication that isolation regions may be formed within and/or upon semiconductor substrates to define active regions of those semiconductor substrates through methods including but not limited to isolation region thermal growth methods and isolation region deposition/patterning methods, for the second preferred embodiment of the present invention the isolation regions 32a and 32b are preferably formed within and upon the semiconductor substrate 30 to define the active region of the semiconductor substrate 30 through an isolation region thermal growth method at a temperature of about 1000 to about 1200 degrees centigrade to form the isolation regions 32a and 32b of silicon oxide within and upon the semiconductor substrate 30.

Shown also within Fig. 1 formed within or upon the active region of the semiconductor substrate 30 is a series of structures which comprises a field effect transistor (FET). The series of structures includes: (1) a gate dielectric layer 34 formed upon the active region of the semiconductor substrate 30; (2) a gate electrode 36 formed and aligned upon the gate dielectric layer 34; (3) a pair of dielectric spacer layers 38a and 38b formed upon a pair of opposite edges of the gate dielectric layer 34 and the gate electrode 36; and (4) a pair of source/drain regions 40a and 40b incorporating a pair of low dose ion implant regions formed within the active region of the semiconductor substrate at areas not covered by the gate dielectric layer 34 and the gate electrode 36. Each of the foregoing structures employed in forming the field effect transistor (FET) within the integrated circuit microelectronics fabrication whose schematic cross-sectional diagram is shown in Fig. 1 may be formed through methods and materials as are conventional in the art of integrated circuit microelectronics fabrication.

For example, although it is known in the art of integrated circuit microelectronics fabrication that gate dielectric layers within field effect transistors (FETs) may be formed through patterning, through methods as are conventional in the art, of blanket gate dielectric layers formed through methods including but not limited to blanket gate dielectric layer thermal growth methods and blanket gate dielectric layer deposition methods, for the second preferred embodiment of the present invention, the gate dielectric layer 34 is preferably formed through patterning, through methods as are conventional in the art, of a blanket gate dielectric layer formed through a blanket gate dielectric layer thermal growth method to form the gate dielectric layer 34 of silicon oxide upon the active region of the semiconductor substrate 30. Preferably, the gate dielectric layer 34 of silicon oxide so formed is from about 20 to about 150 angstroms thick.

Similarly, although it is also known in the art of integrated circuit microelectronics fabrication that gate electrodes may be formed through patterning, through methods as are conventional in the art, of blanket layers of gate electrode materials including but not limited to metals, metal alloys, doped polysilicon and polycides (ie: doped polysilicon/metal silicide stacks) formed upon blanket gate dielectric layers within those integrated circuit microelectronics fabrications, for the preferred embodiment of the present invention, the gate electrode 36 is preferably formed through patterning, through methods as are conventional in the art, of a blanket layer of a doped polysilicon material formed upon the blanket gate dielectric layer to a thickness of from about 1000 to about 5000 angstroms.

Further, it is also known in the art of integrated circuit microelectronics fabrication that dielectric spacer layers may be formed through anisotropic etching of blanket layers of dielectric materials including but not limited to silicon oxide dielectric materials, silicon nitride dielectric materials and silicon oxynitride dielectric materials. For the second preferred

embodiment of the present invention, the dielectric spacer layers 38a and 38b are preferably formed through anisotropic reactive ion etch (RIE) etching of a blanket layer of silicon oxide dielectric material, silicon nitride dielectric material or silicon oxynitride dielectric material to form the pair of dielectric spacer layers 38a and 38b adjoining the pair of opposite edges of the gate dielectric layer 34 and the gate electrode 36.

Finally, it is also known in the art of field effect transistor (FET) fabrication within integrated circuit microelectronics fabrication that source/drain regions are typically formed within an active region of a semiconductor substrate through ion implantation methods employing dopant ions of polarity appropriate to the field effect transistor (FET) desired to be formed. For the second preferred embodiment of the present invention, the pair of source/drain regions 40a and 40b is preferably formed within the active region of the semiconductor substrate 30 through: (1) a low dose implant at an ion implantation dose of from about 1E12 to about 1E14 dopant ions per square centimeter and an ion implantation energy of from about 0.1 to about 200 keV while employing the gate electrode 36 and the gate dielectric layer 34 as a mask; followed by (2) a high dose ion implant at an ion implantation dose of from about 1E15 to about 1E17 dopant ions per square centimeter and an ion implantation energy of from about 0.1 to about 200 keV while employing the gate electrode 36, the gate dielectric layer 34 and the pair of dielectric spacer layers 38a and 38b as a mask. The polarity of the dopant ion employed in forming the pair of source/drain regions 40a and 40b is appropriate to the semiconductor substrate 30 and the field effect transistor (FET).

There is also shown in Fig. 4 formed over the semiconductor substrate 30 including the series of structures which forms the field effect transistor (FET) a planarized pre-metal dielectric (PMD) layer 42. Methods and materials through which planarized dielectric

layers may be formed within integrated circuit microelectronics fabrications are known in the art of integrated circuit microelectronics fabrication. Planarized dielectric layers may be formed within integrated circuit microelectronics fabrications through planarizing, through planarizing methods as are conventional in the art of integrated circuit microelectronics fabrication, of conformal dielectric layers formed within integrated circuit microelectronics fabrications. Conformal dielectric layers may be formed within integrated circuit microelectronics fabrications through methods including but not limited to chemical vapor deposition (CVD) methods, plasma enhanced chemical vapor deposition (PECVD) methods and physical vapor deposition (PVD) sputtering methods to form conformal dielectric layers of dielectric materials including but not limited to silicon oxide dielectric materials, silicon nitride dielectric materials and silicon oxynitride dielectric materials. For the second preferred embodiment of the present invention, the planarized pre-metal dielectric (PMD) layer 42 is preferably formed through planarizing, through a chemical mechanical polish (CMP) planarizing method or reactive ion etch (RIE) etchback planarizing method as is conventional in the art of integrated circuit microelectronics fabrication, a conformal pre-metal dielectric (PMD) layer formed of a silicon oxide dielectric material formed through a plasma enhanced chemical vapor deposition (PECVD) method, as is common in the art of integrated circuit microelectronics fabrication. Other methods and materials may, however, be employed in forming the planarized pre-metal dielectric (PMD) layer 42. Preferably, the planarized pre-metal dielectric (PMD) layer 42 so formed is formed to a thickness of from about 5000 to about 20000 angstroms.

Although not specifically illustrated within the schematic cross-sectional diagram of Fig. 4, it is plausible and under certain circumstances desirable within the second preferred embodiment of the present invention to employ in place of the planarized pre-metal dielectric (PMD) layer 42 a spin-on planarizing layer similar to the spin-on planarizing layer 24 within the

first preferred embodiment of the present invention as illustrated in Fig. 3. Such a spin-on planarizing layer may be employed within the second preferred embodiment of the present invention provided that a thermal treatment to which the planarized pre-metal dielectric (PMD) layer 42 is otherwise exposed (typically for densification purposes) does not exceed about 500 degrees centigrade.

Finally, there is shown in Fig. 4 a series of patterned first conductor layers 44a, 44b and 44c formed upon the planarized pre-metal dielectric (PMD) layer 42, where the series of patterned first conductor layers 44a, 44b and 44c, and exposed portions of the planarized pre-metal dielectric (PMD) layer 42, have formed thereupon a first conformal inter-metal dielectric (IMD) lower layer 46. Within the first second preferred embodiment of the present invention, the series of patterned first conductor layers 44a, 44b and 44c, and the first conformal inter-metal dielectric (IMD) lower layer 46, may be formed through methods as are conventional in the art of integrated circuit microelectronics fabrication.

For example, although it is known in the art of integrated circuit microelectronics fabrication that patterned conductor layers may be formed through patterning, through methods as are conventional in the art, of blanket conductor layers formed within integrated circuit microelectronics fabrications through methods including but not limited to thermally assisted evaporation methods, electron beam assisted evaporation methods, chemical vapor deposition (CVD) methods and physical vapor deposition (PVD) sputtering methods, for the second preferred embodiment of the present invention, the series of patterned first conductor layers 44a, 44b and 44c is preferably formed through patterning, through methods as are conventional in the art, of a blanket first conductor formed at least in part of an aluminum containing conductor material, as is also common in the art of integrated circuit microelectronics fabrication. Similarly

with the microelectronics structures 22a, 22b and 22c within the first preferred embodiment of the present invention as illustrated within the schematic cross-sectional diagrams of Fig. 2 and Fig. 3, each of the patterned first conductor layers 44a, 44b or 44c preferably has a linewidth upon the planarized pre-metal dielectric (PMD) layer 42 of from about 0.2 to about 100 microns, an aspect ratio of from about 0.5:1 to about 40:1 and is separated from an adjoining patterned first conductor layer 44a, 44b or 44c by a pitch of from about 0.4 to about 200 microns. Preferably, each of the patterned first conductor layers 44a, 44b and 44c is formed to a thickness of from about 3000 to about 12000 angstroms upon the planarized pre-metal dielectric (PMD) layer 42.

With respect to the first conformal inter-metal dielectric (IMD) lower layer 46, the first conformal inter-metal dielectric (IMD) lower layer 46 is preferably formed through methods and materials analogous or equivalent to the methods and materials employed in forming the planarized pre-metal dielectric (PMD) layer 42. However, the first conformal inter-metal dielectric (IMD) lower layer 46 is significantly thinner and the first conformal inter-metal dielectric (IMD) lower layer 46 is not planarized. Preferably, the first conformal inter-metal dielectric (IMD) lower layer 46 is formed to a thickness of from about 500 to about 5000 angstroms. Within the second preferred embodiment of the present invention, the first conformal inter-metal dielectric (IMD) lower layer 46 serves as a barrier layer to a spin-on planarizing dielectric layer subsequently formed upon the microelectronics fabrication whose schematic cross-sectional diagram is illustrated in Fig. 4.

Referring now to Fig. 5, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the integrated circuit microelectronics fabrication whose schematic cross-sectional diagram is illustrated in Fig. 4. Shown in Fig. 5 is a schematic cross-sectional diagram of an integrated circuit microelectronics fabrication otherwise equivalent

to the integrated circuit microelectronics fabrication whose schematic cross-sectional diagram is illustrated in Fig. 4, but wherein there is formed upon the first conformal inter-metal dielectric (IMD) lower layer 46 a first spin-on planarizing inter-metal dielectric (IMD) middle layer 48.

Within the second preferred embodiment of the present invention, the first spin-on planarizing inter-metal dielectric (IMD) middle layer 48 is formed through methods and materials analogous or equivalent to the methods and materials employed in forming the spin-on planarizing layer 24 within the first preferred embodiment of the present invention as illustrated within the schematic cross-sectional diagram of Fig. 3. More preferably, within the second preferred embodiment of the present invention the first spin-on planarizing inter-metal dielectric (IMD) middle layer 48 is formed employing a low dielectric constant spin-on dielectric material, such as but not limited to a low dielectric constant spin-on-glass (SOG) dielectric material or a low dielectric constant spin-on polymer dielectric material having a dielectric constant of from about 1.5 to about 3.5. Under such circumstances, the buckminsterfullerene incorporated therein provides particular advantage in providing the first spin-on planarizing inter-metal dielectric (IMD) middle layer 48 with enhanced planarizing abilities and enhanced gap filling capabilities since the buckminsterfullerene incorporated therein itself has a comparatively low dielectric constant, typically from about 2.0 to about 3.5. Low dielectric constant dielectric materials are often desirable when formed interposed between patterned of narrow line width high aspect ratio patterned conductor layers within integrated circuit microelectronics fabrications, since such low dielectric constant dielectric materials often provide integrated circuits within which there is attenuated patterned conductor layer cross-talk and increased integrated circuit speed.

Referring now to Fig. 6, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the integrated circuit microelectronics fabrication

whose schematic cross-sectional diagram is illustrated in Fig. 5. Shown in Fig. 6 is a schematic cross-sectional diagram of an integrated circuit microelectronics fabrication otherwise equivalent to the integrated circuit microelectronics fabrication whose schematic cross-sectional diagram is illustrated in Fig. 5, but wherein, in part, there is formed upon the first spin-on planarizing inter-metal dielectric (IMD) middle layer 48 a first conformal inter-metal dielectric (IMD) upper layer 50.

Within the second preferred embodiment of the present invention, the first conformal inter-metal dielectric (IMD) upper layer 50 is preferably formed through methods and materials analogous or equivalent to the methods and materials employed in forming the first conformal inter-metal dielectric (IMD) lower layer 46. Preferably, the first conformal inter-metal dielectric (IMD) upper layer 50 is formed to a thickness of from about 2000 to about 20000 angstroms.

Also shown within Fig. 6 is the presence of: (1) a series of patterned second conductor layers 52a, 52b and 52c formed upon the first conformal inter-metal dielectric (IMD) upper layer 50; (2) a second conformal inter-metal dielectric (IMD) lower layer 54 formed upon the series of patterned second conductor layers 52a, 52b and 52c and upon exposed portions of the first conformal inter-metal dielectric (IMD) upper layer 50; (3) a second spin-on planarizing inter-metal dielectric (IMD) middle layer 56 formed upon the second conformal inter-metal dielectric (IMD) lower layer 54; and (4) a second conformal inter-metal dielectric (IMD) upper layer 58 formed upon the second spin-on planarizing inter-metal dielectric (IMD) middle layer 56.

Within the second preferred embodiment of the present invention, the series of patterned second conductor layers 52a, 52b and 52c is preferably formed employing methods,

materials and dimensions analogous or equivalent to the methods, materials and dimensions employed in forming the series of patterned first conductor layers 44a, 44b and 44c. Similarly, within the second preferred embodiment of the present invention, the second conformal inter-metal dielectric (IMD) lower layer 54 is preferably formed employing methods, materials and dimensions analogous or equivalent to the methods, materials and dimensions employed in forming the first conformal inter-metal dielectric (IMD) lower layer 46. In addition, within the second preferred embodiment of the present invention, the second spin-on planarizing inter-metal dielectric (IMD) middle layer 56 is preferably formed through methods, materials and dimensions analogous or equivalent to the methods, materials and dimensions employed in forming the first spin-on planarizing inter-metal dielectric (IMD) middle layer 48. Finally, within the second preferred embodiment of the present invention, the second conformal inter-metal dielectric (IMD) upper layer 58 is preferably formed through methods, materials and dimensions analogous or equivalent to the methods, materials and dimensions employed in forming the first conformal inter-metal dielectric (IMD) upper layer 50.

Upon forming the integrated circuit microelectronics fabrication whose schematic cross-sectional diagram is illustrated in Fig. 6, there is formed an integrated circuit microelectronics fabrication having two spin-on planarizing dielectric layers formed therein, where each of the two spin-on planarizing dielectric layers has incorporated therein a concentration of a buckminsterfullerene. The concentration of the buckminsterfullerene incorporated within each of the spin-on planarizing dielectric layers provides the spin-on planarizing dielectric layer so formed with enhanced planarizing abilities and enhanced gap filling capabilities.

As is understood by a person skilled in the art, the preferred embodiments of the present invention are illustrative of the present invention rather than limiting of the present

invention. Revisions and modifications may be made to methods, materials, structures and dimensions through which is provided the preferred embodiments of the present invention while still providing embodiments which are within the spirit and scope of the present invention, as defined by the accompanying claims.

CLAIMS

1. A microelectronics fabrication comprising:

a substrate employed within a microelectronics fabrication;

a spin-on layer formed over the substrate, where the spin-on layer has a buckminsterfullerene material incorporated therein.

2. The microelectronics fabrication of claim 1 wherein the microelectronics fabrication is chosen from the group of microelectronics fabrications consisting of integrated circuit microelectronics fabrications, solar cell microelectronics fabrications, ceramic substrate microelectronics fabrications and flat panel display microelectronics fabrications.

3. The microelectronics fabrication of claim 1 wherein the spin-on layer is formed from a spin-on material chosen from the group of spin on materials consisting of spin-on-glass (SOG) materials, aerogel spin-on materials, nanogel spin-on materials and spin-on polymer materials.

4. The microelectronics fabrication of claim 1 wherein the buckminsterfullerene material is selected from the group of buckminsterfullerene materials consisting of C_{60} buckminsterfullerene materials, C_{70} buckminsterfullerene materials and C_{84} buckministerfullerene materials.

5. A method for forming a microelectronics fabrication comprising:

providing a substrate employed within a microelectronics fabrication;

forming a spin-on layer over the substrate, where the spin-on layer has a buckminsterfullerene material incorporated therein.

6. The method of claim 5 wherein the buckminsterfullerene material enhances the planarization properties of the spin-on layer.

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7. The method of claim 5 wherein the microelectronics fabrication is chosen from the group of microelectronics fabrications consisting of integrated circuit microelectronics fabrications, solar cell microelectronics fabrications, ceramic substrate microelectronics fabrications and flat panel display microelectronics fabrications.

8. The method of claim 5 wherein the spin-on layer is formed from a spin-on material chosen from the group of spin on materials consisting of spin-on-glass (SOG) materials, aerogel spin-on materials, nanogel spin-on materials and spin-on polymer materials.

9. The method of claim 1 wherein the buckminsterfullerene material is selected from the group of buckminsterfullerene materials consisting of C_{60} buckminsterfullerene materials, C_{70} buckminsterfullerene materials and C_{84} buckministerfullerene materials.

10. A microelectronics fabrication fabricated in accord with the method of claim 5.

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