WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a first gate pattern and a second gate pattern on a substrate, the first gate pattern and the second gate pattern being spaced apart from each other; and

a separation pattern that separates the first gate pattern and the second gate pattern from each other,

wherein the first gate pattern includes a first high-k dielectric pattern and a first metal-containing pattern on the first high-k dielectric pattern, the first metal-containing pattern covering a sidewall of the first high-k dielectric pattern,

wherein the second gate pattern includes a second high-k dielectric pattern and a second metal-containing pattern on the second high-k dielectric pattern, and

wherein the separation pattern is in direct contact with the first metal-containing pattern and spaced apart from the first high-k dielectric pattern, and

wherein the first high-k dielectric pattern has an upper sidewall and a lower sidewall that are spaced apart from the separation pattern, the lower sidewall being offset from the upper sidewall, and the first metal-containing pattern is in direct contact with both the upper sidewall and the lower sidewall.

2. The semiconductor device as claimed in claim 1, wherein the first gate pattern and the second gate pattern are elongated in a first direction and placed on an imaginary straight line.

3. The semiconductor device as claimed in claim 2, wherein:

the first gate pattern has a first width parallel to a second direction intersecting the first direction, and

the separation pattern has a second width parallel to the second direction, the second width being equal to or greater than the first width.

4. The semiconductor device as claimed in claim 3, wherein at least a portion of the separation pattern extends in the second direction, the separation pattern having a linear shape when viewed in plan view.

5. The semiconductor device as claimed in any one of claims 1 to 4, wherein:

the first gate pattern further includes a first work function pattern between the first high-k dielectric pattern and the first metal-containing pattern,

a sidewall of the first work function pattern is aligned with the sidewall of the first high-k dielectric pattern,

the first metal-containing pattern is in contact with the sidewall of the first work function pattern, and

the separation pattern is spaced apart from the first work function pattern.

6. The semiconductor device as claimed in any one of claims 1 to 4, wherein:

the first metal-containing pattern includes a first work function pattern and a first metal line pattern, and

the first work function pattern is in contact with the sidewall of the first high-k dielectric pattern.

7. The semiconductor device as claimed in any one of claims 1 to 6, wherein an upper portion of the separation pattern extends to cover a top surface of the first metal-containing pattern.

8. The semiconductor device as claimed in any one of claims 1 to 7, further comprising:

first active fins that protrude from the substrate; and

second active fins that protrude from the substrate,

wherein the first gate pattern crosses over the first active fins,

wherein the second gate pattern crosses over the second active fins, and

wherein a first distance between one of the first active fins that is most adjacent to the second gate pattern and one of the second active fins that is most adjacent to the first gate pattern is greater than a second distance between the first active fins that are adjacent to each other.

9. The semiconductor device as claimed in any one of claims 1 to 7, further comprising:

first active fins that protrude from the substrate;

second active fins that protrude from the substrate; and

a device isolation pattern between the first active fins and the second active fins, the device isolation pattern having a top surface lower than top surfaces of the first and second active fins,

wherein the first gate pattern crosses over the first active fins,

wherein the second gate pattern crosses over the second active fins,

wherein the separation pattern is in contact with the device isolation pattern, and

wherein a bottom surface of the separation pattern is lower than the top surface of the device isolation pattern.

10. The semiconductor device as claimed in any one of claims 1 to 9, wherein:

the first high-k dielectric pattern extends to contact a sidewall of the first metal-containing pattern, the first high-k dielectric pattern extending only on a portion of a bottommost surface of the first metal-containing pattern, and

the second high-k dielectric pattern extends to contact a sidewall of the second metal-containing pattern, the second high-k dielectric pattern extending only on a portion of a bottommost surface of the second metal-containing pattern.

11. The semiconductor device as claimed in claim 10, wherein:

the second metal-containing pattern covers a sidewall of the second high-k dielectric pattern,

the separation pattern is in direct contact with the second metal-containing pattern and spaced apart from the second high-k dielectric pattern, and

the bottommost surfaces of the first and second metal-containing patterns being level with bottommost surfaces of the first and second high-k dielectric patterns, respectively.

12. The semiconductor device as claimed in claim 1, wherein the first gate pattern further includes a first gate capping pattern on the first metal-containing pattern, the first gate capping pattern being in direct contact with a sidewall of the separation pattern.

13. The semiconductor device as claimed in claim 1, further comprising a gate spacer covering both a sidewall of the first gate pattern and a sidewall of the separation pattern.

14. A semiconductor device, comprising:

first active fins that protrude from a substrate;

second active fins that protrude from the substrate and are spaced apart from the first active fins;

a first gate pattern that crosses over the first active fins and is elongated in a first direction;

a second gate pattern that crosses over the second active fins and is elongated in the first direction; and

a separation pattern between the first gate pattern and the second gate pattern,

wherein the first gate pattern includes a first high-k dielectric pattern and a first metal-containing pattern on the first high-k dielectric pattern, the first high-k dielectric pattern being conformal on and between the first active fins, and

wherein the separation pattern is spaced apart from the first high-k dielectric pattern, and

wherein the first high-k dielectric pattern has an upper sidewall and a lower sidewall that are spaced apart from the separation pattern, the lower sidewall being offset from the upper sidewall, and the first metal-containing pattern is in direct contact with both the upper sidewall and the lower sidewall.

15. The semiconductor device as claimed in claim 14, wherein:

the first high-k dielectric pattern extends only on a portion of a bottommost surface of the first metal-containing pattern, and

the first metal-containing pattern is between the separation pattern and a sidewall of the first high-k dielectric pattern.

16. The semiconductor device as claimed in claim 14, wherein:

the second gate pattern includes a second high-k dielectric pattern and a second metal-containing pattern on the second high-k dielectric pattern, and

the separation pattern is in contact with both the first metal-containing pattern and the second metal-containing pattern.

17. The semiconductor device as claimed in any one of claims 14 to 16, wherein:

the first gate pattern has a first width parallel to a second direction intersecting the first direction, and

the separation pattern has a second width parallel to the second direction, the second width being equal to or greater than the first width.

18. The semiconductor device as claimed in any one of claims 14 to 16, wherein an upper portion of the separation pattern protrudes in the first direction or a second direction from a sidewall of the separation pattern, the second direction intersecting the first direction.

19. The semiconductor device as claimed in claim 14, wherein the first gate pattern further includes a first gate capping pattern on the first metal-containing pattern, the first gate capping pattern being in direct contact with a sidewall of the separation pattern.