SYSTEMS AND METHODS OF NON-VOLATILE MEMORY SENSING INCLUDING SELECTIVE/DIFFERENTIAL THRESHOLD VOLTAGE FEATURES

BACKGROUND

Field

The present invention relates to threshold voltage characteristics of MOS circuitry, and, more particularly, to sensing systems and methods associated with differential threshold voltage conditions of MOS devices, such as those in flash memory arrays.

Description of Related Information

Conventional MOS systems and circuitry often use MOS devices characterized by specified threshold voltage and saturation characteristics. Further, some analog signal processing systems, such as those related to array sensing, power on circuitry, comparators, ratio-related latching, buffer driving and other circuits, often have demands such as enhancing margins, increased bitline/leakage control, etc. that are closely associated with their MOS device characteristics. In flash memories, for example, readout and amplification circuitry for sensing operations may operate as a function of such threshold voltage characteristics to maintain linear operation at or throughout desired ranges present on the relevant transistor nodes.

Furthermore, many existing analog flash memory systems include MOS circuitry characterized by unsatisfactory operating points and margins.

In sum, there is a need for sensing systems and methods that may provide adequate operating conditions by, for example, providing differential threshold voltage characteristics, improving voltage operating margins or other voltage conditions, and/or otherwise rendering performance more robust.

SUMMARY

Systems and methods of sensing consistent with the innovations herein are directed to providing selective threshold voltage characteristics via MOS devices having differential threshold voltages.

In one exemplary embodiment, there is provided a metal oxide semiconductor device comprising a substrate of semiconductor material having a source region, a

Claims

1. A sensing circuit comprising:

a reference column including a reference voltage node, a reference memory cell, a first MOS transistor, and a first differential threshold MOS transistor; and

a plurality of data columns, each coupled to a respective data voltage node, in parallel with the reference column, wherein each data column comprises a data memory cell, a second MOS transistor, and a second differential threshold MOS transistor;

wherein one or more of the first and second differential threshold transistors are transistors that each have a gate-to-source threshold voltage that differs from a gate-to-drain threshold voltage;

wherein one or more of the differential threshold transistors comprises:

a substrate of semiconductor material of a first conductivity type;

a first region and a second region in the substrate, wherein the first and second regions are of a second conductivity type and spaced apart from each other defining a channel region therebetween;

an insulating layer disposed over the channel region of the substrate, wherein the insulating layer comprises opposed insulating portions including a first insulating portion adjacent the first region and a second insulating portion adjacent the second region; and

a gate portion above the insulating layer;

wherein each of the first and second insulating portion characterizes a threshold voltage between the gate and the first region or the second region adjacent each insulating portion; and

wherein the first insulating portion is fabricated with varying dimension including a first thickness different than a second thickness of the second insulating portion to provide a first threshold voltage that differs from a second threshold voltage associated with the opposed insulating portion.

2. The circuit of claim 1, wherein one or more of the first and second differential threshold transistors comprises a channel region including a first junction region adjacent a first region and a second junction region adjacent a second region; and

wherein shape of the first insulating portion or shape or implantation of the first junction region are of varying dimension to provide a gate-to-source threshold voltage that differs from a gate-to-drain threshold voltage specified via dimension of one or both of the second insulating portion and/or the second junction region.

3. The circuit of claim 1, wherein one or more of the first and second differential threshold transistors includes a channel region comprising junction regions including a first junction region adjacent the first region and a second junction region adjacent the second region, the first junction region and the second junction region being opposed from each other; and

wherein one or both of shape or implantation of the first junction region or the second junction region are of varying dimension to provide a first threshold voltage that differs from a second threshold voltage associated with the opposed junction region.

4. The circuit of claim 3, wherein the one or both of shape and implantation of the first junction region or the second junction region are varied via supplemental implantation to provide a device having different threshold voltages as a function of the pocket implant.

5. The circuit of claim 3, wherein implantation of the first junction region or the second junction region is varied via supplemental implantation to provide a device having different threshold voltages as a function of the pocket implant.

6. The circuit of claim 5, wherein the varied dimension of the implantation includes one or more of variation in type or composition of implantation, density of implantation, concentration of implantation, and/or variation through a transition region of the first junction region.

7. The circuit of claim 5, wherein the implantation may be of differing composition, including one or more of being doped with differing ions/compounds, having different dosages, formed by differing processes, and/or being fabricated at differing angles.

8. The circuit of claim 5, wherein the implantation is characterized by one or more of differing density/concentration, of varying size, location or strength, and/or of variations of two or more of such differences.

9. The circuit of claim 3, wherein the shape and the implantation of the first junction region or the second junction region are varied via one or more supplemental implants to provide a device having different threshold voltages as a function of the one or more supplemental implants.

10. The circuit of claim 3, further comprising a charge trapping region adjacent the source or drain to control the first threshold voltage or the second threshold voltage.

11. The circuit of claim 1, wherein one or more of the first and second differential threshold transistors comprises:

a substrate of semiconductor material of a first conductivity type;

a first region and a second region in the substrate, wherein the first region and the second region are of a second conductivity type and spaced apart from each other defining a channel region therebetween;

a charge trapping region that yields a first threshold voltage associated with the first region or a second threshold voltage associated with the second region.

12. The circuit of claim 11, wherein the charge trapping region is nitride.

13. The circuit of claim 11, wherein the charge trapping region is a layer.

14. The circuit of claim 13, wherein the layer is nitride.

15. The circuit of claim 1, wherein the first thickness is varied via removal of an offset region from the insulating layer.

16. The circuit of claim 1, wherein a width of the first insulating portion is varied to provide for the differing first threshold voltage.

17. The circuit of claim 1, wherein the first insulating portion includes a region of oxide material removed from the insulating layer to effect a threshold voltage that differs from the second threshold voltage of the second insulating portion.

18. The circuit of claim 17, wherein the region of oxide material removed is in the form of an offset region.

19. The circuit of claim 18, where the offset region is substantially rectilinearly shaped.

20. The circuit of claim 1, wherein the varying dimension effects a change in threshold voltage of 0.1 volts to 0.5 volts.

21. The circuit of claim 1, further comprising a charge trapping region adjacent the first region or the second region to control one or both of the first threshold voltage or the second threshold voltage.

22. A sensing circuit comprising:

a reference column including a reference voltage node, a reference memory cell, a first MOS transistor, and a first differential threshold MOS transistor; and

a plurality of data columns, each coupled to a respective data voltage node, in parallel with the reference column, wherein each data column comprises a data memory cell, a second MOS transistor, and a second differential threshold MOS transistor;

wherein one or more of the first and second differential threshold transistors are transistors that each have a gate-to-source threshold voltage that differs from a gate-to-drain threshold voltage;

wherein one or more of the first and second differential threshold transistors comprises:

a substrate of semiconductor material of a first conductivity type;

a first region and a second region in the substrate, wherein the first region and the second region are of a second conductivity type and spaced apart from each other defining a channel region therebetween;

an insulating layer disposed over the channel region of the substrate, wherein the insulating layer comprises opposed insulating portions including a first insulating portion adjacent the first region and a second insulating portion adjacent the second region, and wherein each insulating portion defines a threshold voltage between the gate and the first region or the second region associated with each insulating portion; and

a gate portion above the insulating layer;

wherein the first insulating portion or the second insulating portion is fabricated of varying length and width, and of different dimension than the opposed insulating portion, to provide a first threshold voltage that differs from a second threshold voltage associated with the opposed insulating portion.

23. The circuit of claim 22, wherein the first insulating portion or the second insulating portion that is fabricated of varying length is also fabricated of varying width.

24. The circuit of claim 22, wherein the insulating layer is transitions from lower to higher surface area to provide the first threshold voltage that differs from an opposed threshold voltage.

25. The circuit of claim 22, wherein the insulating layer is comprised of a plurality portions of two or more differing lengths and/or widths, with differentiation between the plurality of portions denoted by transition regions that reflect transition from regions of differing length and/or width, wherein each of the plurality of portions being characterized by differing threshold voltages.

26. The circuit of claim 25, wherein an overall or composite threshold voltage for each source or each drain being determined as a function of each threshold voltage subcomponent.

27. A sensing circuit comprising:

a reference column including a reference voltage node, a reference memory cell, a first MOS transistor, and a first differential threshold MOS transistor; and

a plurality of data columns, each coupled to a respective data voltage node, in parallel with the reference column, wherein each data column comprises a data memory cell, a second MOS transistor, and a second differential threshold MOS transistor;

wherein one or more of the first and second differential threshold transistors are transistors that each have a gate-to-source threshold voltage that differs from a gate-to-drain threshold voltage;

wherein one or more of the first and second differential threshold transistors includes a metal oxide semiconductor device comprising:

a substrate of semiconductor material of a first conductivity type;

a first region and an opposed second region in the substrate, wherein the first region and the second region are of a second conductivity type and spaced apart from each other defining a channel region therebetween;

an insulating layer disposed over the channel region of the substrate, wherein the insulating layer comprises opposed insulating portions including a first insulating portion adjacent the first region and a second insulating portion adjacent the second region, and wherein each insulating portion defines a threshold voltage between the gate and the first region or the second region associated with each insulating portion; and

a gate portion above the insulating layer;

wherein the first insulating portion or the second insulating portion is fabricated of differing dimension, including varying length, than the opposed insulating portion, to provide a first threshold voltage that differs from a second threshold voltage associated with the opposed insulating portion.

28. The circuit of claim 27, wherein the differing dimension further includes different surface area or volumetric dimension in the length direction.

29. The circuit of claim 22 or 27, further comprising a charge trapping region adjacent the source or drain to control one or both of the first threshold voltage or the second threshold voltage.

30. A sensing circuit comprising:

a reference column including a reference voltage node, a reference memory cell, a first MOS transistor, and a first differential threshold MOS transistor; and

a plurality of data columns, each coupled to a respective data voltage node, in parallel with the reference column, wherein each data column comprises a data memory cell, a second MOS transistor, and a second differential threshold MOS transistor;

wherein one or more of the first and second differential threshold transistors are transistors that each have a gate-to-source threshold voltage that differs from a gate-to-drain threshold voltage;

wherein one or more of the first and second differential threshold transistors includes a metal oxide semiconductor device comprising:

two or more MOS transistor subelements electrically arranged in series, each transistor including:

a substrate of semiconductor material of a first conductivity type;

a first region and a second region in the substrate, wherein the first region and the second region are of a second conductivity type and spaced apart from each other defining a channel region therebetween;

an insulating layer disposed over the channel region of the substrate; and

a gate portion above the insulating layer; and

wherein a first insulating portion of a first transistor is fabricated of a first width that is different than a second width of a second insulating portion of a second transistor, to provide a first threshold voltage of the device that differs from a second threshold voltage of the device.

31. The circuit of claim 30, comprised of three MOS transistor subelements including a first insulating portion, a second insulating portion and a third insulating portion, wherein the insulating portions define threshold voltages for each subelement.

32. The circuit of claim 31, wherein a highest threshold voltage of the subelements determines an overall or composite threshold voltage of the device.

33. The circuit of claim 30, further comprising at least one charge trapping region associated with one or more of the first insulating portion, the second insulating portion, or an insulating portion of another transistor of the two or more transistors, to control one or both of the first threshold voltage or the second threshold voltage.

34. A sensing circuit comprising:

a reference column including a reference voltage node, a reference memory cell, a first MOS transistor, and a first differential threshold MOS transistor; and

a plurality of data columns, each coupled to a respective data voltage node, in parallel with the reference column, wherein each data column comprises a data memory cell, a second MOS transistor, and a second differential threshold MOS transistor;

wherein one or more of the differential threshold transistors are transistors that each have a gate-to-source threshold voltage that differs from a gate-to-drain threshold voltage;

wherein one or more of the differential threshold transistors comprises:

a substrate of semiconductor material of a first conductivity type;

a first region and a second region in the substrate, wherein the first region and the second region are of a second conductivity type and spaced apart from each other defining a channel region therebetween;

a charge trapping region that yields a first threshold voltage associated with the first region or a second threshold voltage associated with the second region.

35. The circuit of claim 34, wherein the charge trapping region is nitride.

36. The circuit of claim 34, wherein the charge trapping region is a layer.

37. The circuit of claim 36, wherein the layer is nitride.

38. The sensing circuit of any one of claims 1, 22, 27, 30 and 34, wherein the first MOS transistor is a cascoding transistor.

39. The sensing circuit of any one of claims 1, 22, 27, 30 and 34, wherein one or more of the first and/or second differential threshold MOS transistors are diode connected and/or are NMOS or native NMOS transistor(s).

40. The sensing circuit of any one of claims 1, 22, 27, 30 and 34, wherein one or more of the data voltage node are each coupled to a comparator.

41. The sensing circuit of any one of claims 1, 22, 27, 30 and 34, wherein each data voltage node is coupled to a comparator.

42. The sensing circuit of any one of claims 1, 22, 27, 30 and 34, wherein one or more of the differential threshold transistor(s) is/are cascoding transistor(s).

43. The sensing circuit of any one of claims 1, 22, 27, 30 and 34, wherein one or more of the differential threshold MOS transistors are transistors having a channel region including a first junction region and a second junction region, wherein shape of the first insulating portion or shape or implantation of the first junction region are of varying dimension to provide a gate-to-source threshold voltage that differs from a gate-to-drain threshold voltage specified via dimension of one or both of the second insulating portion and/or the second junction region.

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BACKGROUND

Field

The present invention relates to threshold voltage characteristics of MOS circuitry, and, more particularly, to sensing systems and methods associated with differential threshold voltage conditions of MOS devices, such as those in flash memory arrays.

Description of Related Information

Conventional MOS systems and circuitry often use MOS devices characterized by specified threshold voltage and saturation characteristics. Further, some analog signal processing systems, such as those related to array sensing, power on circuitry, comparators, ratio-related latching, buffer driving and other circuits, often have demands such as enhancing margins, increased bitline/leakage control, etc. that are closely associated with their MOS device characteristics. In flash memories, for example, readout and amplification circuitry for sensing operations may operate as a function of such threshold voltage characteristics to maintain linear operation at or throughout desired ranges present on the relevant transistor nodes.

Furthermore, many existing analog flash memory systems include MOS circuitry characterized by unsatisfactory operating points and margins.

In sum, there is a need for sensing systems and methods that may provide adequate operating conditions by, for example, providing differential threshold voltage characteristics, improving voltage operating margins or other voltage conditions, and/or otherwise rendering performance more robust.

US 2009/016106 A1 relates to various circuits including MOS transistors that have a bulk voltage terminal for receiving a bulk voltage that is different from a supply voltage and ground. The bulk voltage may be selectively set so that some MOS transistors have a bulk voltage set to the supply voltage or ground and other MOS transistors have a bulk that is different. The bulk voltage may be set to forward or reverse bias pn junctions in the MOS transistor. The various circuits include

comparators, operational amplifiers, sensing circuits, decoding circuits and the other circuits. The circuits may be included in a memory system.

SUMMARY

Systems and methods of sensing consistent with the innovations herein are directed to providing selective threshold voltage characteristics via MOS devices having differential threshold voltages. The present invention is defined in the independent claim 1. The dependent claims defined embodiments of the present invention.

A metal oxide semiconductor device comprising a substrate of semiconductor material having a source region, a

CLAIMS

1. A sensing circuit (200) comprising:

a reference column (230) including a reference voltage node, a reference memory cell (226), a first MOS transistor (218), and a first differential threshold MOS transistor (214); and

a plurality of data columns (250, 270), each coupled to a respective data voltage node, in parallel with the reference column (230), wherein each data column comprises a data memory cell (274, 294), a second MOS transistor (266, 286), and a second differential threshold MOS transistor (262, 282);

wherein one or more of the differential threshold transistors (214; 262, 282) are transistors that each have a gate-to-source threshold voltage that differs from a gate-to-drain threshold voltage.

2. The sensing circuit (200) of claim 1, wherein one or more of the differential threshold transistors (214; 262, 282; 1100) comprises:

a substrate (1110) of semiconductor material of a first conductivity type;

a first region (1144) and a second region (1142) in the substrate (1110), wherein the first and second regions (1144, 1142) are of a second conductivity type and spaced apart from each other defining a channel region (1140) there between;

an insulating layer (1120) disposed over the channel region (1140) of the substrate (1110), wherein the insulating layer (1120) comprises opposed insulating portions including a first insulating portion (1120a) adjacent the first region (1144) and a second insulating portion (1120b) adjacent the second region (1142); and

a gate portion (1130) above the insulating layer (1120);

wherein each insulating portion (1120a, 1120b) characterizes a threshold voltage between the gate (1130) and the first region (1144) or the second region (1142) adjacent each insulating portion (1120a, 1120b); and

wherein the first insulating portion (1120a) is fabricated with varying dimension including a first thickness different than a second thickness of the second insulating portion (1120b) to provide a first threshold voltage that differs from a second threshold voltage associated with the opposed insulating portion.

3. The sensing circuit (200) of claim 1 or 2, wherein the first MOS transistor (218) is a cascoding transistor; and/or

wherein one or more of the first and/or second differential threshold MOS transistors (214; 262, 282) are diode connected and/or are NMOS or native NMOS transistor(s); and/or

wherein one or more of the data voltage node are each coupled to a comparator (258, 278); or

wherein each data voltage node is coupled to a comparator (258, 278).

4. The sensing circuit (200) of claim 1 or 2, wherein one or more of the differential threshold transistor(s) (214; 262, 282) is/are cascoding transistor(s); and/or

wherein one or more of the differential threshold MOS transistors (214; 262, 282; 1100) are transistors having a channel region (1140) including a first junction region (1160a) and a second junction region (1160b), wherein shape of the first insulating portion (1120a) or shape or implantation of the first junction region (1160a) are of varying dimension to provide a gate-to-source threshold voltage that differs from a gate-to-drain threshold voltage specified via dimension of one or both of the second insulating portion (1120b) and/or the second junction region (1160b).

5. The circuit (200) of claim 2, wherein one or more of the differential threshold transistors (214; 262, 282; 1100) comprises a channel region (1140) including a first junction region (1160a) adjacent a first region (1144a, 1142a) and a second junction region (1160b) adjacent a second region (1144b, 1142b); and

wherein shape of the first insulating portion (1120a) or shape or implantation of the first junction region (1160a) are of varying dimension to provide a gate-to-source threshold voltage that differs from a gate-to-drain threshold voltage specified via dimension of one or both of the second insulating portion (1120b) and/or the second junction region (1160b); and/or

wherein one or more of the differential threshold transistors (214; 262, 282; 1100) includes a channel region (1140) comprising junction regions (1160a, 1160b) including a first junction region (1160a) adjacent the first region (1144a, 1142a) and a second junction region (1160b) adjacent the second region (1144b, 1142b), the first junction region (1160a) and the second junction region (1160b) being opposed from each other; and

wherein one or both of shape or implantation of the first junction region (1160a) or the second junction region (1160b) are of varying dimension to provide a first threshold voltage that differs from a second threshold voltage associated with the opposed junction region; and/or

wherein preferably the one or both of shape and implantation of the first junction region (1160a) or the second junction region (1160b) are varied via supplemental implantation to provide a device having different threshold voltages as a function of the pocket implant; and/or

wherein preferably implantation of the first junction region (1160a) or the second junction region (1160b) is varied via supplemental implantation to provide a device having different threshold voltages as a function of the pocket implant; and/or

wherein preferably the varied dimension of the implantation includes one or more of variation in type or composition of implantation, density of implantation, concentration of implantation, and/or variation through a transition region of the first junction region (1160a); and/or

wherein preferably the implantation may be of differing composition, including one or more of being doped with differing ions/compounds, having different dosages, formed by differing processes, and/or being fabricated at differing angles; and/or

wherein preferably the implantation is characterized by one or more of differing density/concentration, of varying size, location or strength, and/or of variations of two or more of such differences; and/or

wherein preferably the shape and the implantation of the first junction region (1160a) or the second junction region (1160b) are varied via one or more supplemental implants to provide a device having different threshold voltages as a function of the one or more supplemental implants; and/or

further preferably comprising a charge trapping region adjacent the source or drain to control the first threshold voltage or the second threshold voltage.

6. The circuit (200) of claim 1 or 2, wherein one or more of the differential threshold transistors (214; 262, 282; 1200) comprises:

a substrate (1210) of semiconductor material of a first conductivity type;

a first region (1244) and a second region (1242) in the substrate (1210), wherein the first region (1244) and the second region (1242) are of a second conductivity type and spaced apart from each other defining a channel region (1240) there between;

a charge trapping region that yields a first threshold voltage associated with the first region (1244) or a second threshold voltage associated with the second region (1242); and

wherein preferably the charge trapping region is nitride; and/or

wherein preferably the charge trapping region is a layer.

7. The sensing circuit (200) of claim 2, wherein the first thickness is varied via removal of an offset region (1336) from the insulating layer (1322); and/or

wherein preferably a width of the first insulating portion (1324) is varied to provide for the differing first threshold voltage; and/or

wherein preferably a width of the first insulating portion (1324) is varied to provide for the differing first threshold voltage; and/or

wherein preferably the first insulating portion (1324) includes a region of oxide material removed from the insulating layer (1322) to effect a threshold voltage that differs from the second threshold voltage of the second insulating portion (1326).

8. The circuit (200) of claim 7, wherein the region of oxide material removed is in the form of an offset region (1336); and/or where the offset region (1336) is substantially rectilinearly shaped.

9. The circuit (200) of claim 2 wherein the varying dimension effects a change in threshold voltage of about 01. volts to about 0.5 volts.

10. The circuit (200) of claim 2, further comprising a charge trapping region adjacent the first region (1144) or the second region (1142) to control one or both of the first threshold voltage or the second threshold voltage.

11. The sensing circuit (200) of claim 1, wherein one or more of the differential threshold transistors (214; 262, 282; 1300) comprises:

a substrate (1310) of semiconductor material of a first conductivity type;

a first region (1344) and a second region (1344) in the substrate (1310), wherein the first region (1344) and the second region (1344) are of a second conductivity type and spaced apart from each other defining a channel region there between;

an insulating layer (1322) disposed over the channel region of the substrate (1310), wherein the insulating layer (1322) comprises opposed insulating portions including a first insulating portion (1324) adjacent the first region (1344) and a second insulating portion (1326) adjacent the second region (1344), and wherein each insulating portion (1324, 1326) defines a threshold voltage between the gate and the first region (1344) or the second region (1344) associated with each insulating portion (1324, 1326); and

a gate portion above the insulating layer (1322);

wherein the first insulating portion (1324) or the second insulating portion (1326) is fabricated of varying length and width, and of different dimension than the opposed insulating portion, to provide a first threshold voltage that differs from a second threshold voltage associated with the opposed insulating portion.

12. The sensing circuit (200) of claim 11, wherein preferably the first insulating portion (1324) or the second insulating portion (1326) that is fabricated of varying length is also fabricated of varying width; and/or

wherein preferably the insulating layer (1322) is transitions from lower to higher surface area to provide the first threshold voltage that differs from an opposed threshold voltage; and/or

wherein preferably the insulating layer (1322) is comprised of a plurality portions of two or more differing lengths and/or widths, with differentiation between the plurality of portions denoted by transition regions that reflect transition from regions of differing length and/or width, wherein each of the plurality of portions being characterized by differing threshold voltages; and/or

wherein preferably an overall or composite threshold voltage for each source or each drain being determined as a function of each threshold voltage subcomponent; and/or

further preferably comprising a charge trapping region adjacent the source or drain to control one or both of the first threshold voltage or the second threshold voltage.

13. The sensing circuit (200) of claim 1, wherein one or more of the differential threshold transistors (214; 262, 282; 1300) includes a metal oxide semiconductor device comprising:

a substrate (1310) of semiconductor material of a first conductivity type;

a first region (1344) and an opposed second region (1344) in the substrate (1310), wherein the first region (1344) and the second region (1344) are of a second conductivity type and spaced apart from each other defining a channel region there between;

an insulating layer (1322) disposed over the channel region of the substrate (1310), wherein the insulating layer (1322) comprises opposed insulating portions including a first insulating portion (1324) adjacent the first region (1344) and a second insulating portion (1326) adjacent the second region (1344), and wherein each insulating portion (1324, 1326) defines a threshold voltage between the gate and the first region (1344) or the second region (1344) associated with each insulating portion (1324, 1326); and

a gate portion above the insulating layer (1322);

wherein the first insulating portion (1324) or the second insulating portion (1326) is fabricated of differing dimension, including varying length, than the opposed insulating portion, to provide a first threshold voltage that differs from a second threshold voltage associated with the opposed insulating portion.

14. The sensing circuit (200) of claim 13, wherein preferably the differing dimension further includes different surface area or volumetric dimension in the length direction; and/or

further preferably comprising a charge trapping region adjacent the source or drain to control one or both of the first threshold voltage or the second threshold voltage.

15. The sensing circuit (200) of claim 1, wherein one or more of the differential threshold transistors (214; 262, 282; 1600) includes a metal oxide semiconductor device comprising:

two or more MOS transistor sub-elements electrically arranged in series, each transistor including:

a substrate (1610) of semiconductor material of a first conductivity type;

a first region and a second region in the substrate (1610), wherein the first region and the second region are of a second conductivity type and spaced apart from each other defining a channel region there between;

an insulating layer (1630) disposed over the channel region of the substrate (1610); and

a gate portion above the insulating layer; and

wherein a first insulating portion (1632) of a first transistor is fabricated of a first width that is different than a second width of a second insulating portion (1634) of a second transistor, to provide a first threshold voltage of the device that differs from a second threshold voltage of the device.

16. The sensing circuit (200) of claim 15, preferably comprised of three MOS transistor sub-elements including a first insulating portion (1632), a second insulating portion (1634) and a third insulating portion (1636), wherein the insulating portions (1632, 1634, 1636) define threshold voltages for each sub-element; and

wherein preferably a highest threshold voltage of the sub-elements determines an overall or composite threshold voltage of the device; and/or

further preferably comprising at least one charge trapping region associated with one or more of the first insulating portion (1632), the second insulating portion (1634), or an insulating portion of another transistor of the two or more transistors, to control one or both of the first threshold voltage or the second threshold voltage.

17. The sensing circuit (200) of claim 1, further preferably comprising a charge trapping region adjacent the source or drain to control the first threshold voltage or the second threshold voltage.

18. The circuit (200) of claim 17, wherein one or more of the differential threshold transistors (214; 262, 282; 1200) comprises:

a substrate (1210) of semiconductor material of a first conductivity type;

a first region (1244) and a second region (1242) in the substrate (1210), wherein the first region (1244) and the second region (1242) are of a second conductivity type and spaced apart from each other defining a channel region (1240) there between;

a charge trapping region that yields a first threshold voltage associated with the first region (1244) or a second threshold voltage associated with the second region (1242); and

wherein preferably the charge trapping region is nitride; and/or

wherein preferably the charge trapping region is a layer.

19. The sensing circuit (200) of one of claims 11, 13, 15, or 17, wherein the first MOS transistor (218) is a cascoding transistor; and/or

wherein one or more of the first and/or second differential threshold MOS transistors (214; 262, 282) are diode connected and/or are NMOS or native NMOS transistor(s); and/or

wherein one or more of the data voltage node are each coupled to a comparator (258, 278); and/or

wherein each data voltage node is coupled to a comparator (258, 278).

20. The sensing circuit (200) of one of claims 11, 13, 15, or 17, wherein one or more of the differential threshold transistor(s) (214; 262, 282) is/are cascoding transistor(s); and/or

wherein one or more of the differential threshold MOS transistors (214; 262, 282; 1100) are transistors having a channel region (1140) including a first junction region (1160a) and a second junction region (1160b), wherein shape of the first insulating portion (1120a) or shape or implantation of the first junction region (1160a) are of varying dimension to provide a gate-to-source threshold voltage that differs from a gate-to-drain threshold voltage specified via dimension of one or both of the second insulating portion (1120b) and/or the second junction region (1160b).