NEW HDD CHIP SET PARTITIONING

TECHNICAL FIELD OF THE INVENTION

The present invention relates to read channel circuits, and more particularly to the chips that the read channel circuits are formed on.

BACKGROUND OF THE INVENTION

The total number of chips required to implement a hard disk drive system varies but may be 7 chips. These chips may be titled read-channel, servo, preamp, DRAM, Controller, flash memory, DSP. Consolidating the digital CMOS chips together in a single chip (or any form of combination of these chips) allows reduction of total number of chips needed and offers lower cost.

This is shown in Figure 1 and allows for the DSP, the controller and possibly DRAM and Flash memory in a single chip.

Chip consolidation allows improved performance at the right time with lowest cost.

In order to reduce development time of read-channel circuits and improve testability, the read-channel has been designed digitally. However, this digital design requires a conversion of the necessary signals from analog-to-digital in a forward section of the communication channel. (read-channel). However, no matter how soon or how far forward the signal processing becomes digital in the read-channel, the analog front-end remains to be the most critical in terms of development time and performance delivery. As integration in a digital CMOS process is required to achieve cost, time and performance, the analog front-end becomes harder and trickier to implement. Advanced CMOS processes with small feature size require lower supply voltage which will affect the performance of the

analog front-end significantly, lower signal-to-noise, lower supply rejection and longer design cycle. Moreover, typical generic CMOS process does not contain capacitors, resistors nor low-threshold devices that are necessary to achieve improved analog performance at lower area. Incorporating any of these electrical elements in a generic CMOS process is generally non-standard and will result in higher cost, longer process development and untransportable design. Therefore the analog front-end in the read channel is one of the most important problems to allow full integration of chip sets. The integration, is affected by higher digital noise, higher noise coupling via substrate, lower data rate, lower supply rejection (no cascade at low supply), and higher process fluctuation.

This integration does not necessarily mean low-cost because the capacitor area is large (Metal/Metal cap), and low performance, i.e. analog front-end will require digital equalization (larger number of taps) to fix the non idealities.

SUMMARY OF THE INVENTION

A new architectural partitioning for chip integration is proposed that allows for low-cost while delivers performance at a much lower risk than previous proposal.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is circuit diagram of a read-channel circuit;

Fig. 2 is an overall circuit diagram;

Fig. 3 is proposed partition for a read-channel;

Fig. 4 is a circuit diagram of a analog section of the read-channel; and

Fig. 5 is a circuit diagram of a digital section of the read-channel.

DETAILED DESCRIPTION OF THE INVENTION

The read-channel may be to be partitioned into two parts. The first part is the analog front-end AGC, VGA, LPF, Ref and may be servo
and is referred to as RDCH#1 1 100. While the second part will contain the digital section (FIR CMS, Viterbi detector, SBDT, Decoder, Describe I/O interface, write path, PLC, time base generator) RDCH#2 200. As shown in Figure 2, the first part, RDCH#1 1 100 will be integrated along the preamp on the flex. This is important where BiCMOS technology is required to deliver noise and speed performance. The addition of RDCH#1 100 to the preamp will not adversely impact the performance of the preamp. In fact, it may reduce the need for external AC-coupling and additional thermal Asperity detection and compensation (used to be in both read-channel and preamp).

Also, there will be no additional clocks needed. Programming is achieved via a serial port for example. A conceptual block diagram is shown in Figure 4.

The second part RDCH#2 200 that is mainly digital in nature is now more adaptable to CMOS standard (or Generic) process. Process improvements will be readily applicable to this part of the read channel. The only analog part of RDCH#2 200 is the Analog-to-Digital convertor (ADC). If this A/D converter would have been placed in RDCH#1 100 then the performance of this circuit will degrade due to switching noise coupling in the most sensitive part of the system, for example the preamp. In this scheme, the ADC will be placed on RDCH#2 200, as shown in Figure 5, to allow for noise isolation in RDCH#1 100. Also, to reduce power due to not having 6 or 7 interface bits switching at max clock rate. Moreover, this might make the flex design more difficult if ADC is placed in RDCH#1 100.

In this proposal the only problem element is ADC design on board of digital process (Generic). Typical ADC designs do not require large capacitances (Flash

ADC) and in some cases no capacitors at all folding ADC. Moreover, the output of ADC does not have to drive large lead at clock max clock rate.

The advantage of current architecture is:

1. Can start design based on current technology by simply partitioning the chip this reduces the design time.
2. ADC is the only analog circuit in the digital partition.
3. No need to develop a special technology.
4. Transfer to new digital technology of the read-channel with little redesign of ADC.
5. True low-cost solution while delivering performance.

THIS SHEET HAS BEEN REPLACED

WHAT IS CLAIMED IS:

1. A read channel circuit comprising:

a digital portion of the read channel circuit;

an analog potion of the read channel circuit; and

an ADC conversion to connect the digital portion with the analog portion, wherein the analog portion is positioned on a different chip than the digital portion.

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