

DESCRIPTION

VIDEO SIGNAL PROCESSING DEVICE

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TECHNICAL FIELD

The present invention relates to a video signal processing device in an image display device (e.g., crystal liquid display, plasma display) on which pixels are fixed in number for display and, more specifically, to a video signal processing device
10 subjecting a video signal inputted into the image display device to A/D conversion with two-phase processing.

BACKGROUND ART

In recent years, with advancement in resolution of a
15 computer being an image signal source, a clock frequency for an image display device has been becoming increasingly faster. In order to bring the image display device to deal with the faster clock frequency, a digital signal processing device where an incoming A/D-converted video signal is processed is required to
20 operate according to the faster clock. This brings about problems such as higher power consumption in the image display device, and increase in cost, for example.

To get around such problems, a conventional image display device lowers the clock frequency to half by carrying out
25 two-phase processing in an A/D converter. Thereby, the digital

signal processing device provided in a stage subsequent to the A/D converter has no need to operate in accordance with the faster clock. Herein, the processing carried out in the A/D converter may be four-phase or six-phase, and is similarly effective to the two-phase processing.

Herein, as to the A/D converter carrying out the two-phase processing, various types of products are available. For example, those include a CXA3026AQ model (manufactured by SONY), and an AD9054BST model (manufactured by AnalogDevices).

FIG. 17 is a block diagram showing the structure of the conventional video signal processing device carrying out the two-phase processing in the A/D converter. In FIG. 17, the video signal processing device is an A/D converter 3 receiving a reference signal 9 and a video signal 24 from an image signal source, carrying out the two-phase processing, and outputting first phase data 10 and second phase data 11. Described next below is the operation of such video signal processing device with reference to FIGS. 17 and 18.

FIG. 18 is a diagram in assistance of explaining the operation of the A/D converter 3 in FIG. 17. In FIG. 18, *a* to *e* denote video data included in the video signal 24 in a valid video period. Blackened objects in the shape of a circle, diamond, square, and triangle denote data in the pedestal level, specifically black data, in a back porch. Moreover, *t*₁ to *t*₁₀ each indicate a certain time. Arrows therein schematically show

the two-phase processing in the A/D converter 3.

In FIG. 18, the video signal 24 includes the back porch and the video data. The back porch is between time t_1 (or before) and time t_5 , while the video signal data is included from time t_5 and onward. Accordingly, the video signal 24 has such structure that a leading edge of a signal including the video data follows an end of the back porch.

Herein, with reference to a pulse of the reference signal 9 provided to the A/D converter 3, the digital data both outputted from the A/D converter 3 is determined based on a phase relationship between the digital data and the video signal 24. Generally, the reference signal 9 is a horizontal synchronizing signal provided from the image signal source.

First, as to the first phase data 10, with reference to the pulse of the reference signal 9, the A/D converter 3 starts the two-phase processing at time t_1 . As shown in FIG. 18, at time t_3 , the black data denoted by the blackened circle is outputted from the A/D converter 3 as the first phase data 10. At the same time, the black data denoted by the diamond is outputted from the A/D converter 3 as the second phase data 11. Thereafter, similarly at time t_5 , the black data each denoted by the square and the triangle is outputted.

Accordingly, in the video signal 24, when the number of data in the back porch, that is from a leading edge of the pulse of the reference signal 9 to immediately before head data a , is even,

the head data a is outputted from the A/D converter 3 as the first phase data 10. On the other hand, when the number of data in the back porch is odd, the head data a is outputted from the A/D converter 3 as the second phase data 11.

5 The problem herein is, if such conventional structure is applied, a display, e.g., crystal liquid display and plasma display, on which pixels are fixed in number for display, may cause one dot short when displaying the video data. Next below, such problem is described by referring to FIGS. 19 and 20.

10 FIG. 19 is a schematic diagram in assistance of explaining the arrangement of output data and display status on the display for a case where the video data a shown in FIG. 18 is outputted from the A/D converter as the first phase data. FIG. 20(a) is a schematic diagram in assistance of explaining the arrangement
15 of output data and display status on the display for a case where the video data a shown in FIG. 18 is outputted from the A/D converter as the second phase data. FIG. 20(b) is a schematic diagram in assistance of explaining the case that the data arrangement is the same as in FIG. 20(a), but the display status
20 is different therefrom.

In FIGS. 19 and 20, a to t denote data included in a video signal, from an image signal source, observed on an arbitrary scan line in a valid video period. Herein, the data inside of a frame in the shape of a square is displayed on the display, while the
25 data outside of the frame is not displayed on the display.

As shown in FIG. 19, when the head data (data displayed on the left end on the display) a of the video signal is included in the first phase data 10 outputted from the A/D converter, the display where pixels displayed thereon are fixed in number displays every video data from a to t . On the other hand, as shown in FIGS. 20(a) and (b), when the head data a is included in the second phase data 11, either the video data t on the right end or the video data a on the left end is problematically not displayed on the display. This is because the digital signal processing device in the stage subsequent to the A/D converter 3 carries out processing in a frequency half of a dot clock coming from the image signal source, causing a video phase on the display to change only in pairs of pixels.

As is known from the above, with the conventional video signal processing device, when the head data a is included in the second phase data 11, the video data is displayed in a state of one dot short as shown in FIG. 20(a) or (b). Consequently, as shown in FIG. 19, the video data a to t cannot be simultaneously displayed.

Therefore, an object of the present invention is to provide a video signal processing device being capable of, even if with an A/D converter carrying out the two-phase processing, displaying every pixel on a display even if a head of video data is not in the first phase output data.

DISCLOSURE OF THE INVENTION

A first aspect of the present invention is directed to a video signal processing device for displaying, on a display, every pixel in a video signal inputted from an image signal source, the
5 device comprising:

a clock delay circuit for receiving a reference signal, and delays the reference signal by the odd number of clocks for output;

a multiplexer for selecting either the reference signal or an output signal from the clock delay circuit for output;

10 an A/D converter for converting the video signal into a digital signal for two-phase output as first phase data and second phase data with reference to an output signal from the multiplexer;

a first leading edge detection circuit for detecting a
15 leading edge of a valid video signal region in the first phase data, and outputs a detection signal corresponding thereto;

a second leading edge detection circuit for detecting a leading edge of a valid video signal region in the second phase data, and outputs a detection signal corresponding thereto;

20 a first back porch detection circuit for detecting a first back porch period starting from the output signal from the multiplexer to the detection signal outputted from the first leading edge detection circuit;

a second back porch detection circuit for detecting a second
25 back porch period starting from the output signal from the

multiplexer to the detection signal outputted from the second leading edge detection circuit; and

a comparator for comparing the first back porch period and the second back porch period, and when the first back porch period is longer than the second back porch period, determining that head data in the valid video signal region in the video signal is not included in the first phase data, and outputting a signal for controlling the multiplexer to switch an output signal therefrom.

As described above, in the first aspect of the present invention, even if a head of video data is not included in first phase data under normal circumstances, a display can display every pixel by regarding a signal being delayed by one clock phase.

According to a second aspect of the present invention, in the first aspect of the present invention,

the first back porch detection circuit detects the first back porch period by using the number of clocks in the video signal, and

the second back porch detection circuit detects the second back porch period by using the number of clocks in the video signal.

As described above, in the second aspect of the present invention, correct counting can be achieved by using the number of dot clocks coming from an image signal source.

According to a third aspect of the present invention, in the first aspect of the present invention, further comprising a first minimum value retention circuit for inputting, into the

comparator, a minimum value of the first back porch periods
outputted from the first back porch detection circuit as another
first back porch period, and

a second minimum value retention circuit for inputting,
5 into the comparator, a minimum value of the second back porch
period outputted from the second back porch detection circuit as
another second back porch period.

As described above, in the third aspect of the present
invention, it is possible to deal with a case where a video signal
10 from an image signal source is such moving image that its back
porch period does not stay the same. Therefore, a display can
assuredly display every video signal.

A fourth aspect of the present invention is directed to a
video signal processing device for displaying, on a display, every
15 pixel in a video signal inputted from an image signal source, the
device comprising:

a clock delay circuit for receiving a reference signal, and
delays the reference signal by the odd number of clocks for output;

a multiplexer for selecting either the reference signal or
20 an output signal from the clock delay circuit for output;

an A/D converter for converting the video signal into a
digital signal for two-phase output as first phase data and second
phase data with reference to an output signal from the
multiplexer;

25 a leading edge detection circuit for detecting, in a

predetermined manner, a leading edge of a valid video signal region in either predetermined the first phase data or the second phase data, and outputs a detection signal corresponding thereto;

a back porch detection circuit for detecting a back porch
5 period starting from the output signal from the multiplexer to the detection signal outputted from the leading edge detection circuit;

a storage part for receiving the back porch period, and storing and outputting in a manner each corresponding to the
10 reference signal selected and outputted by the multiplexer and the output signal from the clock delay circuit; and

a comparator for outputting a control signal for controlling the multiplexer to switch a signal selected and outputted therefrom so that the storage part outputs a back porch
15 period each corresponding to the signal selected and outputted from the multiplexer, comparing the corresponding back porch periods outputted from the storage part with each other, and when the back porch period corresponding to the reference signal is equal to or shorter than the back porch period corresponding to
20 the output signal from the clock delay circuit, determining that head data in the valid video signal region in the video signal is included in the first phase data, and outputting the control signal again.

As described above, in the fourth aspect of the present
25 invention, a display can assuredly display every video signal with

such structure that a back porch period is stored and outputted in a manner corresponding to each state, and based on data outputted thereby, a comparator carries out its determination operation.

5 Also, in the fourth aspect of the present invention, a detection signal used therein is either first phase data or second phase data outputted from the A/D converter. Therefore, without using both data as the detection signal, the video signal processing device can be reduced in area for wiring on a substrate,
10 for example.

According to a fifth aspect of the present invention, in the fourth aspect of the present invention, the back porch detection circuit detects the back porch period by using the number of clocks in the video signal.

15 As described above, in the fifth aspect of the present invention, correct counting can be achieved by using the number of dot clocks coming from an image signal source.

A sixth aspect of the present invention is directed to a video signal processing device for displaying, on a display, every
20 pixel in a video signal inputted from an image signal source, the device comprising:

 a clock delay circuit for receiving a reference signal, and delays the reference signal by the odd number of clocks for output;

 a multiplexer for selecting either the reference signal or
25 an output signal from the clock delay circuit for output;

an A/D converter for converting the video signal into a digital signal for two-phase output as first phase data and second phase data with reference to an output signal from the multiplexer;

5 a leading edge detection circuit for detecting a leading edge of a valid video signal region in the first phase data, and outputs a detection signal corresponding thereto;

 a falling edge detection circuit for detecting a falling edge of a valid video signal region in the second phase data, and
10 outputting a detection signal corresponding thereto;

 a valid video period detection circuit for detecting a valid video period starting from the detection signal outputted from the leading edge detection circuit to the detection signal outputted from the falling edge detection circuit; and

15 a comparator for comparing a value half of an inputted horizontal resolution with the valid video period, and when the value half of the horizontal resolution is larger than the valid video period in value, determining that head data in the valid video signal region in the video signal is not included in the
20 first phase data, and outputting a signal for controlling the multiplexer to switch an output signal therefrom.

 As described above, in the sixth aspect of the present invention, a display can assuredly display every video signal with such structure that a comparator receives the number of pixels
25 detected by a valid video period detection circuit where receiving

a detection pulse each detected by a leading edge detection circuit and a falling edge detection circuit, and a value half of horizontal resolution from an image signal source connected to the present video signal processing device, and then carries
5 out its determination operation.

According to a seventh aspect of the present invention, in the sixth aspect of the present invention, the valid video period detection circuit detects the valid video period by using the number of clocks in the video signal.

10 As described above, in the seventh aspect of the present invention, correct counting can be achieved by using the number of dot clocks coming from an image signal source.

An eighth aspect of the present invention is directed to a video signal processing device for displaying, on a display,
15 every pixel in a video signal inputted from an image signal source, the device comprising:

a clock delay circuit for receiving a reference signal, and delays the reference signal by the odd number of clocks for output;

a multiplexer for selecting either the reference signal or
20 an output signal from the clock delay circuit for output;

an A/D converter for converting the video signal into a digital signal for two-phase output as first phase data and second phase data with reference to an output signal from the multiplexer;

25 a leading edge detection circuit for detecting a leading

edge of a valid video signal region in the second phase data, and
outputs a detection signal corresponding thereto;

a falling edge detection circuit for detecting a falling
edge of the valid video signal region in the first phase data,
5 and outputs a detection signal corresponding thereto;

a valid video period detection circuit for detecting a valid
video period starting from the detection signal outputted from
the leading edge detection circuit to the detection signal
outputted from the falling edge detection circuit; and

10 a comparator for comparing a value half of an inputted
horizontal resolution with the valid video period, and when the
value half of the horizontal resolution is smaller than the valid
video period in value, determining that head data in the valid
video signal region in the video signal is not included in the
15 first phase data, and outputting a signal for controlling the
multiplexer to switch an output signal therefrom.

As described above, in the eighth aspect of the present
invention, no matter what the data included in a video signal is
ON or OFF, a display can assuredly display every video signal with
20 such structure that a comparator receives the number of pixels
detected by a valid video period detection circuit where receiving
a detection pulse each detected by a leading edge detection
circuit and a falling edge detection circuit, and a value half
of horizontal resolution from an image signal source connected
25 to the present video signal processing device, and then carries

out its determination operation.

According to a ninth aspect of the present invention, in the eighth aspect of the present invention, the valid video period detection circuit detects the valid video period by using the
5 number of clocks in the video signal.

As described above, in the ninth aspect of the present invention, correct counting can be achieved by using the number of dot clocks coming from an image signal source.

A tenth aspect of the present invention is directed to a
10 video signal processing device for displaying, on a display, every pixel in a video signal inputted from an image signal source, the device comprising:

a clock delay circuit for receiving a reference signal, and delays the reference signal by the odd number of clocks for output;

15 a multiplexer for selecting either the reference signal or an output signal from the clock delay circuit for output;

an A/D converter for converting the video signal into a digital signal for two-phase output as first phase data and second phase data with reference to an output signal from the
20 multiplexer;

a first leading edge detection circuit for detecting a leading edge of a valid video signal region in the first phase data, and outputs a detection signal corresponding thereto;

a second leading edge detection circuit for detecting a
25 leading edge of a valid video signal region in the second phase

data, and outputs a detection signal corresponding thereto;

a first falling edge detection circuit for detecting a falling edge of the valid video signal region in the second phase data, and outputs a detection signal corresponding thereto;

5 a second falling edge detection signal for detecting a falling edge of the valid video signal region in the first phase data, and outputs a detection signal corresponding thereto;

a first valid video period detection circuit for detecting a first valid video period starting from the detection signal
10 outputted from the first leading edge detection circuit to the detection signal outputted from the first falling edge detection circuit;

a second valid video period detection circuit for detecting a second valid video period starting from the detection signal
15 outputted from the second leading edge detection circuit to the detection signal outputted from the second falling edge detection circuit; and

a comparator for comparing the first valid vide period and the second valid video period, and when the second valid video
20 period is longer than the first valid video period, determining that head data in the valid video signal region in the video signal is not included in the first phase data, and outputting a signal for controlling the multiplexer to switch an output signal therefrom.

25 As described above, in the tenth aspect of the present

invention, a display can assuredly display every video signal with such structure that a valid video period is detected but not a horizontal resolution.

According to an eleventh aspect of the present invention,
5 in the tenth aspect of the present invention,

the first valid video period detection circuit detects the first valid video period by using the number of clocks in the video signal, and

the second valid video period detection circuit detects the
10 second valid video period by using the number of clocks in the video signal

As described above, in the eleventh aspect of the present invention, correct counting can be achieved by using the number of dot clocks coming from an image signal source.

15 A twelfth aspect of the present invention is directed to a video signal processing device for displaying, on a display, every pixel in a video signal inputted from an image signal source, the device comprising:

an A/D converter for converting the video signal into a
20 digital signal for two-phase output as first phase data and second phase data with reference to an incoming reference signal;

a clock delay circuit for receiving the second phase data, and delays the second phase data by the odd number of clocks for output;

25 a first multiplexer for selecting either the first phase

data or an output signal from the clock delay circuit for output;
a second multiplexer for selecting either the second phase data or the first phase data for output
a first leading edge detection circuit for detecting a
5 leading edge of a valid video signal region in the first phase data, and outputs a detection signal corresponding thereto;
a second leading edge detection circuit for detecting a leading edge of a valid video signal region in the second phase data, and outputs a detection signal corresponding thereto;
10 a first back porch detection circuit for detecting a first back porch period starting from the reference signal to the detection signal outputted from the first leading edge detection circuit;
a second back porch detection circuit for detecting a second
15 back porch period starting from the reference signal to the detection signal outputted from the second leading edge detection circuit; and
a comparator for comparing the first back porch period and the second back porch period, and when the first back porch period
20 is longer than the second back porch period, determining that head data in the valid video signal region in the video signal is not included in the first phase data, and outputting a signal for controlling the first and second multiplexers to switch an output signal each therefrom simultaneously, wherein
25 right after activation, the first multiplexer selects the

first phase data for output, and the second multiplexer selects the second phase data for output.

As described above, in the twelfth aspect of the present invention, it is possible to deal with an image signal source
5 having higher resolution, and thus a display can assuredly display every video signal.

According to a thirteenth aspect of the present invention, in the twelfth aspect of the present invention,

the first back porch detection circuit detects the first
10 back porch period by using the number of clocks in the video signal, and

the second back porch detection circuit detects the second back porch period by using the number of clocks in the video signal.

As described above, in the thirteenth aspect of the present
15 invention, correct counting can be achieved by using the number of dot clocks coming from an image signal source.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram showing the structure of a video
20 signal processing device according to a first embodiment of the present invention.

FIGS. 2 are diagrams in assistance of explaining the operation of the video signal processing device according to the first embodiment of the present invention.

25 FIG. 3 is a block diagram showing the structure of a video

signal processing device according to a second embodiment of the present invention.

FIGS. 4 are diagrams in assistance of explaining the operation of the video signal processing device according to the
5 second embodiment of the present invention.

FIGS. 5 are diagrams showing the flow of data in a case where head data in a valid video signal region is outputted from the first phase of an A/D converter 3.

FIGS. 6 are diagrams showing the flow of data in a case where
10 the head data is outputted from the second phase of the A/D converter 3.

FIG. 7 is a block diagram showing the structure of a video signal processing device according to a third embodiment of the present invention.

15 FIG. 8 is a diagram in assistance of explaining the operation of the video signal processing device according to the third embodiment of the present invention.

FIGS. 9 are diagrams showing the relationship among a detection signal generated in a valid video period detection
20 circuit 17, first phase data 10, and second phase data 11.

FIG. 10 is a block diagram showing the structure of a video signal processing device according to a fourth embodiment of the present invention.

FIGS. 11 are diagrams in assistance of explaining the
25 operation of the video signal processing device according to the

fourth embodiment of the present invention.

FIG. 12 is a block diagram showing the structure of a video signal processing device according to a fifth embodiment of the present invention.

5 FIGS. 13 are diagrams in assistance of explaining the operation of the video signal processing device according to the fifth embodiment of the present invention.

FIG. 14 is a block diagram showing the structure of a video signal processing device according to a sixth embodiment of the
10 present invention.

FIGS. 15 are diagrams in assistance of explaining the operation of the video signal processing device according to the sixth embodiment of the present invention.

FIG. 16 is a block diagram showing the structure of a video
15 signal processing device according to a seventh embodiment of the present invention.

FIG. 17 is a block diagram showing the structure of a conventional video signal processing device.

FIG. 18 is a diagram in assistance of explaining the
20 operation of an A/D converter which carries out two-phase processing.

FIG. 19 is a diagram in assistance of explaining the operation of the conventional video signal processing device in a case where a head of video data is outputted from the A/D
25 converter as the first phase data.

FIGS. 20 are diagram in assistance of explaining the operation of the conventional video signal processing device in a case where the head of video data is outputted from the A/D converter as the second phase data.

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BEST MODE FOR CARRYING OUT THE INVENTION

(First Embodiment)

FIG. 1 is a block diagram showing the structure of a video signal processing device according to a first embodiment of the present invention. In FIG. 1, the present video signal processing device includes a one-clock delay circuit 1 where receiving the reference signal 9 and outputting a one-clock-delayed signal, a multiplexer 2 for receiving the output signal from the one-clock delay circuit 1 and the reference signal 9, the A/D converter 3 where receiving an output signal from the multiplexer 2 and the video signal 24 and carrying out the two-phase processing, first and second leading edge detection circuits 4 and 5 for detecting a leading edge of an output signal from the A/D converter 3, first and second back porch detection circuits 6 and 7 for receiving signals from each corresponding first and second leading edge detection circuits 4 and 5 and the output signal from the multiplexer 2, and a comparator 8 where receiving signals each from the first and second leading edge detection circuits 6 and 7 and outputting a control signal 12 for the multiplexer 2. Described below is the operation of such structured video signal

processing device.

In FIG. 1, the reference signal 9 provided from an image signal source connected to the present video signal processing device is applied to both the multiplexer 2 and the one-clock delay circuit 1. The reference signal 9 is generally a horizontal synchronizing signal from the image signal source, but is not necessarily restricted thereto.

The one-clock delay circuit 1 delays the received reference signal 9 by one clock for output to the multiplexer 2. To be specific, the one-clock delay circuit 1 delays the reference signal 9 by one dot clock, i.e., one pixel, out of those from the image signal source.

The multiplexer 2 selects either the received reference signal 9 or an output signal from the one-clock delay circuit 1 for output. Herein, once the control signal 12 was applied from the comparator 8, the multiplexer 2 switches from one received signal which has been selected into the other for output. It is now assumed that the multiplexer 2 has been selecting, for output, the received reference signal 9 but not the output signal from the one-clock delay circuit 1. Thereafter, once the control signal 12 was provided from the comparator 8, the multiplexer 2, in its switching operation, stops outputting the reference signal 9 which has been selected, and starts outputting the output signal from the one-clock delay circuit 1. Herein, right after the present video signal processing device is activated, the

multiplexer 2 presumably selects the reference signal 9 for output. The output signal from the multiplexer 2 is applied to the A/D converter 3.

The A/D converter 3 goes through the two-phase processing
5 after receiving the video signal 24 and the output signal from the multiplexer 2. In detail, with reference to the signal outputted from the multiplexer 2, the A/D converter 3 subjects the video signal 24 to A/D conversion, and then carries out the two-phase conversion so as to simultaneously output the first
10 phase data 10 and the second phase data 11. These digital data is provided to a digital data processing device (not shown) provided in a stage subsequent to the A/D converter 3 for signal processing, and then displayed on a display.

The digital data outputted from the A/D converter 3, that
15 is, the first phase data 10 and the second phase data 11 is provided to the first and second leading edge detection circuits 4 and 5, respectively. As for the received first phase data 10 and the second phase data 11, the first and second leading edge detection circuits 4 and 5 each detect a leading edge of a valid video signal
20 region in the video signal 24 which has been applied to the A/D converter 3. For such positional detection of the leading edge of the valid video signal region, utilized is a blanking period coming from a general image signal source being black from the reference signal 9 to the valid video region. That is, the leading
25 edge of the valid video signal region can be easily detected by

detecting a period starting from the reference signal 9 till the video signal rises.

Herein, when the head data in the valid video signal region is in the pedestal level, the leading edge of the valid video signal region cannot be detected with correctness. In such case, however, the head data in the valid video signal region is always one or more pixels short. Therefore, no such problem occurs that the display where pixels displayed thereon are fixed in number cannot display every data provided from the image signal source connected to the present video signal processing device.

With the leading edge thus detected, the first and second leading edge detection circuits 4 and 5 input the leading edge in a form of pulse signal to the first and second back porch detection circuits 6 and 7, respectively. The first and second back porch detection circuits 6 and 7 then detect a back porch period between the signal outputted from the multiplexer 2 and the leading edge of the valid video signal region detected by the first and second leading edge detection circuits 4 and 5, respectively. Typically, the first and second leading edge detection circuits 4 and 5 each include a counter circuit, and count the back porch period by referring to the number of dot clocks from the image signal source. As such, the number of dot clocks from the image signal source helps the first and second leading edge detection circuits 4 and 5 counting in a correct manner.

As described in the foregoing, when the head data in the

valid video signal region is in the pedestal level, the leading edge of the valid video signal region each detected by the first and second leading edge detection circuits 4 and 5 does not always coincide with the actual leading edge of the valid video signal region. The back porch period is thus defined as a period starting from a leading edge of a signal outputted from the multiplexer 2 to a head position of data in a valid video signal region excepting data in the black level.

The back porch periods detected by the first and second back porch detection circuits 6 and 7 are both provided to the comparator 8. The comparator 8 then outputs the control signal 12 based on a result obtained through determination logic, which will be later described. In response to the control signal 12, the multiplexer 2 switches, for output, between the output signal from the one-clock delay circuit 1 and the reference signal 9. If the comparator 8 decided not to output the control signal 12 in accordance with the result obtained through the determination logic which will be later described, the multiplexer 2 surely does not go through its switching operation.

Next, it is described the determination operation of the comparator 8 in detail by referring to FIGS. 2. FIGS. 2 are time charts showing the relationship between the reference signal 9 and the output signals from the first and second leading edge detection circuits 4 and 5. Specifically, FIG. 2(a) shows a case where the head data (data on the left end on the display) in the

valid video signal region is outputted from the first phase of the A/D converter 3, while FIG. 2(b) shows a case where the head data is outputted from the second phase of the A/D converter 3.

In the foregoing, it is already described that the back
5 porch period is a period detected starting from the pulse position of the signal outputted from the multiplexer 2 to the head data in the valid video signal region. It is now assumed that a back porch number is a value obtained by counting the number of dots (the number of clocks) in the back porch period. In FIGS. 2, the
10 back porch number for the output signal from the leading edge detection circuit 4 is denoted by BP1, and the back porch number for the output signal from the leading edge detection circuit 5 as BP2.

In FIG. 2(a), as described above, the head data is included
15 in the first phase data 10. Therefore, for the output signal from the leading edge detection circuit 4 where receiving the first phase data 10, the back porch number BP1 always shows such relationship with the back porch number BP2 as an equation (1) next below.

20
$$BP1 \leq BP2 \quad \dots (1)$$

This is because, if video signal data next to the head data, i.e., the data at the start of the second phase data 11, is not in the black level, BP1 and BP2 become equal to each other in value, and if in the black level, BP2 never fails to be larger than BP1.

25 When the above equation (1) is satisfied, the comparator

8 does not output the control signal 12 to the multiplexer 2. Thus, the multiplexer 2 keep outputting the reference signal 9 without its switching operation. Once received the reference signal 9, the A/D converter 3 becomes possible to retain a state that the head data in the valid video signal region is always outputted from the first phase data. Therefore, once retaining such state that the head data is always outputted from the first phase data, the present video signal processing circuit basically has no need to operate thereafter.

10 In FIG. 2(b), on the other hand, the head data in the valid video signal region is included in the second phase data 11. Therefore, for the output signal from the leading edge detection circuit 5 where receiving the second phase data 11, the back porch number BP2 always shows such relationship with the back porch number BP1 as an equation (2) next below.

$$BP1 > BP2 \quad \dots (2)$$

This is because, since the head data is included in the second phase data 11, the first phase data 10 in the same phase is surely the black data, and the back porch number BP2 never fails to be smaller than the back porch number BP1.

When the above equation (2) is satisfied, the comparator 8 outputs the control signal 12 to the multiplexer 2 so as to bring the multiplexer 2 to select the signal from the one-clock delay circuit 1. In response to the control signal 12, the multiplexer 2 switches its output signal. Specifically, the multiplexer 2

selects the signal from the one-clock delay circuit 1 for output to the A/D converter 3. Once the signal from the one-clock delay circuit 1 was selected, the A/D converter 3 starts regarding a signal whose phase is delayed by one clock as a reference, retaining the state that the head data in the valid video signal region is always outputted from the first phase data. This is because, as described in the foregoing, if the head data in the valid video signal region is outputted from the first phase data, the comparator 8 does not output the control signal 12 to the multiplexer 2, and accordingly the multiplexer 2 does not switch its output signal. This is the reason why, as described above, the present video signal processing circuit basically has no need to operate once such state is retained that the head data is always outputted from the first phase data.

Note herein that, even if the head data in the valid video signal region is started to be outputted from the second phase data in operation, the present video signal processing device can retain the state that the head data in the valid video signal region is always outputted from the first phase data. This is because, the comparator 8 outputs the control signal 12 to the multiplexer 2 through such determination operation described in the foregoing, and thus the multiplexer 2 switches its output signal into the reference signal 9.

As described in the foregoing, even if a head of video data is not in the first phase output data, the video signal processing

device of this embodiment is capable of displaying every pixel on a display by regarding a signal whose phase is delayed by one clock as a reference.

Note herein that, the video signal processing device of this
5 embodiment can be in such structure that the first and second leading edge detection circuits 4 and 5 are replaced with first and second falling edge detection circuits, respectively. In such structure, the first and second back porch detection circuits 6 and 7 operate to detect a period including both the back porch
10 period and the valid video signal period. Even with such alternative structure, the video signal processing device of this embodiment can operate in a similar manner.

Further, the one-clock delay circuit 1 in the present video signal processing device may be a three-clock delay circuit or
15 a five-clock delay circuit. That means, the one-clock delay circuit 1 may be any type of circuit as far as the reference signal 9 is delayed by the odd number of clocks therein. Still further, although an A/D converter described in this embodiment is the one carrying out the two-phase processing, an A/D converter carrying
20 out four-phase processing or six-phase processing can easily operate in a similar manner.

(Second Embodiment)

FIG. 3 is a block diagram showing the structure of a video signal processing device according to a second embodiment of the
25 present invention. In FIG. 3, the present video signal processing

device is almost identical in structure to the above-described video signal processing device of the first embodiment. The present video signal processing device is not provided with the second leading edge detection circuit 5 and the second back porch detection circuit 7 in FIG. 1. And therein, the first leading edge detection circuit 4 in FIG. 1 is replaced with a leading edge detection circuit 40, and the first back porch detection circuit 6 with a back porch detection circuit 60, and a storage part 13 is additionally provided. These are the differences from the above-described video signal processing device of the first embodiment. Thus, in the present video signal processing device, any constituent identical to that in the video signal processing device of the first embodiment is under the same reference numeral, and is not described again. Herein, a comparator 15 is different from the comparator 8 in reference numeral since receiving a signal different from the one thereto.

In FIG. 3, in an initial state, the multiplexer 2 selects the reference signal 9 for output to the A/D converter 3 without any change. In the same manner as described above, with reference to the signal outputted from the multiplexer 2, the A/D converter 3 subjects the video signal 24 to A/D conversion and then carries out the two-phase processing so that the video signal 24 is outputted as the first phase data 10 and the second phase data 11. The first phase data 10 is provided to the leading edge detection circuit 40. The leading edge detection circuit 40 then

detects a leading edge of a valid video signal region in the video signal 24. A result obtained by the detection is provided to the back porch detection circuit 60. The back porch detection circuit 60 detects a back porch period between a leading edge of the signal
5 (herein, the reference signal 9) outputted from the multiplexer 2 and a leading edge of the valid video signal region outputted from the leading edge detection circuit 40. The back porch period thus detected is provided to the storage part 13. The storage part 13 stores the period, and keeps outputting the period to the
10 comparator 15 at predetermined intervals.

When detecting an input only of the period, the comparator 15 outputs the control signal 12 to the multiplexer 2 so as to bring the multiplexer 2 to change its output signal to an output signal from the one-clock delay circuit 1. The reason for the
15 comparator 15 carrying out such operation is to have the storage part 13 store the back porch period starting from the leading edge of the reference signal 9, and then have the storage part 13 store also the back porch period starting from the leading edge of the output signal from the one-clock delay circuit 1.

20 In response to the control signal 12 from the comparator 15, the multiplexer 2 switches into the output signal from the one-clock delay circuit 1 for output to the A/D converter 3. The A/D converter 3 regards the received signal as a reference, and subjects the video signal 24 to A/D conversion then carries out
25 the two-phase conversion. In a similar manner to the above, the

leading edge detection circuit 40 detects the leading edge of the valid video signal region in the video signal 24. Also, the back porch detection circuit 60 detects the back porch period in a similar manner to the above. The back porch period thus detected
5 is provided to the storage part 13. The storage part 13 then provides both the received back porch period and the stored back porch period to the comparator 15. Herein, the received back porch period may be once stored into the storage part 13.

When detecting an input of those two back porch periods,
10 the comparator 8 determines whether or not outputting the control signal 12 again based on a result obtained through determination logic, which will be later described. If the control signal 12 is inputted, the multiplexer 2 switches its output signal between the output signal from the one-clock delay circuit 1 and the
15 reference signal 9.

Next, it is described the determination operation of the comparator 8 in detail by referring to FIGS. 4 to 6. FIGS. 4 are time charts showing the relationship between the reference signal 9 and the output signal from the storage part 13. Specifically,
20 FIG. 4(a) shows a case where head data (data on the left end on the display) in the valid video signal region is outputted from the first phase of the A/D converter 3, while FIG. 4(b) shows a case where the head data is outputted from the second phase of the A/D converter 3.

25 FIGS. 5 are time charts showing the flow of data for a case



where the head data in the valid video signal region is outputted from the first phase of the A/D converter 3. Specifically, FIG. 5(a) shows a case where the reference signal 9 is applied to the A/D converter 3 without being delayed, while FIG. 5(b) shows a case where the reference signal 9 is delayed by one clock before applied to the A/D converter 3.

FIGS. 6 are time charts showing the flow of data for a case where the head data is outputted from the second phase of the A/D converter 3. Specifically, FIG. 6(a) shows a case where the reference signal 9 is applied to the A/D converter 3 without being delayed, while FIG. 6(b) shows a case where the reference signal 9 is delayed by one clock before applied to the A/D converter 3.

Similarly to the above-described first embodiment, also in this embodiment, the back porch number is presumed to be a value obtained by counting the number of dots (the number of clocks) in the back porch period. In FIGS. 4 to 6, in the case that the reference signal 9 is applied to the A/D converter 3 without being delayed, the back porch number in the output signal from the storage part 13 is denoted by M1. In the case that the reference signal 9 is applied to the A/D converter 3 after being delayed by one clock, the back porch number in the output signal from the storage part 13 is denoted by M2.

In FIG. 4(a), in the case that the reference signal 9 is delayed by one clock before inputted to the A/D converter 3, the leading edge of the output signal from the leading edge detection

circuit 40 comes later by one clock or more compared with the case that the reference signal 9 is inputted to the A/D converter 3 without being delayed. In detail, as will be described, if the head data of the video signal is accompanied by data not in the black level (ON data), the leading edge of the output signal from the leading edge detection circuit 40 comes later only by one clock in the case that the reference signal 9 is delayed only by one clock. If the data is in the black level, the leading edge thereof comes later by more clocks. Herein, since the output signal from the multiplexer 2 is delayed by one clock, the relationship between the back porch numbers M1 and M2 can be expressed by an equation (3) next below.

$$M1 \leq M2 \quad \dots (3)$$

Next below, it is described in detail why such relationship as expressed by the above equation (3) is established by referring to FIGS. 5(a) and (b). In FIGS. 5(a) and (b), t1 to t7 each indicate a time, and arrows therein schematically show the two-phase processing in the A/D converter 3. Moreover, blackened circle and square denote data in the black level in the back porch, and *a* to *d* denote video data in the valid video signal region. Herein, the video data *a* located immediately after the leading edge of the video signal 24 is assumed not in the black level. This is because, if the data is in the black level, such problem to be solved by the present video signal processing device that a display cannot display every data does not occur as described

in the foregoing.

In FIG. 5(a), the leading edge of the output signal from the multiplexer 2 is at time t_1 . Thus, in response to the video signal 24 inputted at time t_1 , the A/D converter 3 starts the two-phase processing. To be specific, once two types of data was inputted, the A/D converter 3 keeps simultaneously outputting the received data until completely receiving next two data. Accordingly, the A/D converter 3 outputs the data denoted by the blackened circle and square at time t_3 , and outputs the video data a and b at time t_5 . In the video signal processing device of this embodiment, only the first phase data 10 goes to the leading edge detection circuit 40. Thus, the leading edge of the output signal from the leading edge detection circuit 40 is found at time t_5 , and it is known that the back porch number M_1 between times t_1 and t_5 is 4. Note herein that, since the video data a is not in the black level, M_1 is determined regardless of the arrangement of the video data.

In FIG. 5(b), since the reference signal 9 is delayed by one clock, the leading edge of the output signal from the multiplexer 2 is at time t_2 . Therefore, the A/D converter 3 starts the two-phase processing in response to the video signal 24 inputted at time t_2 , outputs the data denoted by the blackened square and the video data a at time t_4 , and outputs the video data b and c at time t_6 . In the video signal processing device of this embodiment, only the first phase data 10 goes to the leading edge

detection circuit 40. Thus, the leading edge of the output signal from the leading edge detection circuit 40 is found at time t_6 . It is thus known that the back porch number M2 between times t_2 and t_6 is 4. Note herein that, the video data b or data following thereto may be in the black level. If this is the case, the leading edge of the output signal from the leading edge detection circuit 40 will be found later than time t_6 . Accordingly, M2 becomes 4 or larger and never fails to be equal to or larger than M1 in value. Therefore, the relationship such as the above equation (3) is thus satisfied.

Next, in FIG. 4(b), in the case that the reference signal 9 is delayed by one clock before inputted to the A/D converter 3, the leading edge of the output signal from the leading edge detection circuit 40 always comes before compared with the case that the reference signal 9 is inputted to the A/D converter 3 without being delayed. This is because, as will be described later, when the two-phase processing is carried out with respect to the one-clock delayed signal, the head data of the video signal which has been included in the second-phase data 11 is started to be included in the first-phase data 10. Therefore, the relationship between the back porch numbers M1 and M2 can be expressed as an equation (4) next below.

$$M1 > M2 \quad \dots (4)$$

It is now described in detail why such relationship as the above equation (4) is established by referring to FIGS. 6(a) and

(b). In FIGS. 6(a) and (b), t1 to t8 each denote a time, and arrows therein schematically show the two-phase processing in the A/D converter 3. The blackened circle, square, and triangle indicate the data in the black level in the back porch, and *a* to *d* indicate the video data in the valid video signal region. As already described in the foregoing, the video data *a* immediately after the leading edge of the video signal 24 is not in the black level.

In FIG. 6(a), the leading edge of the output signal from the multiplexer 2 is at time t1. Thus, in response to the video signal 24 inputted at time t1, the A/D converter 3 starts the two-phase processing. Thereafter, at time t3, the A/D converter 3 outputs data denoted by the blackened circle and square, at time t5, outputs data denoted by the blackened triangle and the video data *a*, and at time t7, outputs the video data *b* and *c*. In the video signal processing device of the present invention, only the first phase data 10 goes to the leading edge detection circuit 40. Thus, the leading edge of the output signal from the leading edge detection circuit 40 is found at time t7, and it is known that the back porch number M1 between times t1 and t7 is 6. Note herein that, the video data *b* or the video data *b* with the data following thereto may be in the black level. In such case, the leading edge of the output signal from the leading edge detection circuit 40 will be found later than time t7.

In FIG. 6(b), since the reference signal 9 is delayed by one clock, the leading edge of the output signal from the

multiplexer 2 is at time t_2 . Thus, in response to the video signal 24 inputted at time t_2 , the A/D converter 3 starts the two-phase processing, outputs data denoted by the blackened square and triangle at time t_4 , and outputs the video data a and b at time 5 t_6 . Since only the first phase data 10 goes to the leading edge detection circuit 40 in the video signal processing device of this embodiment, the leading edge of the output signal from the leading edge detection circuit 40 is found at time t_6 . It is thus known that the back porch number M_2 between times t_2 and t_6 is 4, and 10 rendering M_2 always smaller than M_1 in value. As such, such relationship as the above equation (4) is established.

When the above equation (3) is satisfied, the comparator 8 again outputs the control signal 12 to the multiplexer 2. In response thereto, the multiplexer 2 again goes through its 15 switching operation so as to output the reference signal 9. Once the reference signal 9 was inputted, the A/D converter 3 can retain a state that the head data in the valid video signal region is outputted always from the first phase data. Therefore, similarly in the first embodiment, the present video signal 20 processing circuit basically has no need to operate once such state that the head data is outputted always from the first phase data is retained.

When the above equation (4) is satisfied, the comparator 8 does not output the control signal 12 to the multiplexer 2 so 25 as to let the multiplexer 2 keep selecting the signal from the



one-clock delay circuit 1. With no control signal 12 inputted, the multiplexer 2 keeps selecting the signal from the one-clock delay circuit 1 for output to the A/D converter 3. Once the signal from the one-clock delay circuit 1 was selected, the A/D converter
5 3 regards a signal whose phase is delayed by one clock as a reference, and thus, the head data in the valid video signal region is assured to be always outputted from the first phase data. As such, similarly to the case in the first embodiment, the present video signal processing circuit has no need to operate once such
10 state that the head data is always outputted from the first phase data is retained.

Note herein that, even if the head data in the valid video signal region is started to be outputted from the second phase data in operation, similarly to the first embodiment, the present
15 video signal processing device can retain the state that the head data in the valid video signal region is always outputted from the first phase data.

As described in the foregoing, according to the video signal processing device of the present invention in which a back porch
20 period outputted from the back porch detection circuit 60 is stored in the storage part 13, and outputted to the comparator 15 for determination operation therein based on the data, a display can assuredly display every video signal thereon.

Further, compared with the video signal processing devices
25 of the above-described first embodiment and of the later-

described embodiments, the video signal processing device of this embodiment does not use the second phase data 11 outputted from the A/D converter 3 as a detection signal. Therefore, in the present video signal processing device, wiring on a substrate can
5 be reduced in area, for example.

Herein, although the first phase data 10 is used as the detection signal in this embodiment, the second phase data 11 can surely be used. Moreover, the video signal processing device of this embodiment can be provided with a falling edge detection
10 circuit instead of the leading edge detection circuit 40. If this is the case, the back porch detection circuit 60 operates to detect a period including both the back porch period and the valid video signal period. In such alternative structure, the video signal processing device of this embodiment can operate in a similar
15 manner.

Still further, similarly to the case in the first embodiment, the one-clock delay circuit 1 may be any type of circuit as far as the reference signal 9 is delayed by the odd number of clocks therein. Also, the A/D converter 3 may be the one carrying out
20 four-phase processing or six-phase processing, which can easily operate in a similar manner.

(Third Embodiment)

FIG. 7 is a block diagram showing the structure of a video signal processing device according to a third embodiment of the
25 present invention. In FIG. 7, the present video signal processing

device is almost identical in structure to the above-described video signal processing device of the second embodiment in FIG. 3. The present video signal processing device is not provided with the back porch detection circuit 60 and the storage part 13 in FIG. 3, but is newly provided with a falling edge detection circuit 16 and a valid video signal period detection circuit 17. These are the differences from the above-described video signal processing device of the second embodiment. Thus, in the present video signal processing device, any constituent identical to that in the video signal processing device of the second embodiment is under the same reference numeral, and is not described again. Herein, a comparator 18 is different from the comparator 15 in reference numeral since receiving a signal different from the one thereto. Described next below is the operation of such structured present video signal processing device with reference to FIGS. 8 and 9.

First, once the first phase data 10 was inputted from the A/D converter 3, the leading edge detection circuit 40 detects a position where the first phase data 10 first rises with reference to a pulse of an output signal from the multiplexer 2. A result obtained by the detection is outputted in a form of pulse signal as shown in FIG. 8.

On the other hand, in response to the second phase data 11 from the A/D converter 3, the falling edge detection circuit 16 detects a position where the second phase data 11 falls last with

reference to a pulse position of the output signal from the multiplexer 2. The result obtained thereby is outputted in such form of pulse signal as shown in FIG. 8.

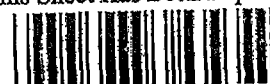
The signals outputted from the leading edge detection
5 circuit 40 and the falling edge detection circuit 16 go to the valid video signal period detection circuit 17. From those signals, the valid video signal period detection circuit 17 generates a valid video signal detection signal therein as shown in FIG. 8. Moreover, the valid video signal period detection
10 circuit 17 includes a counter circuit, and counts the above valid video period detection signal for pulse width on the basis of the number of dot clocks from the image signal source, and detects the number of pixels included in the valid video signal processing period. As such, the number of dot clocks from the image signal
15 source helps the valid video period detection circuit 17 counting in a correct manner. Note herein that, by the two-phase processing carried out in the A/D converter 3, the number of pixels is reduced to half of that in the valid video period for the actual video signal 24.

20 The comparator 18 receives the number of pixels included in the valid video signal period detected by the valid video period detection circuit 17. The comparator 18 also receives, from a value output part which is not shown, a value half of the horizontal resolution in the image signal source connected to the present
25 video signal processing device. Here, the horizontal resolution

in the image signal source can be easily calculated from frequencies of a horizontal synchronizing signal and a vertical synchronizing signal unique to the image signal source. Based on a result obtained by subjecting each received value to a
5 predetermined determination logic, the comparator 18 outputs the control signal 12 to the multiplexer 2. In response to the control signal 12, the multiplexer 2 switches its output signal between the output signal from the one-clock delay circuit 1 and the reference signal 9. Herein, if the comparator⁸ decided not to
10 output the control signal 12 according to the result obtained by the determination logic which will be later described, the multiplexer 2 surely does not go through its switching operation.

Next, it is described in detail the determination operation of the comparator⁸ by referring to FIGS. 9. FIGS. 9 are time
15 charts showing the relationship among the detection signal generated in the valid video period detection circuit 17, the first phase data 10, and the second phase data 11. Specifically, FIG. 9(a) shows a case where head data (data on the left end on the display) in the valid video signal region is outputted from
20 the first phase of the A/D converter 3, while FIG. 9(b) shows a case where the head data is outputted from the second phase of the A/D converter 3.

In FIGS. 9, *a* to *t* denote data included in the video signal
24 provided to the A/D converter 3. For convenience, each of *a*
25 to *t* is assumed to be ON. In this embodiment, needless to say,



the data included in the video signal 24 may be in the black level.

First, as shown in FIG. 9(a), head data (data on the left end on the display) *a* in the valid video signal region is included in the first phase data 10. Thus, the data *b* which is the second
5 from the head is included in the second phase data 11 at the same phase position as *a* in the first phase data. In this manner, the A/D converter 3 subjects 20 pieces of data from data *a* to data *t* to the two-phase processing.

The leading edge and the falling edge of the detection
10 signal generated in the valid video period detection circuit 17 coincide with the leading edge of the first phase data 10 and the falling edge of the second phase data 11, respectively. Accordingly, the data *a* to data *t* fit in a range of a pulse width of the detection signal generated in the valid video period
15 detection circuit 17. If this is the case, as shown in FIG. 8(a), such relationship as an equation (5) is established between the number of pixels detected by the valid video period detection circuit 17 and the horizontal resolution.

$$\text{Detected Number of Pixels} = \text{Horizontal Resolution} / 2 \dots (5)$$

20 When the above equation (5) is satisfied, the comparator 8 does not output the control signal 12 to the multiplexer 2. The multiplexer 2 thus outputs the reference signal 9 without going through its switching operation. Once the reference signal 9 was inputted, the A/D converter 3 can retain such state that the head
25 data in the valid video signal region is outputted always from



the first phase data. Accordingly, similarly to the case in the first embodiment, the present video signal processing circuit basically has no need to operate once such state that the head data is always outputted from the first phase data is retained.

5 Next, as shown in FIG. 9(b), the head data (data on the left end of the display) *a* in the valid video signal region is included in the second phase data 11. Thus, the data *b* second from the head is included in the second phase data 11 at a position having the one-clock-delayed phase relationship with the position of *a*
10 in the first phase data. As such, the A/D converter 3 subjects 20 pieces of data from data *a* to data *t* to the two-phase processing.

Here, the leading edge and the falling edge of the detection signal generated in the valid video period detection circuit 17 coincide with the leading edge of the first phase data 10 and the
15 falling edge of the second phase data 11, respectively. Accordingly, the phase of the data *a* which is the head data in the second phase data 11 is delayed by one clock from the leading edge of the first phase data 10, while the phase of the data *t* which is the last data in the first phase data 10 is delayed by
20 one clock from the falling edge of the second phase data 11. Thus, neither data fits in the range of the pulse width of the detection signal generated in the valid video period detection circuit 17. If so, as shown in FIG. 8(a), the number of pixels detected by the valid video period detection circuit 17 and the horizontal
25 resolution has such relationship as an equation (6) next below.



Detected Number of Pixels = (Horizontal Resolution/2) -

1 ... (6)

When the above-equation (6) is satisfied, the comparator
18 8 outputs the control signal 12 to the multiplexer 2 so as to bring
5 the multiplexer 2 to select a signal from the one-clock delay
circuit 1. In response to the control signal 12, the multiplexer
2 switches its output signal. To be specific, the multiplexer
2 selects a signal from the one-clock delay circuit 1 for output
to the A/D converter 3. Once the signal from the one-clock delay
10 circuit 1 was selected, the A/D converter 3 regards a one-
clock-delayed signal as a reference, retaining the state that the
head data in the valid video signal region is always outputted
from the first phase data. Therefore, similar to the case in the
first embodiment, the present video signal processing circuit
15 basically has no need to operate once the state that the head data
is always outputted from the first phase data is retained.

Note herein that, even if the head data in the valid video
signal region is started to be outputted from the second phase
data in operation, similarly to the case in the first embodiment,
20 the present video signal processing device can retain the state
that the head data in the valid video signal region is always
outputted from the first phase data.

As described in the foregoing, according to such structured
video signal processing device of the present invention that the
25 valid video period detection circuit 17 where receiving pulses



detected by the leading edge detection circuit 40 and the falling edge detection circuit 16 detects the number of pixels in the valid video period, and the comparator 18 receives the number of pixels and a value half of the horizontal resolution for comparison, a display can assuredly display every video signal thereon.

Note herein that, although each of the video data a to t in the valid video signal region in the video signal 24 is assumed to be ON in this embodiment, the present video signal processing device operates in a similar manner to the above if only the data a and t is ON. Further, the one-clock delay circuit 1 may be any type of circuit as far as the reference signal 9 is delayed by the odd number of clocks therein. Still further, the A/D converter 3 may be the one carrying out four-phase processing or six-phase processing, which can easily operate in a similar manner.

(Fourth Embodiment)

FIG. 10 is a block diagram showing the structure of a video signal processing device according to a fourth embodiment of the present invention. In FIG. 10, the present video signal processing device is almost identical in structure to the above-described video signal processing device of the third embodiment in FIG. 7. Thus, constituents in the present video signal processing device are the same as those in the video signal processing device of the third embodiment, and thus are under the same reference numerals and not described again. Note that, in

FIG. 7, the leading edge detection circuit 40 receives the first phase data 10 and the falling edge detection circuit 16 receives the second phase data 11, but in the present video signal processing device, the leading edge detection circuit 40 receives
5 the second phase data 11 and the falling edge detection circuit 16 receives the first phase data 10. Described below is the reason for such differences.

As described in the foregoing, in the video signal processing device of the third embodiment, the valid video signal
10 in the video signal 24 provided to the A/D converter 3 needs to be risen at both ends (i.e., the data needs to be ON). For example, in FIG. 9(a), with the head data *a* being OFF (i.e., data in the black level), the detection signal generated in the valid video period detection circuit 17 is less than a half of the horizontal
15 resolution in the image signal source. Thus, the comparator 18 outputs the control signal 12 so as to bring the multiplexer 2 to switch its outputs.

However, even if the output of the multiplexer 2 is switched, the detection signal generated in the valid video period detection
20 circuit 17 remains less than a half of the horizontal resolution in the image signal source. As a result, the comparator 18 again outputs the control signal 12 so as to bring the multiplexer 2 to switch its output. Consequently, the comparator 18 falls into an endless loop in operation.

25 As such, with such structured video signal processing

device of the third embodiment, as described above, the video signal 24 needs to be conditionally restricted to be ON at both ends. If not conditionally restricted, the video signal processing device needs to be additionally provided with a
5 constituent to detect whether the comparator 18 falls into the above-described endless loop, rendering the circuit complicated and the cost increased.

Therefore, with the present video signal processing device of this embodiment structured as shown in FIG. 10, such problem
10 of falling into the endless loop in the video signal processing device of the third embodiment can be easily cleared. Next below, the operation of the present video signal processing device is described with reference to FIGS. 11.

FIGS. 11 are time charts showing the relationship among the
15 detection signal generated in the valid video period detection circuit 17, the first phase data 10, and the second phase data 11. Specifically, FIG. 11(a) shows a case where the head data (data displayed on the left end on the display) in the valid video signal region is included in the first phase data 10 from the A/D
20 converter 3, while FIG. 11(b) shows a case where the head data is included in the second phase data from the A/D converter 3.

In FIGS. 11, *a* to *t* denote the data included in the video signal 24 provided to the A/D converter 3. Herein, for convenience, each of the data *a* to *t* is assumed to be ON. In this
25 embodiment, the case that the video signal 24 includes data in

the black level will be described later.

First, in the case as shown in FIG. 11(a), the head data (data displayed on the led end on the display) *a* in the valid video signal region is included in the first phase data 10. Therefore, the data *b* second from the head is included in the second phase data 11 at the same phase position as the first phase data *a*. As such, the A/D converter 3 subjects 20 pieces of data from data *a* to data *t* to the two-phase processing.

The leading edge and the falling edge of the detection signal generated in the valid video period detection circuit 17 coincide with the leading edge of the second phase data 11 and the falling edge of the first phase data 10, respectively. Accordingly, the data *a* to data *t* fit in a range of the pulse width of the detection signal generated in the valid video period detection circuit 17. If this is the case, as shown in FIG. 11(a), such relationship as an equation (7) is established between the number of pixels detected by the valid video period detection circuit 17 and the horizontal resolution.

$$\text{Detected Number of Pixels} = \text{Horizontal Resolution}/2 \dots (7)$$

When the above equation (7) is satisfied, the comparator 8 outputs the control signal 12 to the multiplexer 2 so as to bring the multiplexer 2 to select the reference signal 9. In response to the control signal 12, the multiplexer 2 selects the reference signal 9 corresponding to the control signal for output to the A/D converter 3. Once receiving the reference signal 9, the A/D



converter 3 can retain a state that the head data in the valid video signal region is always outputted from the first phase data. Therefore, once retaining the state that the head data is always outputted from the first phase data, similar to the case in the first embodiment, the present video signal processing circuit
5 basically has no need to operate thereafter.

Next, in the case as shown in FIG. 11(b), the head data (data displayed on the left end on the display) *a* in the valid video signal region is included in the second phase data 11.
10 Accordingly, the data *b* second from the head is included in the second phase data 11 at a position 11 having the one-clock-delayed phase relationship with the position of *a* in the first phase data. As such, the A/D converter 3 subjects 20 pieces of data from data *a* to data *t* to the two-phase processing.

15 The leading edge and the falling edge of the detection signal generated in the valid video period detection circuit 17 coincide with the leading edge of the second phase data 11 and the falling edge of the first phase data 10, respectively. Accordingly, the data *a* being the head data in the second phase
20 data 11 and the data *t* being the last data in the first phase data 10 both fit in a range of the pulse width of the detection signal generated in the valid video period detection circuit 17. If this is the case, as shown in FIG. 11(b), such relationship as an equation (8) is established between the number of pixels detected
25 by the valid video period detection circuit 17 and the horizontal

resolution.

$$\text{Detected Number of Pixels} = (\text{Horizontal Resolution}/2) + 1 \dots (8)$$

Since such equation (8) as in the above is established, by
5 taking the above-described equation (7) into consideration, the
number of pixels detected by the valid video period detection
circuit 17 and the horizontal resolution have such relationship
therebetween as an equation (9) if the above equation (8) is
expressed by the inequality.

$$\text{Detected Number of Pixels} > \text{Horizontal Resolution}/2 \dots (9)$$

When the above equation (9) is satisfied, the comparator
8 outputs the control signal 12 to the multiplexer 2 so as to bring
the multiplexer 2 to select the signal from the one-clock delay
15 circuit 1. In response to the control signal 12, the multiplexer
2 switches its output signal. Once the signal from the one-clock
delay circuit was selected, the A/D converter 3 starts regarding
a signal whose phase is delayed by one clock as a reference,
retaining a state that the head data in the valid video signal
20 region is always outputted from the first phase data. Therefore,
once retaining the state that the head data is always outputted
from the first phase data, similar to the case in the first
embodiment, the present video signal processing circuit basically
has no need to operate thereafter.

25 Note herein that, even if the head data in the valid video



signal region is started to be outputted from the second phase data in operation, similarly to the case in the first embodiment, the present video signal processing device can retain the state that the head data in the valid video signal region is always
5 outputted from the first phase data.

In FIGS. 11, described next is a case where an arbitrary pixel is OFF. A state that the video signal 24 is always one pixel short on the display is observed only when the above equation (9) is satisfied. This is because, such pixel shortage is not
10 observed when the head or the last of the video data is in the black level, but the video data needs to be ON at both ends in order to satisfy the equation (9).

Thus, when an equation (10) is satisfied, the comparator 8 retains the output state from the multiplexer 2 for output to
15 the A/D converter without any change.

$$\text{Detected Number of Pixels} \leq \text{Horizontal Resolution}/2 \quad \dots$$

(10)

When the above-described equation (9) is satisfied, the comparator 8 outputs the control signal 12 so as to switch the
20 output from the multiplexer 2. With such operation of the comparator 8, the present video signal processing device can bring the display to display a video without pixel shortage.

As described in the foregoing, according to such structured present video signal processing device that the valid video period
25 detection circuit 17 where receiving detection pulses detected



by the leading edge detection circuit 40 and the falling edge
detection circuit 16 detects the number of pixels, and the
comparator 18 receives the detected number of pixels and a value
half of the horizontal resolution for comparison, a display can
5 assuredly display every video signal thereon.

In this embodiment, similarly to the case in the first
embodiment, the one-clock delay circuit 1 may be any type of
circuit as far as the reference signal 9 is delayed by the odd
number of clocks therein. Also, the A/D converter 3 may be the
10 one carrying out four-phase processing or six-phase processing,
which can easily operate in a similar manner.

(Fifth Embodiment)

FIG. 12 is a block diagram showing the structure of a video
signal processing device according to a fifth embodiment of the
15 present invention. In FIG. 12, the present video signal
processing device is almost identical in structure to the
above-described video signal processing device of the third
embodiment in FIG. 7. Note that, the present video signal
processing device is provided with a first leading edge detection
20 circuit 4, a first falling edge detection circuit 160, and a first
valid video period detection circuit 20 instead of the leading
edge detection circuit 40, the falling edge detection circuit 160,
and the valid video period detection circuit 17 in FIG. 7. And
therein, a second leading edge detection circuit 5, a second
25 falling edge detection circuit 21, and a second valid video period



detection circuit 22 are additionally provided. These are the differences from the above-described video signal processing device of the third embodiment. Thus, in the present video signal processing device, any constituent identical to that in the video
5 signal processing device of the third embodiment is under the same reference numeral, and is not described again. Herein, a comparator 23 is different from the comparator 15 in reference numeral since receiving a signal different from the one thereto.

Focusing on a signal applied to the leading edge detection
10 circuits, the falling edge detection circuits, and the valid video period detection circuits, the present video signal processing device may be a combination, in structure, of the video signal processing device of the above-described third embodiment in FIG. 7 and the video signal processing device of the above-described
15 fourth embodiment in FIG. 10. Details are described below.

As described in the foregoing, the video signal processing devices of the third and fourth embodiments have to detect the horizontal resolution in the image signal source. This horizontal resolution in the image signal source can be estimated
20 by detecting, generally, the frequencies of the horizontal synchronizing signal and the vertical synchronizing signal from the respective image signal sources. In the recent market, however, such estimation of the horizontal resolution in the frequencies of the horizontal synchronizing signal and the
25 vertical synchronizing signal may not be applicable to some image



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signal sources.

Therefore, in order to bring the display deal with such image signal sources, the device needs to be differently structured so as to recognize such image signal sources. Moreover, if such image signal sources vary in type, the device thus differently-structured becomes larger in size, enlarging the circuit in its entirety.

By taking these into consideration, the video signal processing device of this embodiment can easily clear the above-described problems with the structure as shown in FIG. 12. Next below, the operation of the present video signal processing device is described by referring to FIGS. 13.

FIGS. 13 are time charts showing the relationship among the detection signals generated in the valid video period detection circuits 17 and 22, the first phase data 10, and the second phase data 11. Specifically, FIG. 13(a) shows a case where the head data (data on the left end on the display) in the valid video signal region is included in the first phase of the A/D converter 3, while FIG. 13(b) shows a case where the head data is included in the second phase of the A/D converter 3.

In FIGS. 13, a to t denote data included in the video signal 24 provided to the A/D converter 3. For convenience, each of a to t is assumed to be ON.

First, as shown in FIG. 11(a), the head data (data on the left end on the display) a in the valid video signal region is



included in the first phase data 10. Thus, the data *b* which is the second from the head is included in the second phase data 11 at the same phase position as *a* in the first phase data. In this manner, the A/D converter 3 subjects 20 pieces of data from data
5 *a* to data *t* to the two-phase processing.

The leading edge and falling edge of the detection signal generated in the valid video period detection circuit 17 coincide with the leading edge of the first phase data 10 and the falling edge of the second phase data 11, respectively. This is the same
10 operation as the video signal processing device of the third embodiment, that is, the same as the above-described case shown in FIG. 9 (a). The leading edge and falling edge of the detection signal generated in the valid video period detection circuit 22 coincide with the leading edge of the second phase data 11 and
15 the falling edge of the first phase data 10, respectively. This is the same operation as the video signal processing device of the fourth embodiment, that is, the same as the above-described case shown in FIG. 11(a).

Therefore, as shown in FIG. 13(a), such relationship as an
20 equation (11) below is established between a pulse width PW1 of the detection signal generated in the valid video period detection circuit 17 and a pulse width PW2 of the detection signal generated in the valid video period detection circuit 22.

$$PW1 = PW2 \quad \dots (11)$$

25 When the above equation (11) is satisfied, the comparator

8 outputs the control signal 12 to the multiplexer 2 so as to bring
the multiplexer 2 to select the reference signal 9. In response
to the control signal 12, the multiplexer 2 selects the reference
signal 9 corresponding to the control signal for output to the
5 A/D converter 3. As such, once receiving the reference signal
9, the A/D converter 3 can retain a state that the head data in
the valid video signal region is always outputted from the first
phase data. Therefore, once retaining the state that the head
data is always outputted from the first phase data, the present
10 video signal processing circuit basically has no need to operate
thereafter.

Next, as shown in FIG. 13(b), the head data (data on the
left end of the display) *a* in the valid video signal region is
included in the second phase data 11. Thus, the data *b* second
15 from the head is included in the second phase data 11 at a position
having the one-clock-delayed phase relationship with the position
of *a* in the first phase data. As such, the A/D converter 3 subjects
20 pieces of data from data *a* to data *t* to the two-phase processing.

The leading edge and falling edge of the detection signal
20 generated in the valid video period detection circuit 17 coincide
with the leading edge of the first phase data 10 and the falling
edge of the second phase data 11, respectively. This is the same
operation as the video signal processing device of the third
embodiment, that is, the same as the above-described case shown
25 in FIG. 9 (b). The leading edge and falling edge of the detection



signal generated in the valid video period detection circuit 22 coincide with the leading edge of the second phase data 11 and the falling edge of the first phase data 10, respectively. This is the same operation as the video signal processing device of the fourth embodiment, that is, the same as the above-described case shown in FIG. 8(b).

Therefore, as shown in FIG. 13(a), such relationship as an equation (12) below is established between a pulse width PW1 of the detection signal generated in the valid video period detection circuit 17 and a pulse width PW2 of the detection signal generated in the valid video period detection circuit 22.

$$PW1 < PW2 \quad \dots (12)$$

When the above equation (12) is satisfied, the comparator 8 outputs the control signal 12 to the multiplexer 2 so as to let the multiplexer 2 select the signal from the one-clock delay circuit 1. In response to the control signal 12, the multiplexer 2 switches its output signal. To be specific, the multiplexer 2 selects the signal from the one-clock delay circuit 1 for output to the multiplexer 2. Once the signal from the one-clock delay circuit 1 was selected, the A/D converter 3 regards a signal whose phase is delayed by one clock as a reference, and thus, such state that the head data in the valid video signal region is always outputted from the first phase data can be retained. As such, similarly to the case in the first embodiment, the present video signal processing circuit has no need to operate once such state



that the head data is always outputted from the first phase data is retained.

Note herein that, even if the head data in the valid video signal region is started to be outputted from the second phase data in operation, similarly to the case in the first embodiment, the present video signal processing device can retain the state that the head data in the valid video signal region is always outputted from the first phase data.

Next, in FIG. 11(a), described is a case where only the video data a and t is OFF. In such case, the head data is not included in the first phase data 10, and the last data of the video data is not included in the second phase data 11. That is in the same state as in FIG. 11(b). With the above equation (12) established, the comparator 8 thus outputs the control signal 12 to the multiplexer 2 so as to bring the multiplexer 2 to select the signal from the one-clock delay circuit 1. In response to the control signal 12, the multiplexer 2 switches its output signal. To be specific, the multiplexer 2 selects the signal from the one-clock delay circuit 1 for output to the A/D converter 3. Once the signal from the one-clock delay circuit 1, the A/D converter 3 regards a signal whose phase is delayed by one clock as a reference, and thus, the state that the head data in the valid video signal region is always outputted from the first phase data.

At this time, the head data a in the video signal 24 is included in the second phase data 11. This may sound that the



status is not ideal. However, since the video data a and t is the black data, the data has pixel shortage from the beginning, and thus does not cause such problem as described in the foregoing if shown on the display as it is. In FIG. 11(b), when only the video data a and t is OFF, the similar description is applicable.

Further, in FIG. 11(a), it is described a case where any arbitrary pixel excepting for the video data a and t is OFF. In this case, when the video data b or s is the black data, PW1 becomes larger than PW2. Accordingly, when the following equation (13) is established, the comparator 8 retains the output state of the multiplexer 2, and outputs the same to the multiplexer 2 as it is.

$$PW1 \leq PW2 \quad \dots (13)$$

In FIG. 11(b), when any arbitrary pixel excepting for the video data a and t is OFF, the above equation (12) is applicable.

As is known from the above, when the above equation (13) is satisfied, the comparator 8 does not output the control signal 12 to the multiplexer 12 so that the state for the output signal in the multiplexer 2 is retained. When the above equation (12) is satisfied, the comparator 8 outputs the control signal 12 to the multiplexer 2 so as to bring the multiplexer 2 to switch its output signal. By such operation, the present video signal processing device can always let the display display the video without pixel shortage.

Herein, in this embodiment, similarly to the case in the



first embodiment, the one-clock delay circuit 1 may be any type of circuit as far as the reference signal 9 is delayed by the odd number of clocks therein. Still further, the A/D converter 3 may be the one carrying out four-phase processing or six-phase
5 processing, resulting in the similar operation.

As is known from the above, according to the structure of the video signal processing device of this embodiment, the display can assuredly display every video signal thereon without detecting the horizontal resolution in the image signal source.

10 (Sixth Embodiment)

FIG. 14 is a block diagram showing the structure of a video signal processing device according to a sixth embodiment of the present invention. In FIG. 14, the present video signal processing device is almost identical in structure to the
15 above-described video signal processing device of the first embodiment in FIG. 1. The present video signal processing device is not provided with the multiplexer 2 and the one-clock delay circuit 1, but is newly provided with multiplexers 26 and 27, and a one-clock delay circuit 25. Further, signal input/output is
20 different therein. These are the differences from the above-described video signal processing device of the first embodiment. Thus, in the present video signal processing device, any constituent identical to that in the video signal processing device of the first embodiment is under the same reference numeral,
25 and is not described again.

On comparison between the video signal processing device of the above-described first or fifth embodiment, the present video signal processing device is characterized in the position of the one-clock delay circuit 25. Next below, the reason for such characteristic is described.

In the video signal processing device of the first or the fifth embodiment, the phase of the pulse outputted from the multiplexer 2 is changed in response to the video signal 24 so that the display can assuredly display every video signal thereon. Herein, the one-clock delay circuit 1 provided in those video signal processing devices delays a signal from an image signal source only by one pixel. Accordingly, when dealing with an image signal source whose resolution is in super high level, the one-clock delay circuit 1 needs to be structured by very high speed elements. If this is the case, problematically, the cost thereof is increased, and the consumption electricity is also increased.

Therefore, the present video signal processing device is so structured as shown in FIG. 14 to easily clear the above problems. In detail, in FIG. 14, the one-clock delay circuit 25 receives the second phase data 11, and then delays the data by one clock through the two-phase processing (that is, originally two clocks from the image signal source). Accordingly, the one-clock delay circuit 25 can deal with the image signal source having the super high resolution without being structured by the super fast elements.

Next, in the present video signal processing device, the multiplexer 26 receives the first phase data 10, and a signal outputted from the one-clock delay circuit 25 where receiving the second phase data 11, that is, the one-clock delayed second phase data 11. The multiplexer 27 receives the first phase data 10 and the second phase data 11. When the present video signal processing device is activated, the multiplexer 26 selects the first phase data 10 for output, while the multiplexer 26 selects the second phase data 11 for output. Thereafter, in response to the control signal 12 outputted from the comparator 8, the multiplexer 26 switches itself to select the one-clock-delayed second phase data 11 for output, while the multiplexer 26 switches itself to select the first phase data 10 for output.

On comparison between the video signal processing device of the first embodiment, the operation of such structured video signal processing device of this embodiment is described by referring to FIGS. 15.

FIGS. 15 are schematic diagrams showing the relationship among the first phase data 10, the second phase data 11, an output signal 28 from the multiplexer 26, and an output signal 29 from the multiplexer 27. In FIGS. 15, a to t denote data included in the video signal 24 going to the A/D converter 3. Specifically, FIG. 15(a) shows a case where the head data (data displayed on the left end on the display) in the valid video signal region is included in the first phase data 10 from the A/D converter 3, while



FIG. 15(b) shows a case where the head data is included in the second phase data 11 from the A/D converter 11.

First, in such case as shown in FIG. 15(a), the comparator 8 operates in a similar manner to the video signal processing device of the first embodiment. That is, as described in the foregoing, when the above equation (1) is satisfied, the comparator 8 does not output the control signal 12 to the multiplexers. Accordingly, as described in the foregoing, the multiplexers 26 and 27 select, without going through its switching operation, the first phase data 10 and the second phase data 11 outputted from the A/D converter 3, respectively, for output. In this manner, the present video signal processing device can retain the state that the head data in the valid video signal region is always outputted from the first phase data. Therefore, once retaining the state that the head data is always outputted from the first phase data, the present video signal processing circuit basically has no need to operate thereafter.

Next, similarly in such case as shown in FIG. 15(b), the comparator 8 operates in the same manner as the video signal processing device of the first embodiment. To be specific, as described in the foregoing, when the above equation (2) is satisfied, the comparator 8 outputs the control signal 12 to the multiplexers. Accordingly, in response to the control signal 12, the multiplexers 25 and 26 going through the above-described switching operation. In detail, the multiplexer 26 switches



itself to select the one-clock delayed second phase data 11 for output, while the multiplexer 26 switches itself to select the first phase data 10 for output. In such manner, the present video signal processing device can retain the state that the head data
5 in the valid video signal region is always outputted from the first phase data. Therefore, once retaining the state that the head data is always outputted from the first phase data, the present video signal processing circuit basically has no need to operate thereafter.

10 Note herein that, even if the head data in the valid video signal region is started to be outputted from the second phase data in operation, the present video signal processing device can retain the state that the head data in the valid video signal region is always outputted from the first phase data.

15 As is known from the above, the video signal processing device of this embodiment can deal with an image signal source having higher resolution, and can assuredly let the display display every video signal thereon.

Note herein that, the video signal processing device of this
20 embodiment can be provided with first and second falling edge detection circuits instead of the first and second leading edge detection circuits 4 and 5. With such structure, the first and second back porch detection circuits 6 and 7 operate to detect a period including the back porch period and the valid video signal
25 period. Thus, with such structure, the video signal processing



device of this embodiment can also operate in a similar manner.

Further, for the sake of clarity, the video signal processing device of this embodiment is a modification in structure of the video signal processing device of the first embodiment. Here, the video signal processing device of this
5 embodiment can be a modification of the video signal processing device of the above-described second or the fifth embodiment. In detail, the control signal 12 controlling the multiplexer 2 provided in the video signal processing device of the above-
10 described second or the fifth embodiment can be used as a control signal controlling the multiplexers 26 and 27 provided in the present video signal processing device. With such structure, the video signal processing device of this embodiment can be easily realized by modifying the video signal processing device of the
15 second or the fifth embodiment.

Further, in this embodiment, the one-clock delay circuit 1 may be any type of circuit as far as the reference signal 9 is delayed by the odd number of clocks therein. Still further, the A/D converter 3 may be the one carrying out four-phase processing
20 or six-phase processing, resulting in a similar operation.

(Seventh Embodiment)

FIG. 16 is a block diagram showing the structure of a video signal processing device according to a seventh embodiment of the present invention. In FIG. 16, the present video signal
25 processing device is almost identical in structure to the

above-described video signal processing device of the first embodiment in FIG. 1. The present video signal processing device is newly provided with first and second minimum value retention circuits 30 and 31, and this is the difference from the
5 above-described video signal processing device of the first embodiment. Thus, in the present video signal processing device, any constituent identical to that in the video signal processing device of the first embodiment is under the same reference numeral, and is not described again. Next below, it is described the reason
10 why the first and second minimum value retention circuits 30 and 31 are newly provided.

The video signal processing device of the first embodiment is so structured that the back porch periods each outputted from the first and second back porch detection circuits 6 and 7 go to
15 the comparator 8, and accordingly let the display display every video signal thereon. With such structure, no problem occurs if any arbitrary line in the video signal 24 can be extracted for operation such as a still image. However, if the video signal 24 is a moving image, the back porch period does not stay the same.
20 Thus, the phase of the line on the image is frequently shifted. In this respect, the video signal processing device does not operate in a normal manner.

Thus, the video signal processing device of this embodiment can clear easily the above-described problem by using, as shown
25 in FIG. 16, the first minimum value retention circuit 30 for

receiving the back porch period detected by the first back porch
detection circuit 6, and detecting the minimum value thereof, and
the second minimum value retention circuit 31 for receiving the
back porch period detected by the second back porch detection
5 circuit 7, and detecting the minimum value thereof. Next below,
the operation of the present video signal processing device is
described by referring to FIG. 16.

In FIG. 16, the first and second minimum value retention
circuits 30 and 31 are circuits for detecting, respectively, the
10 minimum value of the back porch periods successively outputted
from the corresponding back porch detection circuits 5 and 7. The
first and second minimum value retention circuits 30 and 31
typically store the minimum value, compare the received back porch
period with the minimum value in storage, and operate to update
15 the minimum value.

Thanks to the first and second minimum value retention
circuits 30 and 31, the present video signal processing device
can fixedly recognize the back porch period of the video signal
24 by utilizing the minimum value thereof. In such manner, the
20 present video signal processing device can operate in a stable
manner for detection in the moving images. Further, with the
first and second minimum value retention circuits 30 and 31,
detection of the back porch period can be carried out real time.
Thus, the present video signal processing device can let the
25 display display every pixel of the video signal 24 thereon

regardless of the types of the video signal 24 provided from the image signal source.

As described in the foregoing, the video signal processing device of this embodiment can deal with the case, with ease, that
5 a video signal from the image signal source is a moving image, and can assuredly let the display display every video signal thereon.

For the sake of clarity, the video signal processing device of this embodiment is provided with the first and second minimum
10 value retention circuits 30 and 31 in addition to the video signal processing device of the first embodiment. Here, the video signal processing device of this embodiment may be provided with first and second maximum value retention circuits instead of the first and second minimum value retention circuits 30 and 31, and the
15 first and second falling edge detection circuits instead of the first and second leading edge detection circuits 4 and 5. In such structure, the first and second back porch detection circuits 6 and 7 operate to detect a period including both the back porch period and the valid video signal period. Thus, even with such
20 alternative structure, the video signal processing device of this embodiment can operate in a similar manner.

In this embodiment, similarly to the cases in the above-described embodiments, the one-clock delay circuit 25 may be any type of circuit as far as the reference signal 9 is delayed
25 by the odd number of clocks therein. Also, the A/D converter 3

may be the one carrying out four-phase processing or six-phase processing, resulting in the same operation.

INDUSTRIAL APPLICABILITY

5 With the present invention, a display on which pixels are fixed in number for display can display every video signal from an image signal source connected to a video signal processing device by detecting a back porch period or a valid video signal period in data varied in phase outputted from an A/D converter,
10 and even if the image signal source is higher in resolution, the display can assuredly display every video signal by switching output data varied in phase from the A/D converter.

CLAIMS



1. A video signal processing device for displaying, on a display, every pixel in a video signal inputted from an image signal source, the device comprising:

a clock delay circuit for receiving a reference signal, and
5 delays the reference signal by the odd number of clocks for output;

a multiplexer for selecting either said reference signal or an output signal from said clock delay circuit for output;

an A/D converter for converting said video signal into a digital signal for two-phase output as first phase data and
10 second phase data with reference to an output signal from said multiplexer;

a first leading edge detection circuit for detecting a leading edge of a valid video signal region in said first phase data, and outputs a detection signal corresponding thereto;

15 a second leading edge detection circuit for detecting a leading edge of a valid video signal region in said second phase data, and outputs a detection signal corresponding thereto;

a first back porch detection circuit for detecting a first back porch period starting from the output signal from said
20 multiplexer to the detection signal outputted from said first leading edge detection circuit;

a second back porch detection circuit for detecting a second back porch period starting from the output signal from said



25 multiplexer to the detection signal outputted from said second
leading edge detection circuit; and

a comparator for comparing said first back porch period and
said second back porch period, and when said first back porch
period is longer than said second back porch period, determining
that head data in the valid video signal region in said video signal
30 is not included in said first phase data, and outputting a signal
for controlling said multiplexer to switch an output signal
therefrom.

2. The video signal processing device according to claim 1,
wherein said first back porch detection circuit detects said first
back porch period by using the number of clocks in said video signal,
and

5 said second back porch detection circuit detects said
second back porch period by using the number of clocks in said
video signal.

3. The video signal processing device according to claim 1,
further comprising a first minimum value retention circuit for
inputting, into the comparator, a minimum value of said first back
porch periods outputted from said first back porch detection
5 circuit as another first back porch period, and

a second minimum value retention circuit for inputting,
into the comparator, a minimum value of said second back porch



period outputted from said second back porch detection circuit as another second back porch period.

4. A video signal processing device for displaying, on a display, every pixel in a video signal inputted from an image signal source, the device comprising:

a clock delay circuit for receiving a reference signal, and
5 delays the reference signal by the odd number of clocks for output;

a multiplexer for selecting either said reference signal or an output signal from said clock delay circuit for output;

an A/D converter for converting said video signal into a digital signal for two-phase output as first phase data and second
10 phase data with reference to an output signal from said multiplexer;

a leading edge detection circuit for detecting, in a predetermined manner, a leading edge of a valid video signal region in either predetermined said first phase data or said
15 second phase data, and outputs a detection signal corresponding thereto;

a back porch detection circuit for detecting a back porch period starting from the output signal from said multiplexer to the detection signal outputted from said leading edge detection
20 circuit;

a storage part for receiving said back porch period, and storing and outputting in a manner each corresponding to said



reference signal selected and outputted by said multiplexer and the output signal from said clock delay circuit; and

25 a comparator for outputting a control signal for controlling said multiplexer to switch a signal selected and outputted therefrom so that said storage part outputs a back porch period each corresponding to the signal selected and outputted from said multiplexer, comparing the corresponding back porch
30 periods outputted from said storage part with each other, and when the back porch period corresponding to said reference signal is equal to or shorter than the back porch period corresponding to the output signal from said clock delay circuit, determining that head data in the valid video signal region in said video signal
35 is included in said first phase data, and outputting said control signal again.

5. The video signal processing device according to claim 4, wherein said back porch detection circuit detects said back porch period by using the number of clocks in said video signal.

6. A video signal processing device for displaying, on a display, every pixel in a video signal inputted from an image signal source, the device comprising:

 a clock delay circuit for receiving a reference signal, and
5 delays the reference signal by the odd number of clocks for output;
 a multiplexer for selecting either said reference signal



or an output signal from said clock delay circuit for output;
an A/D converter for converting said video signal into a digital signal for two-phase output as first phase data and second
10 phase data with reference to an output signal from said multiplexer;

a leading edge detection circuit for detecting a leading edge of a valid video signal region in said first phase data, and outputs a detection signal corresponding thereto;

15 a falling edge detection circuit for detecting a falling edge of a valid video signal region in said second phase data, and outputting a detection signal corresponding thereto;

a valid video period detection circuit for detecting a valid video period starting from the detection signal outputted from
20 said leading edge detection circuit to the detection signal outputted from said falling edge detection circuit; and

a comparator for comparing a value half of an inputted horizontal resolution with said valid video period, and when the value half of said horizontal resolution is larger than said valid
25 video period in value, determining that head data in the valid video signal region in said video signal is not included in said first phase data, and outputting a signal for controlling said multiplexer to switch an output signal therefrom.

7. The video signal processing device according to claim 6, wherein said valid video period detection circuit detects said



valid video period by using the number of clocks in said video signal.

8. A video signal processing device for displaying, on a display, every pixel in a video signal inputted from an image signal source, the device comprising:

a clock delay circuit for receiving a reference signal, and
5 delays the reference signal by the odd number of clocks for output;

a multiplexer for selecting either said reference signal or an output signal from said clock delay circuit for output;

an A/D converter for converting said video signal into a digital signal for two-phase output as first phase data and second
10 phase data with reference to an output signal from said multiplexer;

a leading edge detection circuit for detecting a leading edge of a valid video signal region in said second phase data, and outputs a detection signal corresponding thereto;

15 a falling edge detection circuit for detecting a falling edge of the valid video signal region in said first phase data, and outputs a detection signal corresponding thereto;

a valid video period detection circuit for detecting a valid video period starting from the detection signal outputted from
20 said leading edge detection circuit to the detection signal outputted from said falling edge detection circuit; and

a comparator for comparing a value half of an inputted



horizontal resolution with said valid video period, and when the value half of said horizontal resolution is smaller than said
25 valid video period in value, determining that head data in the valid video signal region in said video signal is not included in said first phase data, and outputting a signal for controlling said multiplexer to switch an output signal therefrom.

9. The video signal processing device according to claim 8, wherein said valid video period detection circuit detects said valid video period by using the number of clocks in said video signal.

10. A video signal processing device for displaying, on a display, every pixel in a video signal inputted from an image signal source, the device comprising:

a clock delay circuit for receiving a reference signal, and
5 delays the reference signal by the odd number of clocks for output;

a multiplexer for selecting either said reference signal or an output signal from said clock delay circuit for output;

an A/D converter for converting said video signal into a digital signal for two-phase output as first phase data and second
10 phase data with reference to an output signal from said multiplexer;

a first leading edge detection circuit for detecting a leading edge of a valid video signal region in said first phase



data, and outputs a detection signal corresponding thereto;

15 a second leading edge detection circuit for detecting a
leading edge of a valid video signal region in said second phase
data, and outputs a detection signal corresponding thereto;

 a first falling edge detection circuit for detecting a
falling edge of the valid video signal region in said second phase

20 data, and outputs a detection signal corresponding thereto;

 a second falling edge detection signal for detecting a
falling edge of the valid video signal region in said first phase
data, and outputs a detection signal corresponding thereto;

 a first valid video period detection circuit for detecting

25 a first valid video period starting from the detection signal
outputted from said first leading edge detection circuit to the
detection signal outputted from said first falling edge detection
circuit;

 a second valid video period detection circuit for detecting

30 a second valid video period starting from the detection signal
outputted from said second leading edge detection circuit to the
detection signal outputted from said second falling edge
detection circuit; and

 a comparator for comparing said first valid vide period and

35 said second valid video period, and when said second valid video
period is longer than said first valid video period, determining
that head data in the valid video signal region in said video signal
is not included in said first phase data, and outputting a signal



for controlling said multiplexer to switch an output signal
40 therefrom.

11. The video signal processing device according to claim 10,
wherein said first valid video period detection circuit detects
said first valid video period by using the number of clocks in
said video signal, and

5 said second valid video period detection circuit detects
said second valid video period by using the number of clocks in
said video signal

12. A video signal processing device for displaying, on a display,
every pixel in a video signal inputted from an image signal source,
the device comprising:

an A/D converter for converting said video signal into a
5 digital signal for two-phase output as first phase data and second
phase data with reference to an incoming reference signal;

a clock delay circuit for receiving said second phase data,
and delays the second phase data by the odd number of clocks for
output;

10 a first multiplexer for selecting either said first phase
data or an output signal from said clock delay circuit for output;

a second multiplexer for selecting either said second phase
data or said first phase data for output

a first leading edge detection circuit for detecting a



- 15 leading edge of a valid video signal region in said first phase data, and outputs a detection signal corresponding thereto;
- a second leading edge detection circuit for detecting a leading edge of a valid video signal region in said second phase data, and outputs a detection signal corresponding thereto;
- 20 a first back porch detection circuit for detecting a first back porch period starting from said reference signal to the detection signal outputted from said first leading edge detection circuit;
- a second back porch detection circuit for detecting a second
- 25 back porch period starting from said reference signal to the detection signal outputted from said second leading edge detection circuit; and
- a comparator for comparing said first back porch period and said second back porch period, and when said first back porch
- 30 period is longer than said second back porch period, determining that head data in the valid video signal region in said video signal is not included in said first phase data, and outputting a signal for controlling said first and second multiplexers to switch an output signal each therefrom simultaneously, wherein
- 35 right after activation, the first multiplexer selects the first phase data for output, and the second multiplexer selects the second phase data for output.

13. The video signal processing device according to claim 12,



wherein said first back porch detection circuit detects said first back porch period by using the number of clocks in said video signal, and

5 said second back porch detection circuit detects said second back porch period by using the number of clocks in said video signal.

ABSTRACT

It is possible to let a display, on which pixels are fixed
in number for display, display every video signal with a simple
5 circuit structure.

A one-clock delay circuit (1) delays a reference signal (9)
by one clock for output, a multiplexer (2) switches between the
one-clock-delayed signal and the reference signal (9) for output,
an A/D converter (3) subjects a video signal (24) to two-phase
10 processing with reference to an output signal from the multiplexer
(2), and a comparator (8) outputs a control signal (12) to the
multiplexer (2) to let the multiplexer (2) to select the one-
clock delayed signal when determining, based on a result obtained
by detection in the first and second back porch detection circuits
15 (6) and (7), that a head of video data is not included in first
phase output data.

FIG. 1

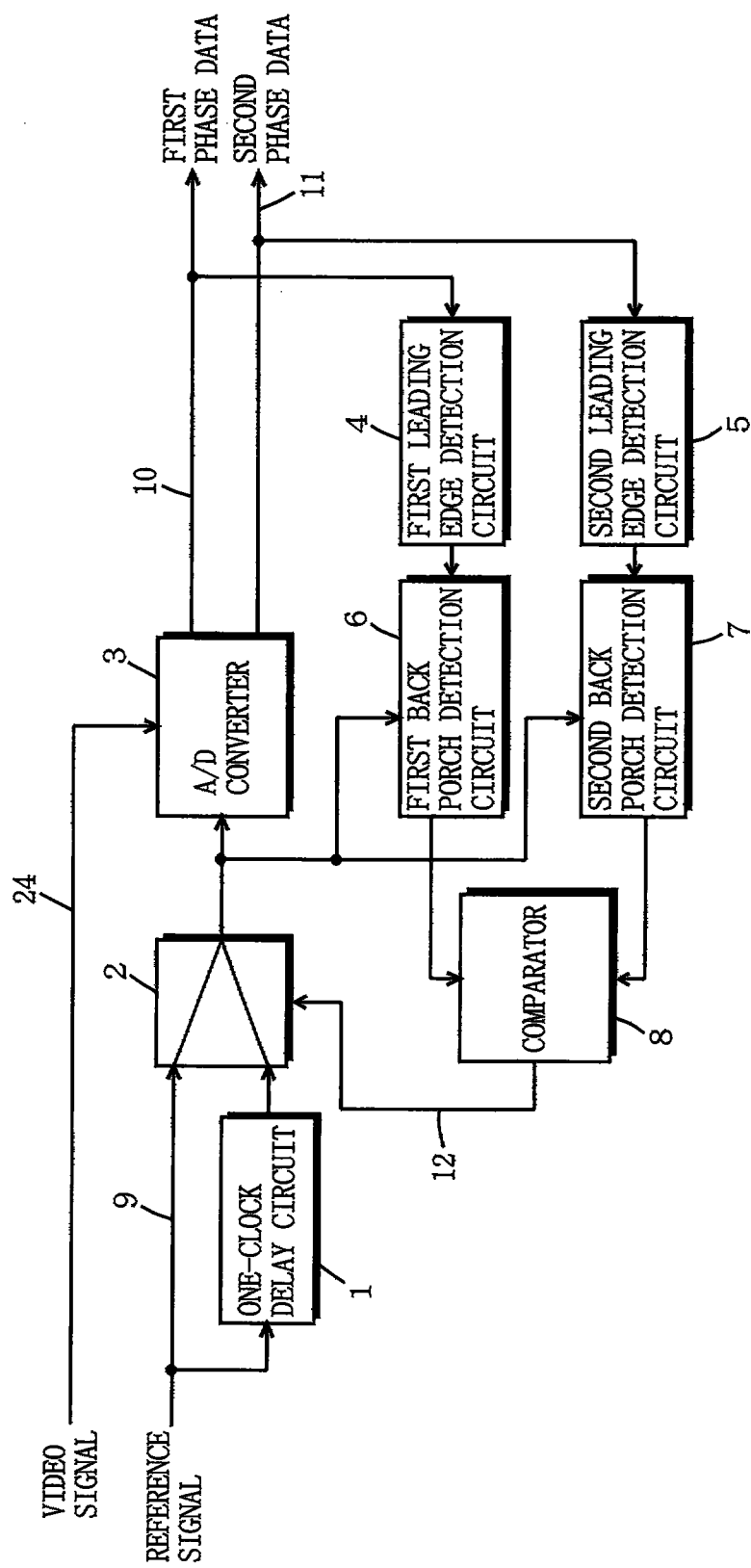


FIG. 2A

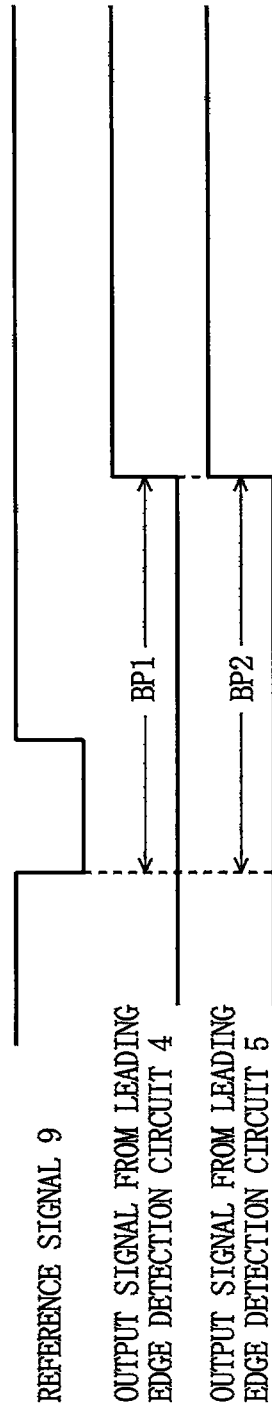


FIG. 2B

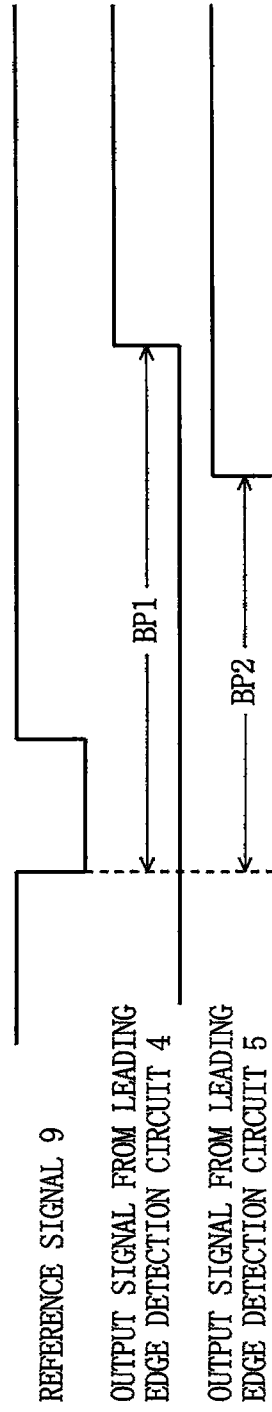


FIG. 3

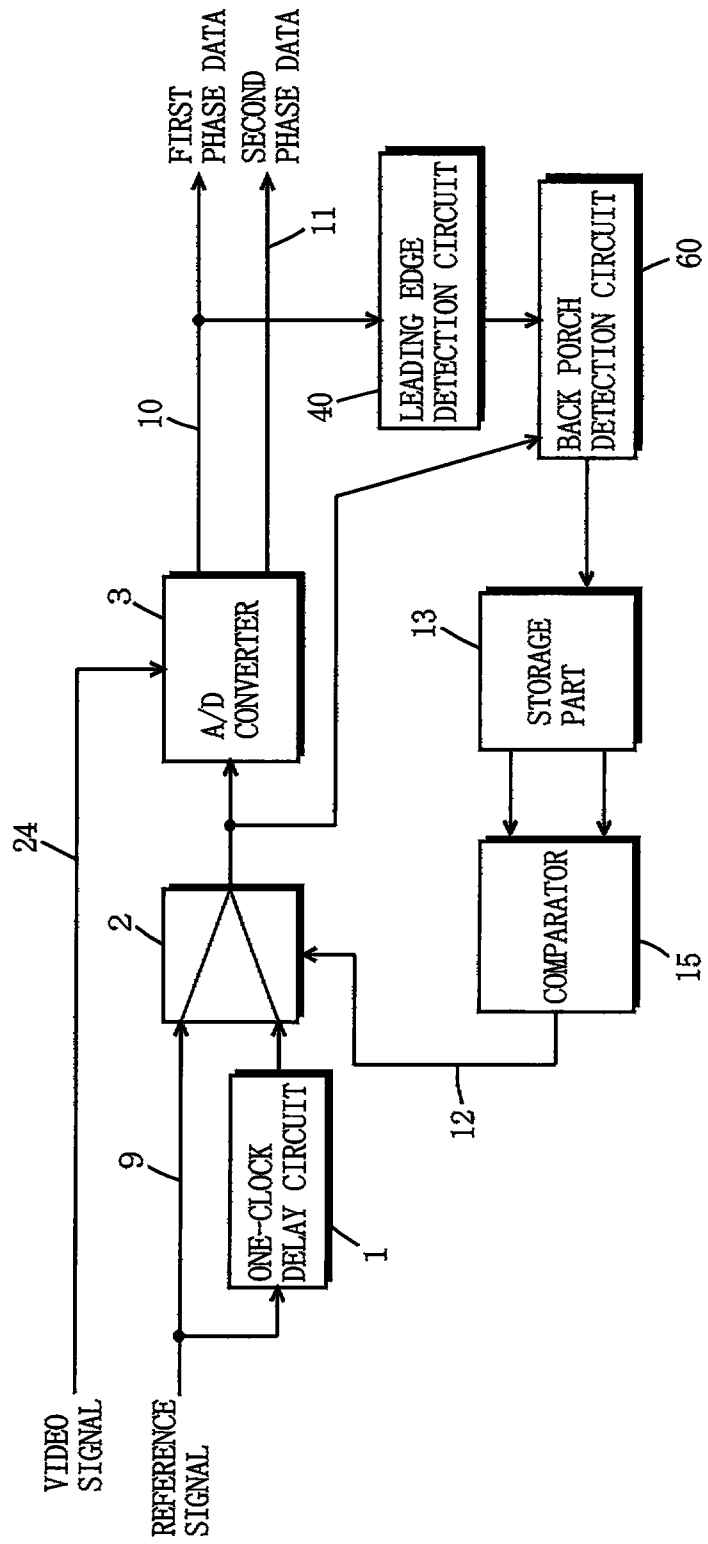


FIG. 4 A

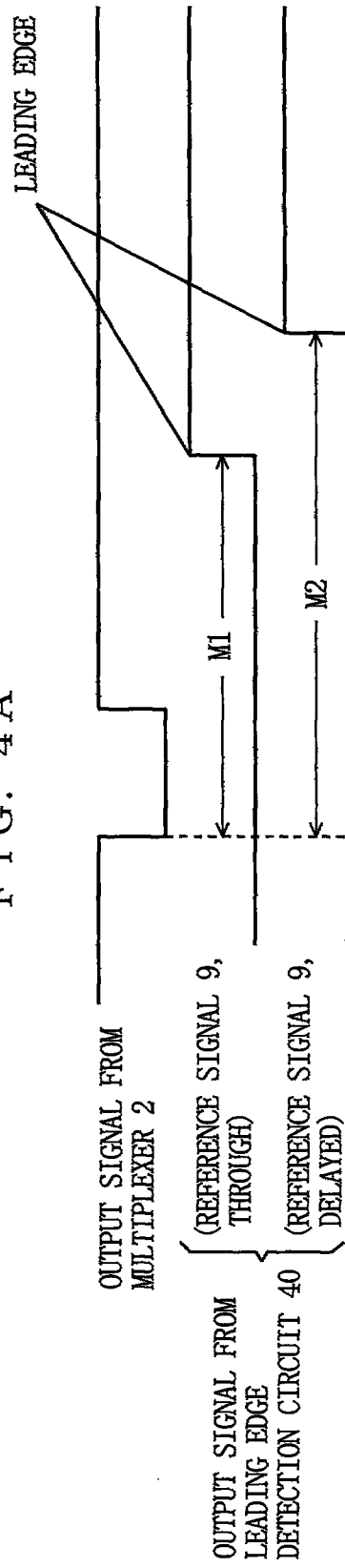


FIG. 4 B

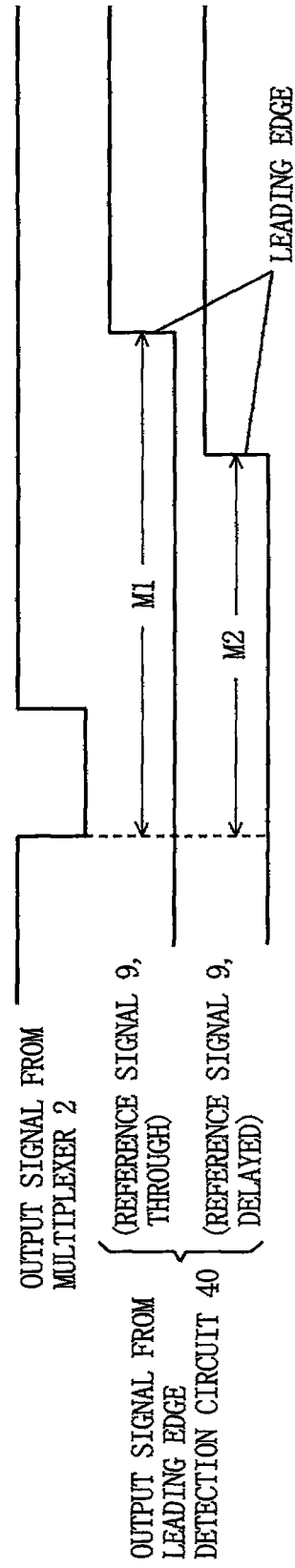


FIG. 5A

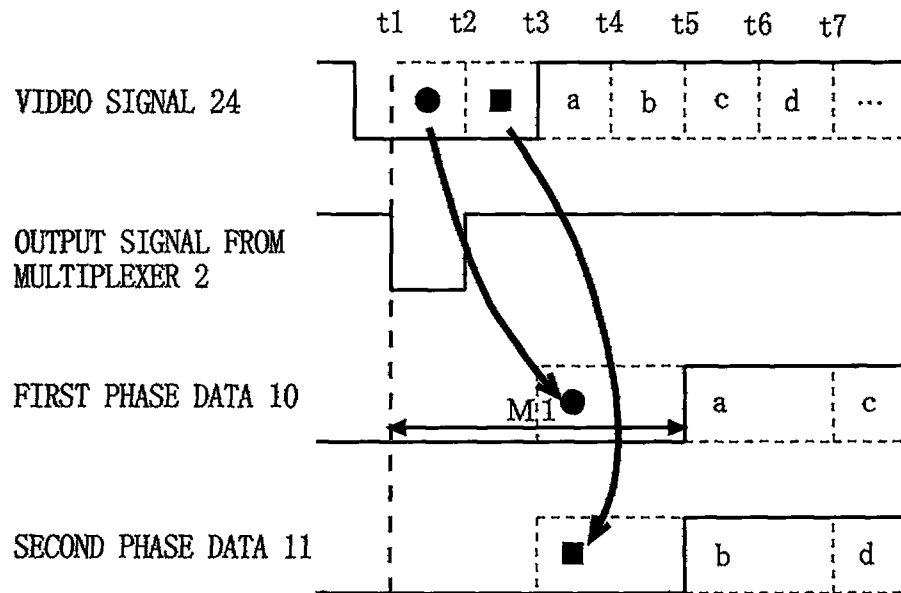


FIG. 5B

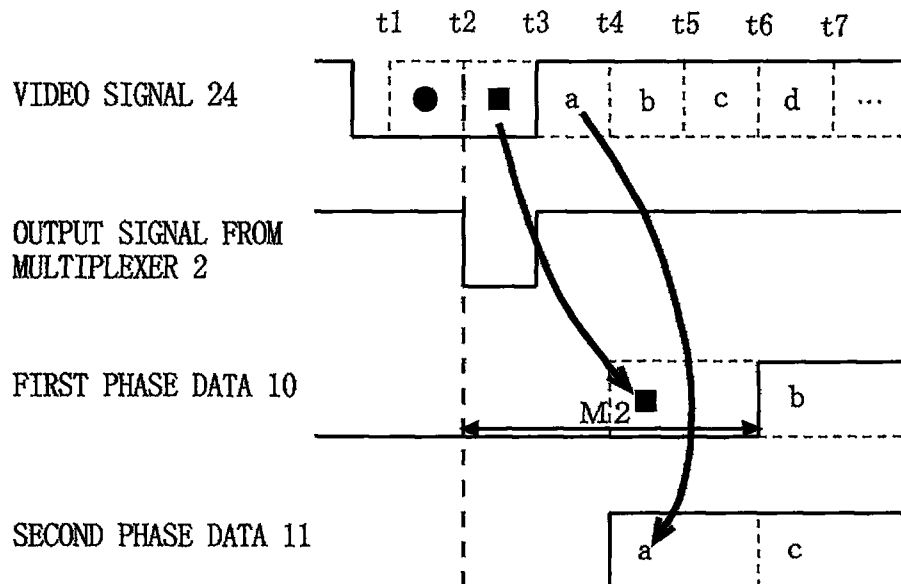


FIG. 6A

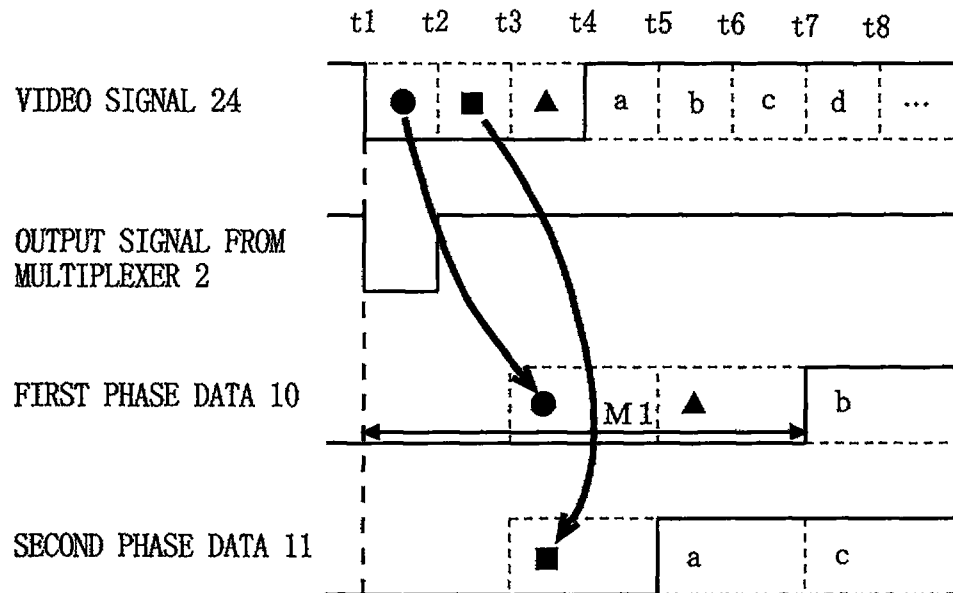


FIG. 6B

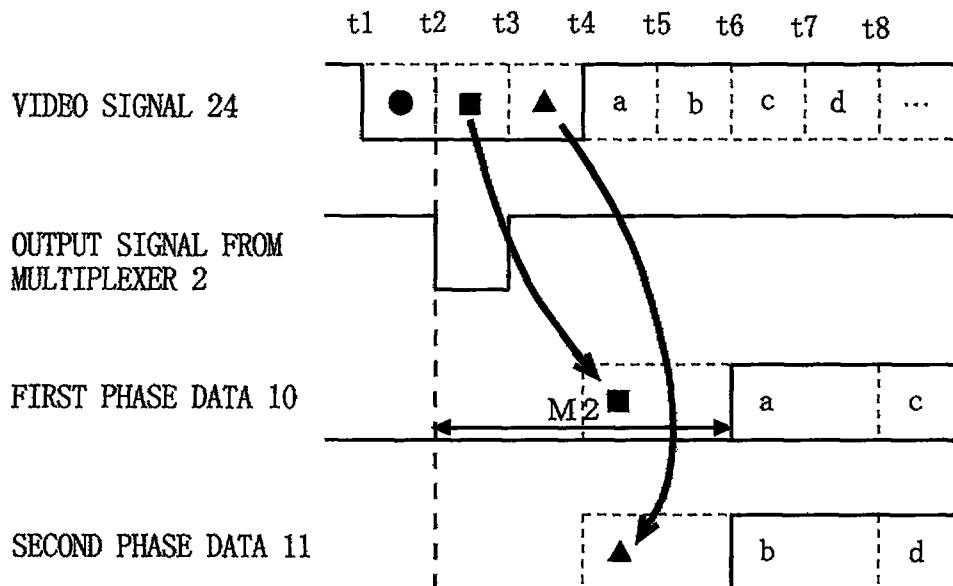


FIG. 7

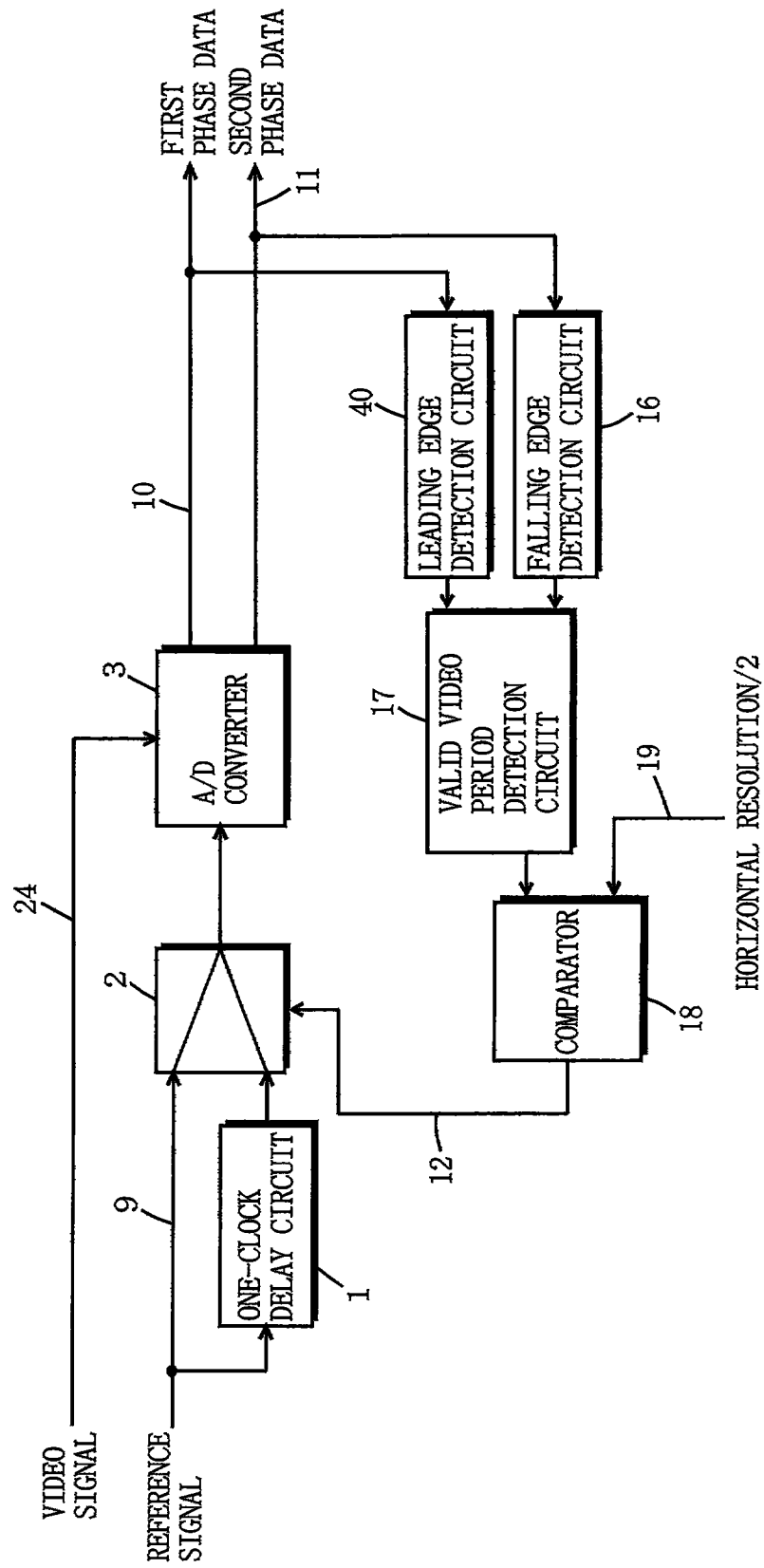


FIG. 8

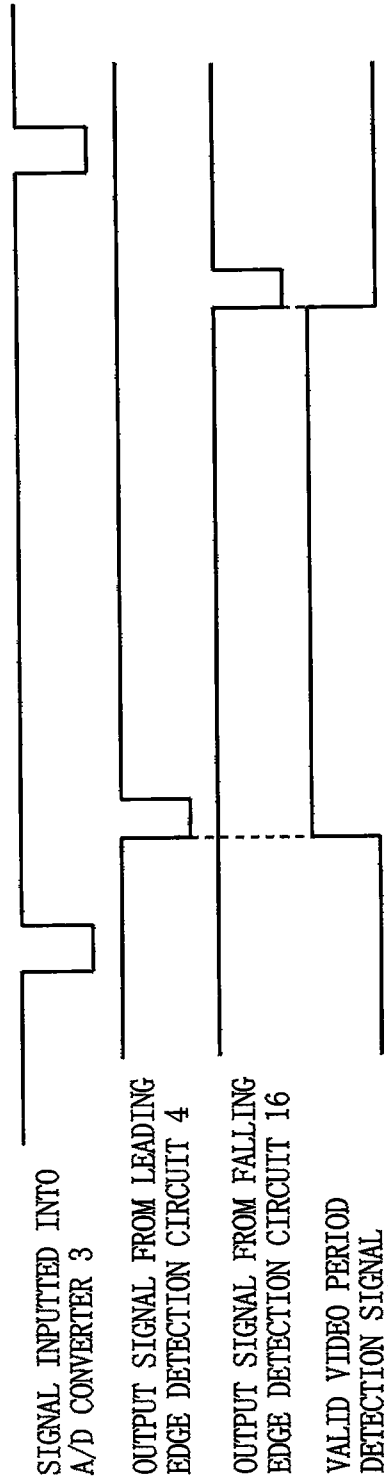


FIG. 9 A

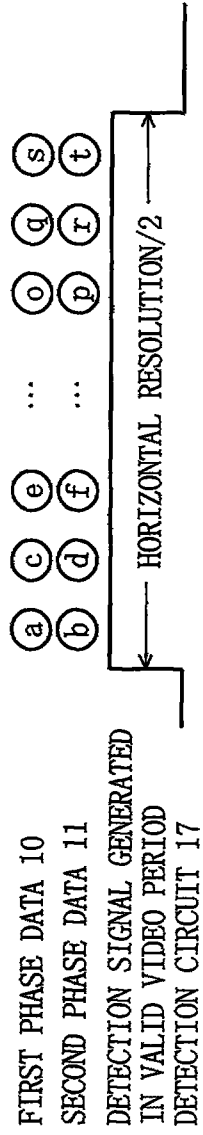


FIG. 9 B

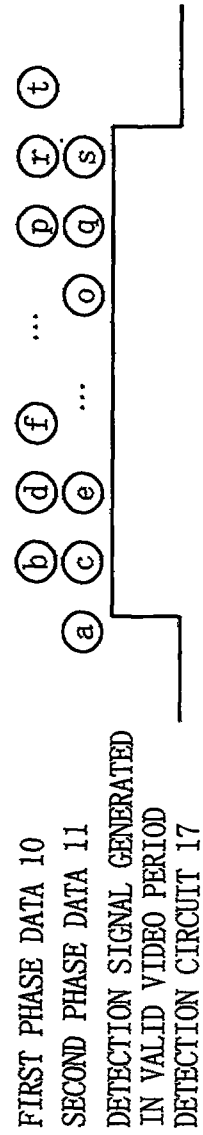


FIG. 10

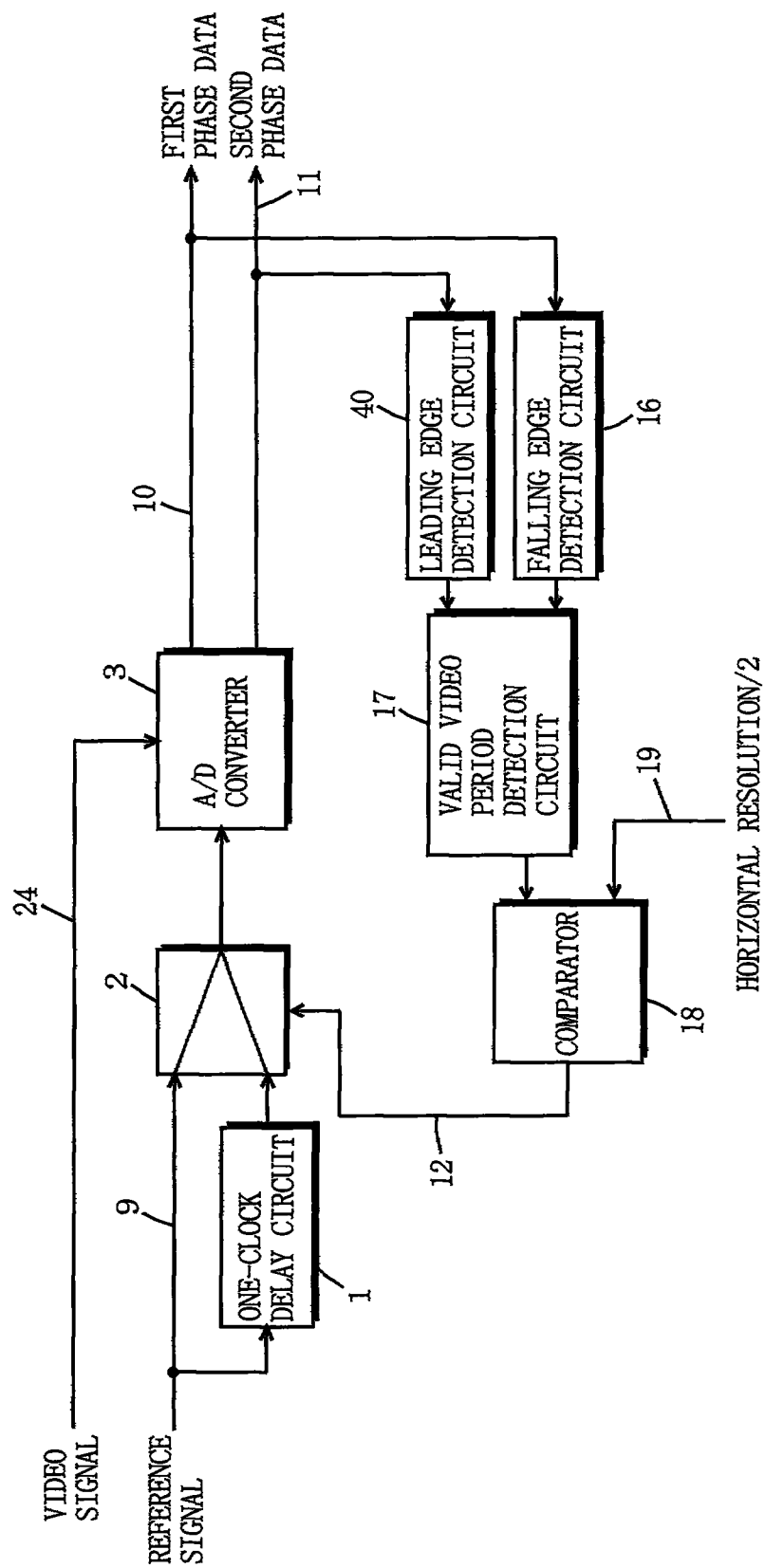


FIG. 11A

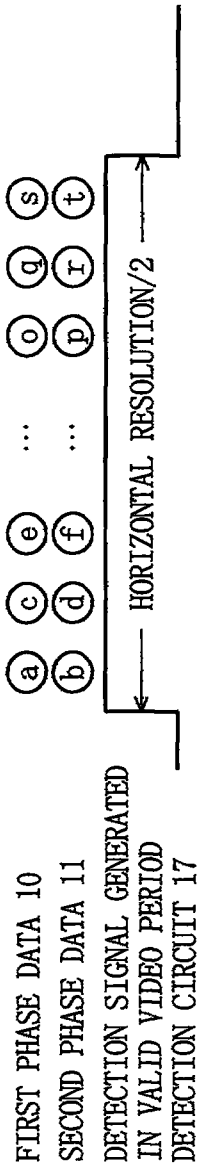


FIG. 11B

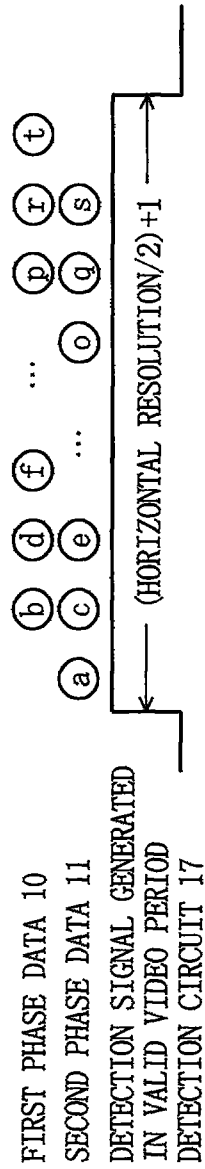


FIG. 12

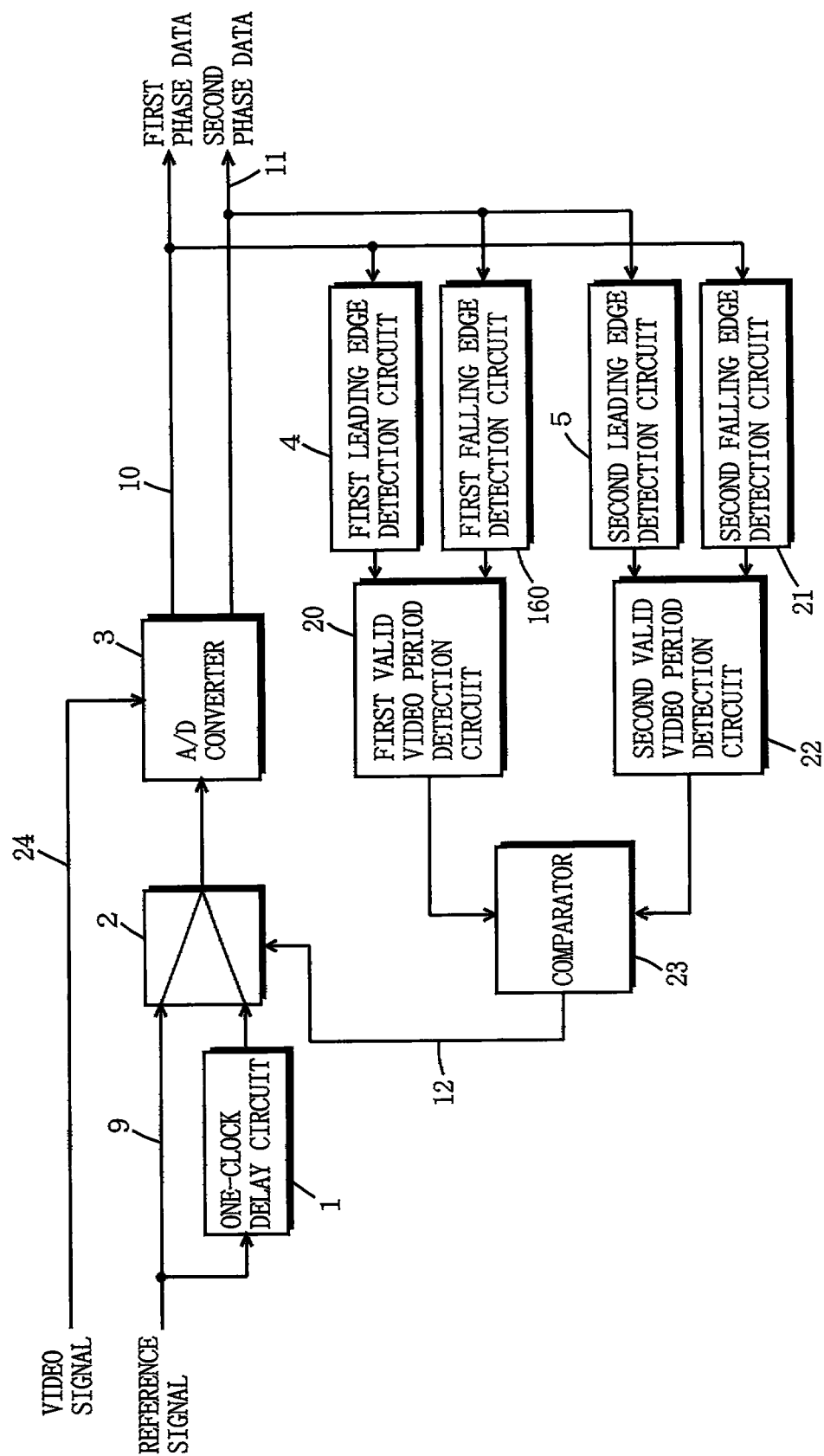


FIG. 13A

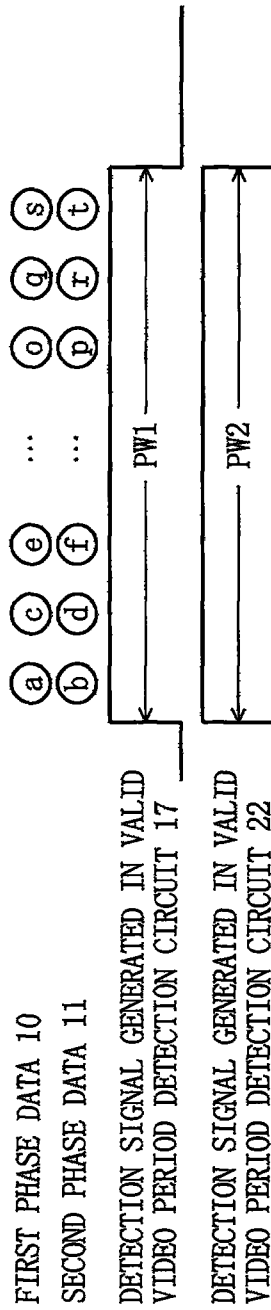
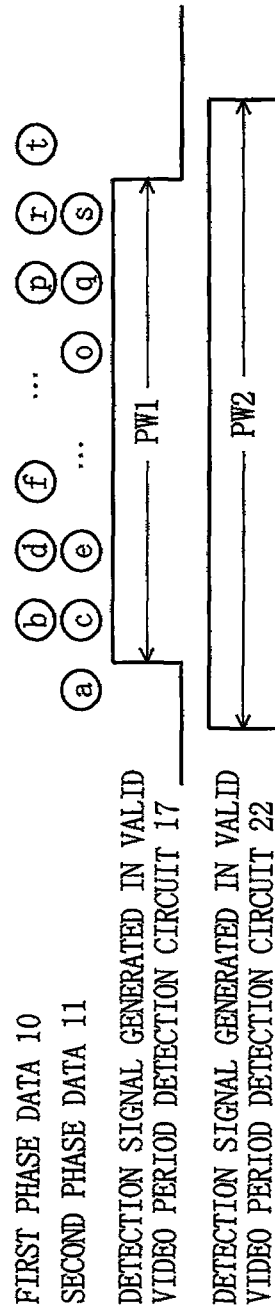


FIG. 13B



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FIG. 14

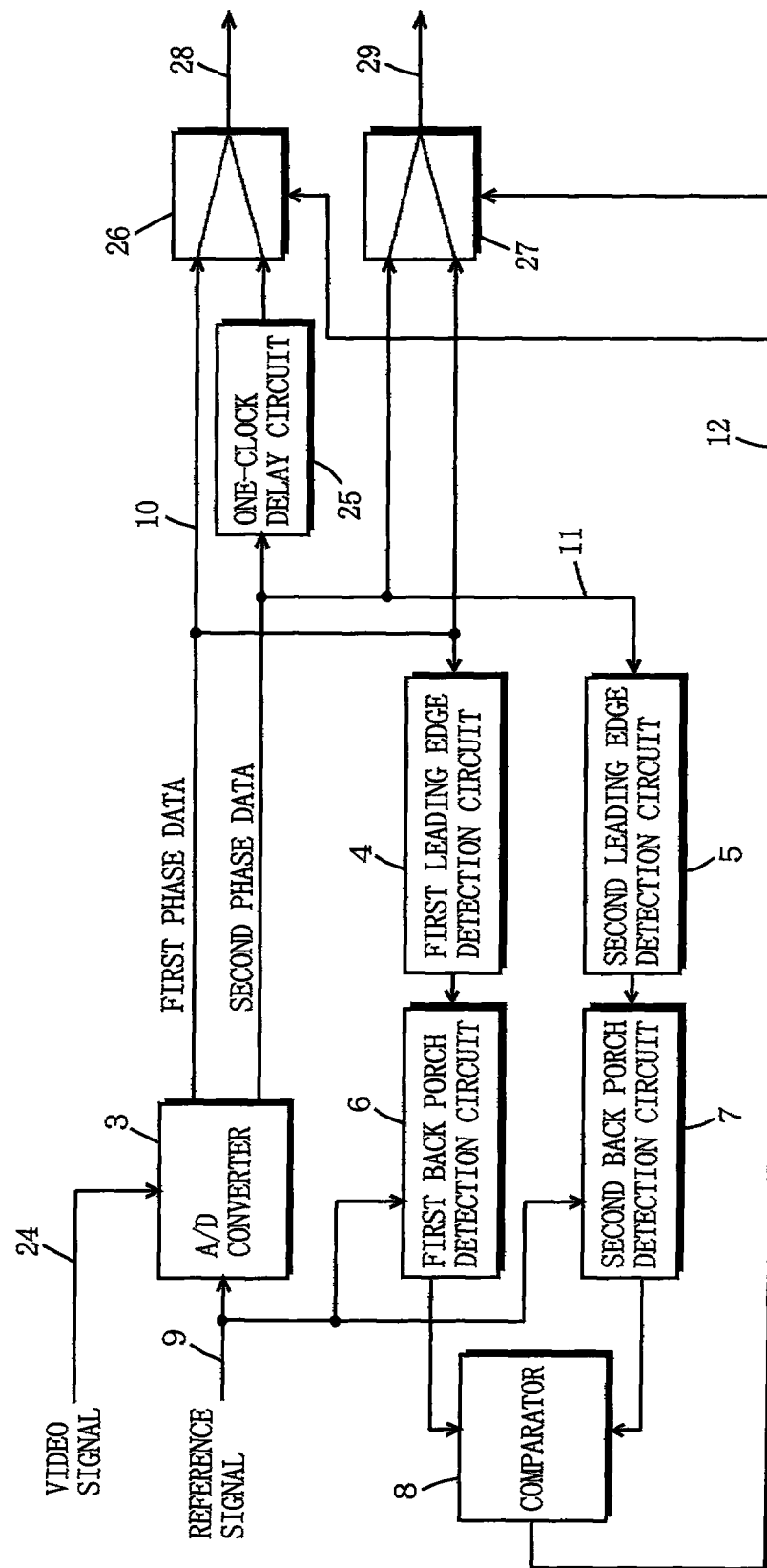


FIG. 15A

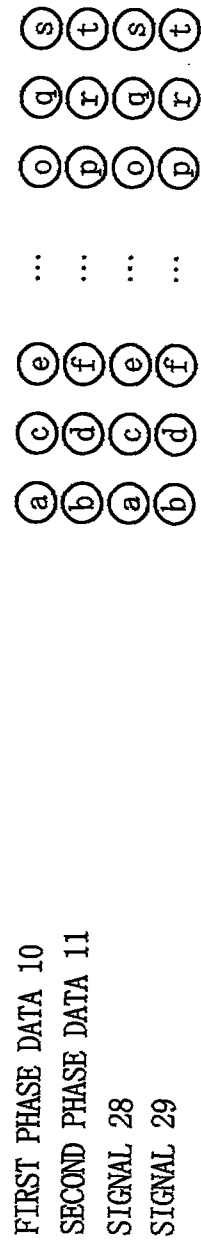


FIG. 15B

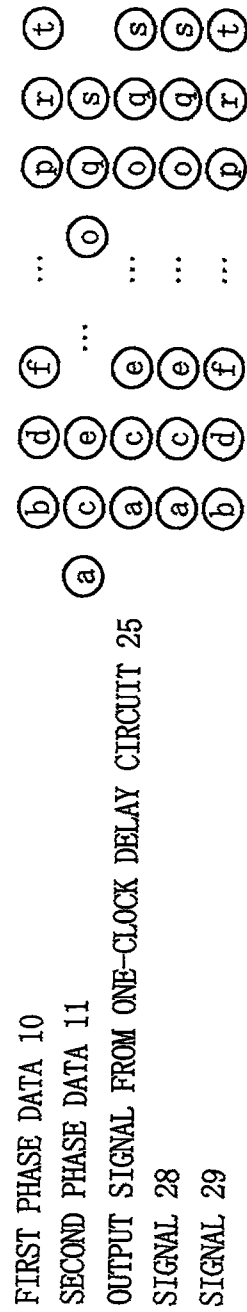


FIG. 16

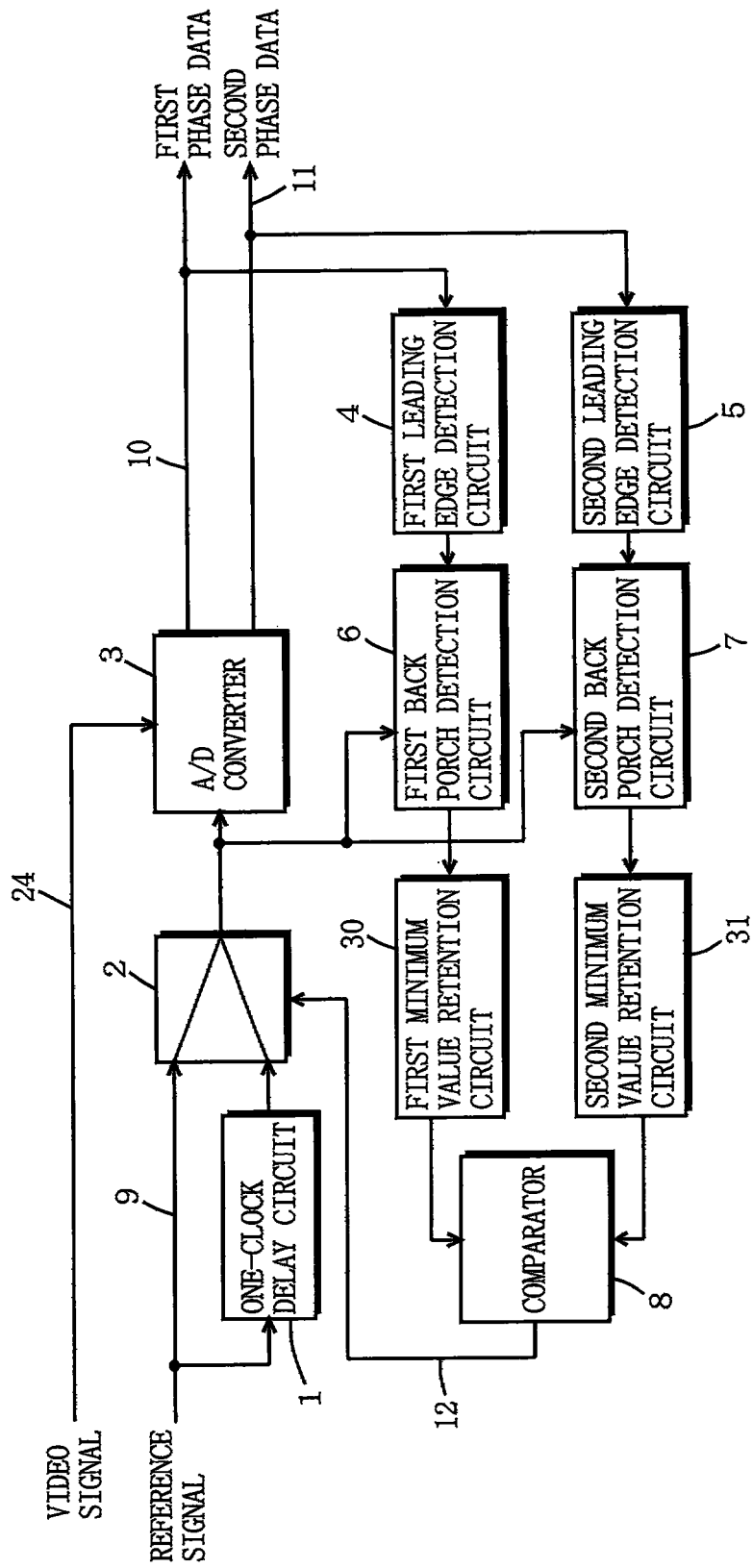


FIG. 17

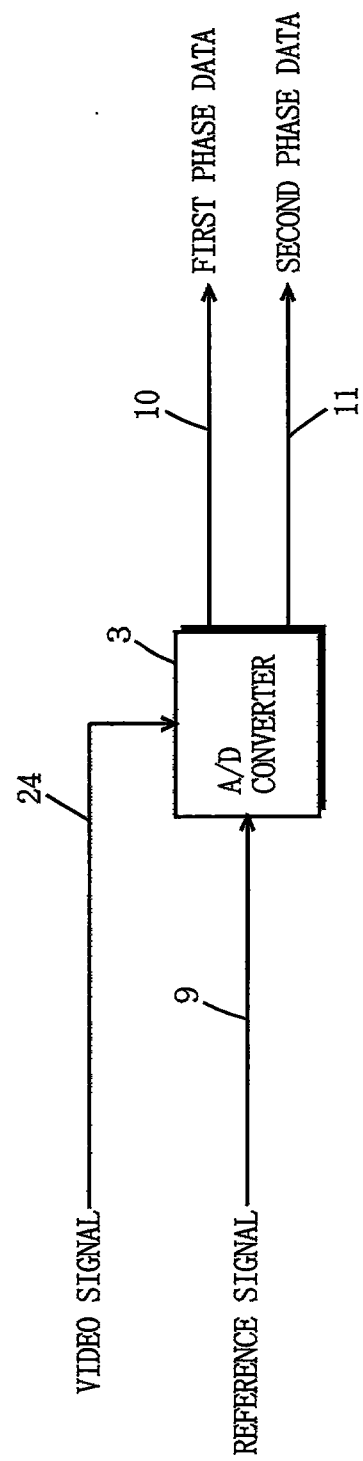


FIG. 18

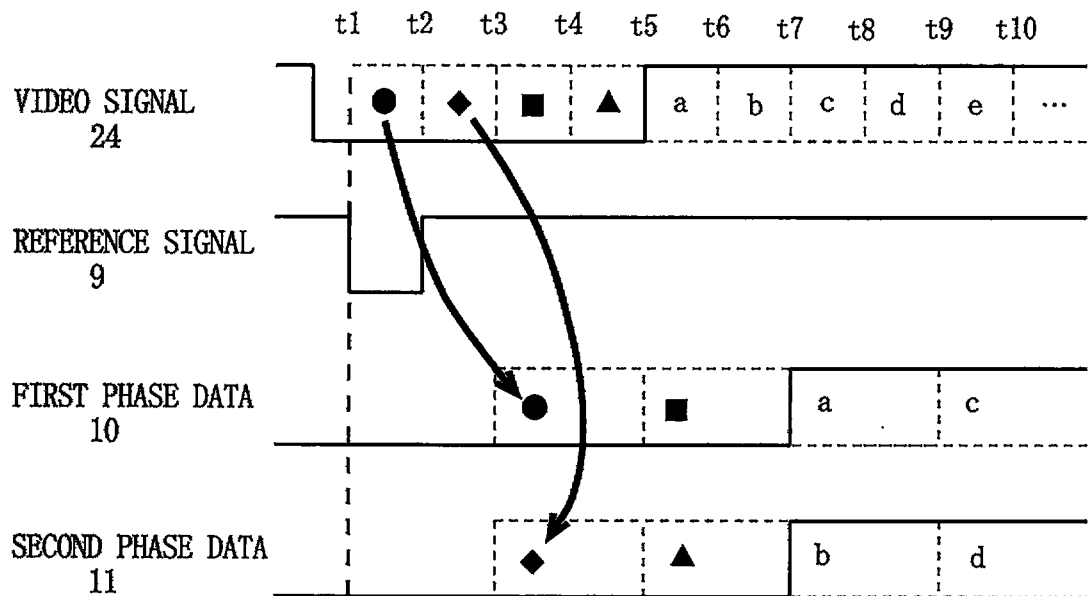


FIG. 19

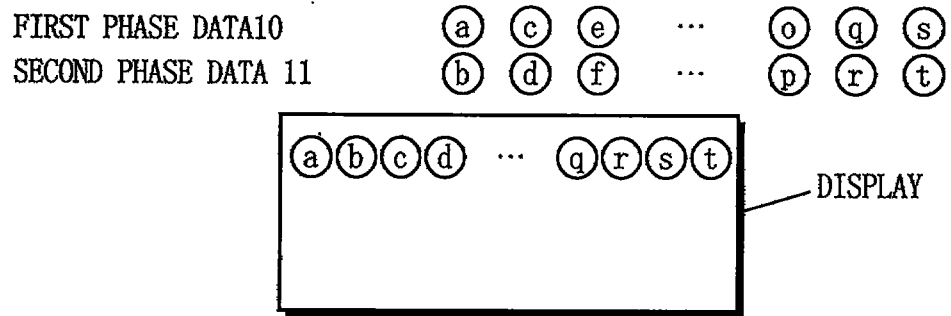


FIG. 20A

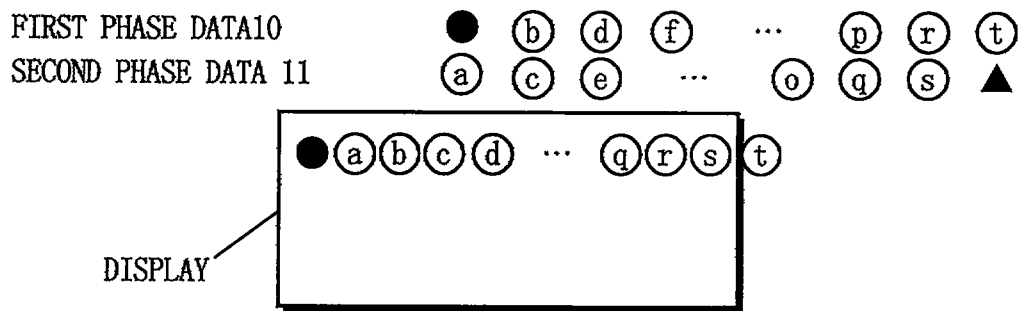
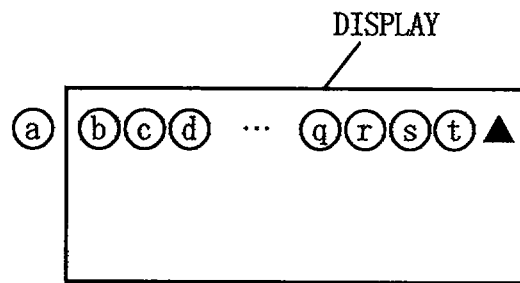


FIG. 20B



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leading edge detection circuit 40 detects the leading edge of the valid video signal region in the video signal 24. Also, the back porch detection circuit 60 detects the back porch period in a similar manner to the above. The back porch period thus detected is provided to the storage part 13. The storage part 13 then provides both the received back porch period and the stored back porch period to the comparator 15. Herein, the received back porch period may be once stored into the storage part 13.

When detecting an input of those two back porch periods, the comparator ¹⁵8 determines whether or not outputting the control signal 12 again based on a result obtained through determination logic, which will be later described. If the control signal 12 is inputted, the multiplexer 2 switches its output signal between the output signal from the one-clock delay circuit 1 and the reference signal 9.

Next, it is described the determination operation of the comparator ¹⁵8 in detail by referring to FIGS. 4 to 6. FIGS. 4 are time charts showing the relationship between the reference signal 9 and the output signal from the storage part 13. Specifically, FIG. 4(a) shows a case where head data (data on the left end on the display) in the valid video signal region is outputted from the first phase of the A/D converter 3, while FIG. 4(b) shows a case where the head data is outputted from the second phase of the A/D converter 3.

FIGS. 5 are time charts showing the flow of data for a case

5 multiplexer 2 is at time t2. Thus, in response to the video signal
24 inputted at time t2, the A/D converter 3 starts the two-phase
processing, outputs data denoted by the blackened square and
triangle at time t4, and outputs the video data *a* and *b* at time
10 t6. Since only the first phase data 10 goes to the leading edge
detection circuit 40 in the video signal processing device of this
embodiment, the leading edge of the output signal from the leading
edge detection circuit 40 is found at time t6. It is thus known
that the back porch number M2 between times t2 and t6 is 4, and
15 rendering M2 always smaller than M1 in value. As such, such
relationship as the above equation (4) is established.

When the above equation (3) is satisfied, the comparator
¹⁵~~8~~ again outputs the control signal 12 to the multiplexer 2. In
response thereto, the multiplexer 2 again goes through its
15 switching operation so as to output the reference signal 9. Once
the reference signal 9 was inputted, the A/D converter 3 can
retains a state that the head data in the valid video signal region
is outputted always from the first phase data. Therefore,
similarly in the first embodiment, the present video signal
20 processing circuit basically has no need to operate once such
state that the head data is outputted always from the first phase
data is retained.

When the above equation (4) is satisfied, the comparator
¹⁵~~8~~ does not output the control signal 12 to the multiplexer 2 so
25 as to let the multiplexer 2 keep selecting the signal from the

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in the image signal source can be easily calculated from frequencies of a horizontal synchronizing signal and a vertical synchronizing signal unique to the image signal source. Based on a result obtained by subjecting each received value to a
5 predetermined determination logic, the comparator 18 outputs the control signal 12 to the multiplexer 2. In response to the control signal 12, the multiplexer 2 switches its output signal between the output signal from the one-clock delay circuit 1 and the reference signal 9. Herein, if the comparator ¹⁸~~8~~ decided not to
10 output the control signal 12 according to the result obtained by the determination logic which will be later described, the multiplexer 2 surely does not go through its switching operation.

Next, it is described in detail the determination operation of the comparator ¹⁸~~8~~ by referring to FIGS. 9. FIGS. 9 are time
15 charts showing the relationship among the detection signal generated in the valid video period detection circuit 17, the first phase data 10, and the second phase data 11. Specifically, FIG. 9(a) shows a case where head data (data on the left end on the display) in the valid video signal region is outputted from
20 the first phase of the A/D converter 3, while FIG. 9(b) shows a case where the head data is outputted from the second phase of the A/D converter 3.

In FIGS. 9, *a* to *t* denote data included in the video signal
24 provided to the A/D converter 3. For convenience, each of *a* to *t* is assumed to be ON. In this embodiment, needless to day,
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the data included in the video signal 24 may be in the black level.

First, as shown in FIG. 9(a), head data (data on the left end on the display) *a* in the valid video signal region is included in the first phase data 10. Thus, the data *b* which is the second from the head is included in the second phase data 11 at the same phase position as *a* in the first phase data. In this manner, the A/D converter 3 subjects 20 pieces of data from data *a* to data *t* to the two-phase processing.

The leading edge and the falling edge of the detection signal generated in the valid video period detection circuit 17 coincide with the leading edge of the first phase data 10 and the falling edge of the second phase data 11, respectively. Accordingly, the data *a* to data *t* fit in a range of a pulse width of the detection signal generated in the valid video period detection circuit 17. If this is the case, as shown in FIG. ⁹~~8~~(a), such relationship as an equation (5) is established between the number of pixels detected by the valid video period detection circuit 17 and the horizontal resolution.

$$\text{Detected Number of Pixels} = \text{Horizontal Resolution}/2 \dots (5)$$

When the above equation (5) is satisfied, the comparator ¹⁸~~8~~ does not output the control signal 12 to the multiplexer 2. The multiplexer 2 thus outputs the reference signal 9 without going through its switching operation. Once the reference signal 9 was inputted, the A/D converter 3 can retain such state that the head data in the valid video signal region is outputted always from

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the first phase data. Accordingly, similarly to the case in the first embodiment, the present video signal processing circuit basically has no need to operate once such state that the head data is always outputted from the first phase data is retained.

5 Next, as shown in FIG. 9(b), the head data (data on the left end of the display) *a* in the valid video signal region is included in the second phase data 11. Thus, the data *b* second from the head is included in the second phase data 11 at a position having the one-clock-delayed phase relationship with the position of *a*
10 in the first phase data. As such, the A/D converter 3 subjects 20 pieces of data from data *a* to data *t* to the two-phase processing.

Here, the leading edge and the falling edge of the detection signal generated in the valid video period detection circuit 17 coincide with the leading edge of the first phase data 10 and the
15 falling edge of the second phase data 11, respectively. Accordingly, the phase of the data *a* which is the head data in the second phase data 11 is delayed by one clock from the leading edge of the first phase data 10, while the phase of the data *t* which is the last data in the first phase data 10 is delayed by
20 one clock from the falling edge of the second phase data 11. Thus, neither data fits in the range of the pulse width of the detection signal generated in the valid video period detection circuit 17.
If so, as shown in FIG. ^{9(b)}~~8(a)~~, the number of pixels detected by the valid video period detection circuit 17 and the horizontal
25 resolution has such relationship as an equation (6) next below.

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Detected Number of Pixels = (Horizontal Resolution/2) -
1 ... (6)

When the above-equation (6) is satisfied, the comparator
¹⁸
~~8~~ outputs the control signal 12 to the multiplexer 2 so as to bring
5 the multiplexer 2 to select a signal from the one-clock delay
circuit 1. In response to the control signal 12, the multiplexer
2 switches its output signal. To be specific, the multiplexer
2 selects a signal from the one-clock delay circuit 1 for output
to the A/D converter 3. Once the signal from the one-clock delay
10 circuit 1 was selected, the A/D converter 3 regards a one-
clock-delayed signal as a reference, retaining the state that the
head data in the valid video signal region is always outputted
from the first phase data. Therefore, similar to the case in the
first embodiment, the present video signal processing circuit
15 basically has no need to operate once the state that the head data
is always outputted from the first phase data is retained.

Note herein that, even if the head data in the valid video
signal region is started to be outputted from the second phase
data in operation, similarly to the case in the first embodiment,
20 the present video signal processing device can retain the state
that the head data in the valid video signal region is always
outputted from the first phase data.

As described in the foregoing, according to such structured
video signal processing device of the present invention that the
25 valid video period detection circuit 17 where receiving pulses

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the black level will be described later.

First, in the case as shown in FIG. 11(a), the head data (data displayed on the led end on the display) *a* in the valid video signal region is included in the first phase data 10. Therefore, 5 the data *b* second from the head is included in the second phase data 11 at the same phase position as the first phase data *a*. As such, the A/D converter 3 subjects 20 pieces of data from data *a* to data *t* to the two-phase processing.

The leading edge and the falling edge of the detection 10 signal generated in the valid video period detection circuit 17 coincide with the leading edge of the second phase data 11 and the falling edge of the first phase data 10, respectively. Accordingly, the data *a* to data *t* fit in a range of the pulse width of the detection signal generated in the valid video period 15 detection circuit 17. If this is the case, as shown in FIG. 11(a), such relationship as an equation (7) is established between the number of pixels detected by the valid video period detection circuit 17 and the horizontal resolution.

$$\text{Detected Number of Pixels} = \text{Horizontal Resolution}/2 \dots (7)$$

20 When the above equation (7) is satisfied, the comparator ¹⁸~~8~~ outputs the control signal 12 to the multiplexer 2 so as to bring the multiplexer 2 to select the reference signal 9. In response to the control signal 12, the multiplexer 2 selects the reference signal 9 corresponding to the control signal for output to the 25 A/D converter 3. Once receiving the reference signal 9, the A/D

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resolution.

$$\text{Detected Number of Pixels} = (\text{Horizontal Resolution}/2) + 1 \dots (8)$$

Since such equation (8) as in the above is established, by taking the above-described equation (7) into consideration, the number of pixels detected by the valid video period detection circuit 17 and the horizontal resolution have such relationship therebetween as an equation (9) if the above equation (8) is expressed by the inequality.

$$\text{Detected Number of Pixels} > \text{Horizontal Resolution}/2 \dots (9)$$

When the above equation (9) is satisfied, the comparator ~~18~~¹⁸ outputs the control signal 12 to the multiplexer 2 so as to bring the multiplexer 2 to select the signal from the one-clock delay circuit 1. In response to the control signal 12, the multiplexer 2 switches its output signal. Once the signal from the one-clock delay circuit was selected, the A/D converter 3 starts regarding a signal whose phase is delayed by one clock as a reference, retaining a state that the head data in the valid video signal region is always outputted from the first phase data. Therefore, once retaining the state that the head data is always outputted from the first phase data, similar to the case in the first embodiment, the present video signal processing circuit basically has no need to operate thereafter.

Note herein that, even if the head data in the valid video

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signal region is started to be outputted from the second phase data in operation, similarly to the case in the first embodiment, the present video signal processing device can retain the state that the head data in the valid video signal region is always
5 outputted from the first phase data.

In FIGS. 11, described next is a case where an arbitrary pixel is OFF. A state that the video signal 24 is always one pixel short on the display is observed only when the above equation (9) is satisfied. This is because, such pixel shortage is not
10 observed when the head or the last of the video data is in the black level, but the video data needs to be ON at both ends in order to satisfy the equation (9).

Thus, when an equation (10) is satisfied, the comparator ¹⁸~~8~~ retains the output state from the multiplexer 2 for output to
15 the A/D converter without any change.

$$\text{Detected Number of Pixels} \leq \text{Horizontal Resolution}/2 \quad \dots$$

(10)

When the above-described equation (9) is satisfied, the comparator ¹⁸~~8~~ outputs the control signal 12 so as to switch the
20 output from the multiplexer 2. With such operation of the comparator ¹⁸~~8~~, the present video signal processing device can bring the display to display a video without pixel shortage.

As described in the foregoing, according to such structured present video signal processing device that the valid video period
25 detection circuit 17 where receiving detection pulses detected

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by the leading edge detection circuit 40 and the falling edge detection circuit 16 detects the number of pixels, and the comparator 18 receives the detected number of pixels and a value half of the horizontal resolution for comparison, a display can assuredly display every video signal thereon.

In this embodiment, similarly to the case in the first embodiment, the one-clock delay circuit 1 may be any type of circuit as far as the reference signal 9 is delayed by the odd number of clocks therein. Also, the A/D converter 3 may be the one carrying out four-phase processing or six-phase processing, which can easily operate in a similar manner.

(Fifth Embodiment)

FIG. 12 is a block diagram showing the structure of a video signal processing device according to a fifth embodiment of the present invention. In FIG. 12, the present video signal processing device is almost identical in structure to the above-described video signal processing device of the third embodiment in FIG. 7. Note that, the present video signal processing device is provided with a first leading edge detection circuit 4, a first falling edge detection circuit ¹⁶~~160~~, and a first valid video period detection circuit 20 instead of the leading edge detection circuit 40, the falling edge detection circuit ¹⁶~~160~~, and the valid video period detection circuit 17 in FIG. 7. And therein, a second leading edge detection circuit 5, a second falling edge detection circuit 21, and a second valid video period

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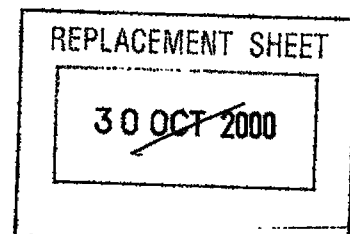
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detection circuit 22 are additionally provided. These are the differences from the above-described video signal processing device of the third embodiment. Thus, in the present video signal processing device, any constituent identical to that in the video
5 signal processing device of the third embodiment is under the same reference numeral, and is not described again. Herein, a comparator 23 is different from the comparator ¹⁸~~15~~ in reference numeral since receiving a signal different from the one thereto.

Focusing on a signal applied to the leading edge detection
10 circuits, the falling edge detection circuits, and the valid video period detection circuits, the present video signal processing device may be a combination, in structure, of the video signal processing device of the above-described third embodiment in FIG. 7 and the video signal processing device of the above-described
15 fourth embodiment in FIG. 10. Details are described below.

As described in the foregoing, the video signal processing devices of the third and fourth embodiments have to detect the horizontal resolution in the image signal source. This horizontal resolution in the image signal source can be estimated
20 by detecting, generally, the frequencies of the horizontal synchronizing signal and the vertical synchronizing signal from the respective image signal sources. In the recent market, however, such estimation of the horizontal resolution in the frequencies of the horizontal synchronizing signal and the
25 vertical synchronizing signal may not be applicable to some image

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signal sources.

Therefore, in order to bring the display deal with such image signal sources, the device needs to be differently structured so as to recognize such image signal sources. Moreover, if such image signal sources vary in type, the device thus differently-structured becomes larger in size, enlarging the circuit in its entirety.

By taking these into consideration, the video signal processing device of this embodiment can easily clear the above-described problems with the structure as shown in FIG. 12. Next below, the operation of the present video signal processing device is described by referring to FIGS. 13.

FIGS. 13 are time charts showing the relationship among the detection signals generated in the valid video period detection circuits ²⁰~~17~~ and 22, the first phase data 10, and the second phase data 11. Specifically, FIG. 13(a) shows a case where the head data (data on the left end on the display) in the valid video signal region is included in the first phase of the A/D converter 3, while FIG. 13(b) shows a case where the head data is included in the second phase of the A/D converter 3.

In FIGS. 13, *a* to *t* denote data included in the video signal 24 provided to the A/D converter 3. For convenience, each of *a* to *t* is assumed to be ON.

First, as shown in FIG. ¹³~~11~~(a), the head data (data on the left end on the display) *a* in the valid video signal region is

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²³
8 outputs the control signal 12 to the multiplexer 2 so as to bring the multiplexer 2 to select the reference signal 9. In response to the control signal 12, the multiplexer 2 selects the reference signal 9 corresponding to the control signal for output to the A/D converter 3. As such, once receiving the reference signal 9, the A/D converter 3 can retain a state that the head data in the valid video signal region is always outputted from the first phase data. Therefore, once retaining the state that the head data is always outputted from the first phase data, the present video signal processing circuit basically has no need to operate thereafter.

Next, as shown in FIG. 13(b), the head data (data on the left end of the display) *a* in the valid video signal region is included in the second phase data 11. Thus, the data *b* second from the head is included in the second phase data 11 at a position having the one-clock-delayed phase relationship with the position of *a* in the first phase data. As such, the A/D converter 3 subjects 20 pieces of data from data *a* to data *t* to the two-phase processing.

The leading edge and falling edge of the detection signal generated in the valid video period detection circuit 17 coincide with the leading edge of the first phase data 10 and the falling edge of the second phase data 11, respectively. This is the same operation as the video signal processing device of the third embodiment, that is, the same as the above-described case shown in FIG. 9 (b). The leading edge and falling edge of the detection

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signal generated in the valid video period detection circuit 22 coincide with the leading edge of the second phase data 11 and the falling edge of the first phase data 10, respectively. This is the same operation as the video signal processing device of the fourth embodiment, that is, the same as the above-described case shown in FIG. ~~8~~¹¹(b).

Therefore, as shown in FIG. 13^(b)~~(a)~~, such relationship as an equation (12) below is established between a pulse width PW1 of the detection signal generated in the valid video period detection circuit 17 and a pulse width PW2 of the detection signal generated in the valid video period detection circuit 22.

$$PW1 < PW2 \quad \dots (12)$$

When the above equation (12) is satisfied, the comparator ~~8~~²³ outputs the control signal 12 to the multiplexer 2 so as to let the multiplexer 2 select the signal from the one-clock delay circuit 1. In response to the control signal 12, the multiplexer 2 switches its output signal. To be specific, the multiplexer 2 selects the signal from the one-clock delay circuit 1 for output to the multiplexer 2. Once the signal from the one-clock delay circuit 1 was selected, the A/D converter 3 regards a signal whose phase is delayed by one clock as a reference, and thus, such state that the head data in the valid video signal region is always outputted from the first phase data can be retained. As such, similarly to the case in the first embodiment, the present video signal processing circuit has no need to operate once such state

that the head data is always outputted from the first phase data is retained.

Note herein that, even if the head data in the valid video signal region is started to be outputted from the second phase data in operation, similarly to the case in the first embodiment, the present video signal processing device can retain the state that the head data in the valid video signal region is always outputted from the first phase data.

Next, in FIG. ¹³11(a), described is a case where only the video data *a* and *t* is OFF. In such case, the head data is not included in the first phase data 10, and the last data of the video data is not included in the second phase data 11. That is in the same state as in FIG. 11(b). With the above equation (12) established, the comparator ²³8 thus outputs the control signal 12 to the multiplexer 2 so as to bring the multiplexer 2 to select the signal from the one-clock delay circuit 1. In response to the control signal 12, the multiplexer 2 switches its output signal. To be specific, the multiplexer 2 selects the signal from the one-clock delay circuit 1 for output to the A/D converter 3. Once the signal from the one-clock delay circuit 1, the A/D converter 3 regards a signal whose phase is delayed by one clock as a reference, and thus, the state that the head data in the valid video signal region is always outputted from the first phase data.

At this time, the head data *a* in the video signal 24 is included in the second phase data 11. This may sound that the

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status is not ideal. However, since the video data a and t is the black data, the data has pixel shortage from the beginning, and thus does not cause such problem as described in the foregoing if shown on the display as it is. In FIG. 11(b), when only the video data a and t is OFF, the similar description is applicable.

Further, in FIG. ¹³~~11~~(a), it is described a case where any arbitrary pixel excepting for the video data a and t is OFF. In this case, when the video data b or s is the black data, PW1 becomes larger than PW2. Accordingly, when the following equation (13) is established, the comparator ²³~~8~~ retains the output state of the multiplexer 2, and outputs the same to the multiplexer 2 as it is.

$$PW1 \leq PW2 \quad \dots (13)$$

In FIG. ¹³~~11~~(b), when any arbitrary pixel excepting for the video data a and t is OFF, the above equation (12) is applicable.

As is known from the above, when the above equation (13) is satisfied, the comparator ²³~~8~~ does not output the control signal 12 to the multiplexer 12 so that the state for the output signal in the multiplexer 2 is retained. When the above equation (12) is satisfied, the comparator ²³~~8~~ outputs the control signal 12 to the multiplexer 2 so as to bring the multiplexer 2 to switch its output signal. By such operation, the present video signal processing device can always let the display display the video without pixel shortage.

Herein, in this embodiment, similarly to the case in the

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Next, in the present video signal processing device, the multiplexer 26 receives the first phase data 10, and a signal outputted from the one-clock delay circuit 25 where receiving the second phase data 11, that is, the one-clock delayed second phase data 11. The multiplexer 27 receives the first phase data 10 and the second phase data 11. When the present video signal processing device is activated, the multiplexer 26 selects the first phase data 10 for output, while the multiplexer ²⁷~~26~~ selects the second phase data 11 for output. Thereafter, in response to the control signal 12 outputted from the comparator 8, the multiplexer 26 switches itself to select the one-clock-delayed second phase data 11 for output, while the multiplexer ²⁷~~26~~ switches itself to select the first phase data 10 for output.

On comparison between the video signal processing device of the first embodiment, the operation of such structured video signal processing device of this embodiment is described by referring to FIGS. 15.

FIGS. 15 are schematic diagrams showing the relationship among the first phase data 10, the second phase data 11, an output signal 28 from the multiplexer 26, and an output signal 29 from the multiplexer 27. In FIGS. 15, *a* to *t* denote data included in the video signal 24 going to the A/D converter 3. Specifically, FIG. 15(a) shows a case where the head data (data displayed on the left end on the display) in the valid video signal region is included in the first phase data 10 from the A/D converter 3, while

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FIG. 15(b) shows a case where the head data is included in the second phase data 11 from the A/D converter 11.

First, in such case as shown in FIG. 15(a), the comparator 8 operates in a similar manner to the video signal processing device of the first embodiment. That is, as described in the foregoing, when the above equation (1) is satisfied, the comparator 8 does not output the control signal 12 to the multiplexers. Accordingly, as described in the foregoing, the multiplexers 26 and 27 select, without going through its switching operation, the first phase data 10 and the second phase data 11 outputted from the A/D converter 3, respectively, for output. In this manner, the present video signal processing device can retain the state that the head data in the valid video signal region is always outputted from the first phase data. Therefore, once retaining the state that the head data is always outputted from the first phase data, the present video signal processing circuit basically has no need to operate thereafter.

Next, similarly in such case as shown in FIG. 15(b), the comparator 8 operates in the same manner as the video signal processing device of the first embodiment. To be specific, as described in the foregoing, when the above equation (2) is satisfied, the comparator 8 outputs the control signal 12 to the multiplexers. Accordingly, in response to the control signal 12, the multiplexers ²⁶/₂₅ and ²⁷/₂₈ going through the above-described switching operation. In detail, the multiplexer 26 switches

itself to select the one-clock delayed second phase data 11 for output, while the multiplexer ²⁷/₂₆ switches itself to select the first phase data 10 for output. In such manner, the present video signal processing device can retain the state that the head data
5 in the valid video signal region is always outputted from the first phase data. Therefore, once retaining the state that the head data is always outputted from the first phase data, the present video signal processing circuit basically has no need to operate thereafter.

10 Note herein that, even if the head data in the valid video signal region is started to be outputted from the second phase data in operation, the present video signal processing device can retain the state that the head data in the valid video signal region is always outputted from the first phase data.

15 As is known from the above, the video signal processing device of this embodiment can deal with an image signal source having higher resolution, and can assuredly let the display display every video signal thereon.

Note herein that, the video signal processing device of this
20 embodiment can be provided with first and second falling edge detection circuits instead of the first and second leading edge detection circuits 4 and 5. With such structure, the first and second back porch detection circuits 6 and 7 operate to detect a period including the back porch period and the valid video signal
25 period. Thus, with such structure, the video signal processing

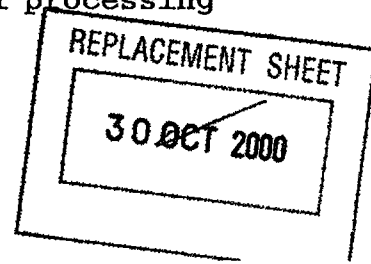
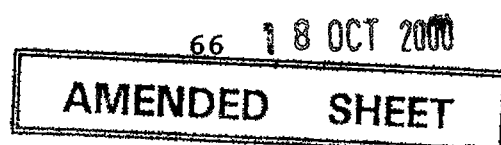


FIG. 13A

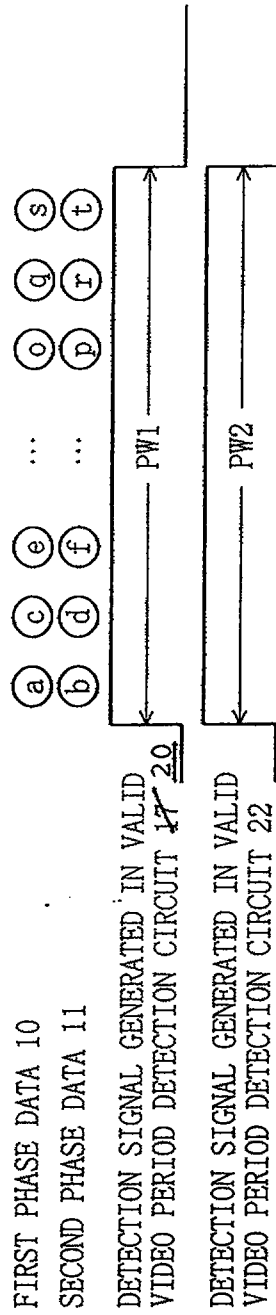
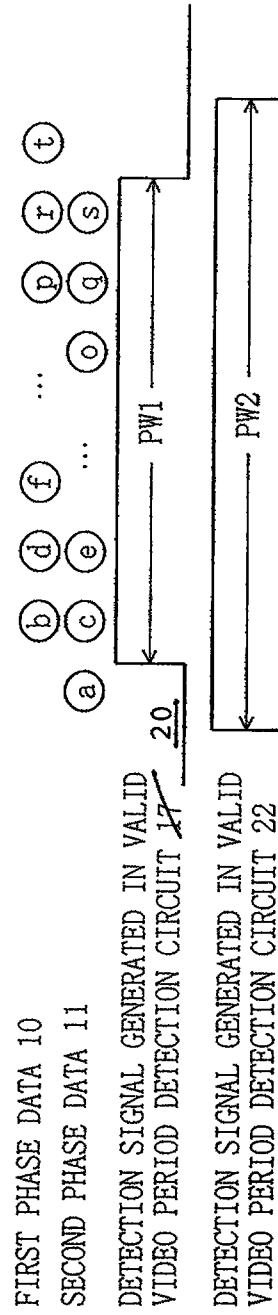


FIG. 13B



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