

## CLAIMS

1. Process for manufacturing a deep junction electronic device comprising the steps of:

- 5                   a) Providing a substrate (1) of a monocrystalline semiconductor material, said substrate having a plane surface (9);
- b) Depositing a layer (5) of non monocrystalline semiconductor material on said plane surface (9), said layer (5) of non monocrystalline semiconductor material having an external  
10                   surface (19);
- c) Incorporating inactivated dopant elements prior to step b) into said substrate (1) and/or, respectively, during or after step b) into said layer (5) of non monocrystalline semiconductor material, so as to form an inactivated doped layer (27) of monocrystalline  
15                   semiconductor material and/or, respectively, an inactivated doped layer (7) of non monocrystalline semiconductor material;
- d) Exposing, after the step c), an area of said external surface (19) formed at step b) to a laser thermal anneal beam (30) having a density of energy higher than a determined threshold, so as to  
20                   melt the layer (5) of non monocrystalline semiconductor material within a volume defined by said laser thermal anneal beam down to an interface with the substrate (1), and so as to activate said dopant elements incorporated at step c) ;
- e) Stopping exposure of said area to said laser thermal anneal beam  
25                   so as to induce epi-like crystallization of said layer (5) of non monocrystalline semiconductor material from said interface (6, 8) with the substrate (1) and formation of epi-like monocrystalline semiconductor material (15) extending over said volume between said interface and said external surface (19), wherein said  
30                   substrate (1) and/or, respectively, said epi-like monocrystalline semiconductor material (15), comprises a layer (17, 27) of activated doped monocrystalline semiconductor material.

2. Process for manufacturing a deep junction electronic device according to claim 1 wherein during step d) said laser beam (30) is an excimer laser beam

having a laser wavelength in the range of absorption of said non monocrystalline semiconductor material.

3. Process for manufacturing a deep junction electronic device according to claim 2 further comprising another step of cleaning said surface (9) of the substrate (1) prior to step b), so as to remove any oxide layer from said surface (9).

4. Process for manufacturing a deep junction electronic device according to claim 1 wherein the step c) comprises a step c1) which is performed after step a) and prior to step b), said step c1) comprising exposure of said surface (9) of the substrate (1) to an ion implantation beam (40) so as to implant said inactivated dopant elements into the monocrystalline semiconductor substrate (1) and to form a layer (27) of monocrystalline semiconductor material doped by said inactivated dopant elements and extending from said plane surface (9) into the monocrystalline semiconductor substrate (1).

5. Process for manufacturing a deep junction electronic device according to claim 4 wherein the step c) comprises a step c2) which is performed during b), said step c2) comprising the incorporation of dopant elements into the layer (5) of non monocrystalline semiconductor material.

6. Process for manufacturing a deep junction electronic device according to claim 5 wherein the layer (37) of activated doped monocrystalline semiconductor is doped with a first dopant type and the layer (17) of activated doped epi-like monocrystalline semiconductor is doped with a second dopant type.

7. Process for manufacturing a deep junction electronic device according to claim 5 further comprising another step of cleaning said surface (9) of the substrate (1) prior to step b), so as to remove any oxide layer from said surface (9).

8. Process for manufacturing a deep junction electronic device according to claim 4 wherein the step c) comprises a step c3) which is performed after the steps a) and b), said step c3) comprising exposure of said layer (5) of non monocrystalline semiconductor material to an ion implantation beam (40) so as to implant said inactivated dopant elements into the layer (5) of non monocrystalline semiconductor material and to form a layer (7) of non monocrystalline semiconductor material doped by said inactivated dopant elements.

9. Process for manufacturing a deep junction electronic device according

to claim 8 wherein the layer (37) of activated doped monocrystalline semiconductor is doped with a first dopant type and the layer (17) of activated doped epi-like monocrystalline semiconductor is doped with a second dopant type.

10. Process for manufacturing a deep junction electronic device  
5 according to claim 4 further comprising another step of cleaning said surface (9) of the substrate (1) prior to step b), so as to remove any oxide layer from said surface (9).

11. Process for manufacturing a deep junction electronic device  
10 according to claim 1 further comprising another step of cleaning said surface (9) of the substrate (1) prior to step b), so as to remove any oxide layer from said surface (9).

12. Process for manufacturing a deep junction electronic device according to claim 1 wherein the semiconductor material is selected among silicon and germanium.

13. Process according to claim 1 wherein said step c) of incorporating  
15 inactivated dopant elements is achieved so as to incorporate dopant elements with a gradient profile along a direction transverse to the plane surface (9) of the substrate (1).

14. Process for manufacturing a deep junction electronic device  
20 according to claim 1 wherein the layer (15) of epi-like monocrystalline semiconductor material has a thickness comprised between 500 nanometers and 3 micrometers.

15. Process for manufacturing a deep junction electronic device  
25 according to claim 1 wherein at step d) said laser beam is an excimer laser beam having an energy density in the range from 0.1 to 10 J/cm<sup>2</sup> and a laser wavelength lower than 600 nanometers.

16 Process for manufacturing a deep junction electronic device according to claim 1 wherein said steps d) and e) are performed in a gaseous atmosphere selected among an inert gas, air or vacuum and under controlled pressure and  
30 temperature.

17. Process for manufacturing a deep junction electronic device according to claim 1 further comprising a step of measuring an optical beam reflected on the external surface of the layer (5) of non monocrystalline semiconductor material so as to control full melt of said layer (5) of non

monocrystalline semiconductor material during said step d), and so as to control epi-like crystallization of said layer (15) during said step e).

18. Process for manufacturing a deep junction electronic device according to claim 1 wherein the step c) comprises a step c3) which is performed  
5 after the steps a) and b), said step c3) comprising exposure of said layer (5) of non monocrystalline semiconductor material to an ion implantation beam (40) so as to implant said inactivated dopant elements into the layer (5) of non monocrystalline semiconductor material and to form a layer (7) of non monocrystalline semiconductor material doped by said inactivated dopant elements.

10 19. Process for manufacturing a deep junction electronic device according to claim 1 wherein the step c) comprises a step c2) which is performed during step b), said step c2) comprising the incorporation of dopant elements into the layer (5) of non monocrystalline semiconductor material.

20. Deep junction electronic device comprising a monocrystalline  
15 semiconductor substrate (1), said deep junction electronic device comprises a layer (15) of epi-like monocrystalline semiconductor material (15) having an external surface (19) and an interface (6,8) with said monocrystalline semiconductor substrate (1), and wherein said monocrystalline semiconductor substrate (1), and/or, respectively, said layer (15) of epi-like monocrystalline  
20 semiconductor material (15), comprises a layer (17, 27) of activated doped monocrystalline semiconductor material, wherein said interface (6, 8) is located at a depth comprised between 1 and 5 micrometers from said external surface, and wherein the doping profile of said layer (17, 27) of activated doped monocrystalline semiconductor material is a non-Gaussian profile.