

**A semiconductor wafer and a method for producing the
semiconductor wafer**

5 The invention is directed to a semiconductor wafer comprising a silicon single crystal substrate having a top surface and a stack of layers covering the top surface, and to a method for producing the semiconductor wafer. Specifically, the invention is directed to a layered semiconductor wafer comprising a
10 silicon single crystal substrate having Group III-nitride heteroepitaxial layers deposited thereon.

The layered semiconductor wafer is useful as a source for producing electronic and optoelectronic devices, e.g. high-
15 power devices, high-frequency devices like HEMTs (high electron mobility transistors) and light-emitting devices like LEDs (light emitting diodes) and light-detector devices like UV detectors.

20 There is a considerable crystal lattice mismatch between silicon and Group III-nitrides like e.g. AlN, AlGa_N, GaN, and AlInGa_N, and a considerable mismatch in regard of coefficients of thermal expansion (CTE). Crystal lattice mismatch and CTE mismatch induce film stress and cause serious problems like
25 poor crystal quality due to formation of dislocations, as well as a deformation by bowing of the layered semiconductor wafer or even cracking of the Group III-nitride layers or the whole layered semiconductor wafer. CTE mismatch produces significant tensile stress after cooling of the layered semiconductor
30 wafer.

Various attempts have been made to reduce film stress. According to US 2009/0008647 Al crack-free layers can be grown by using e.g. graded AlGa_N buffer layers, AlN interlayers,
35 AlN/GaN or AlGa_N/GaN-based superlattices, or an in-situ silicon

nitride masking step. Although the presence of e.g. an AlGaN buffer layer may provide some compressive stress which counteracts tensile stress caused by CTE mismatch after cooling from the deposition temperature, this counteracting stress is not sufficient for a complete compensation. As a consequence, the deformation of the layered semiconductor wafer after cooling from the deposition temperature remains an issue.

Therefore, it is an object of the claimed invention to provide a proper solution to this problem.

The claimed invention is directed to a semiconductor wafer comprising a silicon single crystal substrate having a top surface and a stack of layers covering the top surface, the stack of layers comprising

an AlN nucleation layer which covers the top surface of the silicon single crystal substrate, wherein the top surface of the silicon single crystal substrate has a crystal lattice orientation which is off-oriented with respect to the {111}-plane, the normal to the top surface being inclined with respect to the <111>-direction toward the <11-2>-direction by an inclination angle θ of not less than 0.3° and not more than 6° , the azimuthal tolerance of the inclination being $\pm 0.1^\circ$; and

an AlGaN buffer layer which covers the AlN nucleation layer and comprises one or more $\text{Al}_x\text{Ga}_{1-x}\text{N}$ layers, wherein $0 < x < 1$.

In addition, the claimed invention is directed to a method for producing a semiconductor wafer comprising a silicon single crystal substrate having a top surface and a stack of layers covering the top surface, the method comprising

providing the silicon single crystal substrate having a top surface, the top surface of the silicon single crystal substrate having a crystal lattice orientation which is off-

oriented with respect to the {111}-plane, the normal to the top

surface being inclined with respect to the $\langle 111 \rangle$ -direction toward the $\langle 11-2 \rangle$ -direction by an inclination angle θ of not less than 0.3° and not more than 6° , the azimuthal tolerance of the inclination being $\pm 0.1^\circ$;

- 5 depositing on the top surface of the silicon single crystal substrate an AlN nucleation layer which covers the top surface of the silicon single crystal substrate;
depositing an AlGa_xN buffer layer which covers the AlN nucleation layer and comprises one or more Al_xGa_{1-x}N layers,
10 wherein $0 < x < 1$.

"A layer covering another layer" has the meaning herein that the layer covers the other layer directly or that one or more intermediate layers between the layer and the other layer
15 exist.

"AlGa_xN buffer layer" means one or more layers having a composition Al_xGa_{1-x}N, wherein $0 < x < 1$. The composition can be constant or graded. A graded composition can be stepwise or
20 continuously graded. Various Al_xGa_{1-x}N layers participating in forming the AlGa_xN buffer layer can have the same or different compositions. The AlGa_xN buffer layer may comprise further layers, in particular one or more further AlN layers, one or more GaN layers and a combination of AlN and GaN layers. The
25 top surface of the AlGa_xN buffer layer is a group-III polar nitride surface.

It is preferred that the stack of layers comprises one or more device forming layers, e.g. layers which are suitable for being
30 processed to electronic or optoelectronic devices. The one or more device forming layers cover the AlGa_xN buffer layer and have a composition of a binary, ternary or quaternary Group III-nitride consisting of at least one of the elements Al, Ga and In.

The inventors of the present invention found that providing a silicon single crystal substrate having a top surface with the claimed off-orientation will improve the properties of an AlN nucleation layer which is grown on the top surface of the silicon single crystal substrate. The off-orientation of the top surface promotes the coalescence of small islands at the initial stage of the growth and favors the growth of AlN islands having larger dimensions as compared to the dimensions of AlN islands initially growing on an exactly {111}-oriented silicon single crystal substrate. When coalescing during the formation of the AlN nucleation layer, larger AlN islands induce less tensile stress to the AlN layer as compared to smaller AlN islands. As a result the stress state of the AlN nucleation layer is less tensile or even relaxed in comparison to the stress state of an AlN nucleation layer deposited on an exactly {111}-oriented silicon single crystal substrate. In addition, the growth of larger AlN islands promote that less pits are formed in the AlN nucleation layer. The density of pits in the AlN nucleation layer should be as low as possible since it negatively affects the quality of an AlGaN buffer layer which is grown on the AlN nucleation layer.

Due to reduced tensile stress in the AlN nucleation layer, more compressive stress will build up in the AlGaN buffer layer and, where appropriate, in the device forming layer(s). Accordingly, the potential of the AlGaN buffer layer and, where appropriate, of the device forming layer(s) increases to provide compressive stress which counteracts tensile stress caused by CTE mismatch after cooling of the layered wafer from the deposition temperature. Therefore, deformation of the layered wafer may become considerably less and its bow may be significantly reduced.

The inclination angle θ between the $\langle 111 \rangle$ -direction and the normal to the top surface of the silicon single crystal

substrate is chosen to be not less than 0.3° and not more than 6° , preferably not less than 0.8° and not more than 5.5° . In this case terraces are present on the top surface of the silicon single crystal substrate. The terraces promote the initial growth of large AlN islands. If the inclination angle θ is less than 0.3° , the improvement regarding the properties of the AlN nucleation layer becomes insignificant. If the inclination angle θ is more than 6° , a homogeneous AlN nucleation layer cannot be grown due to a low aspect ratio of the terraces present on the top surface of the silicon single crystal substrate. However, the growth parameters, e.g. growth temperature, pressure, and ratio between metal organic (MO) precursor and NH_3 in the gas phase also influence the AlN nucleation islands and consequently the post-deposition bow of the layered semiconductor wafer. An azimuthal variation tolerance range of the inclination of the normal to the top surface is $\pm 0.1^\circ$.

The AlN nucleation layer has a thickness which is preferably not less than 20 nm and not more than 500 nm.

The silicon single crystal substrate is preferably a silicon single crystal wafer having a polished front side representing the off-oriented top surface. Alternatively, a silicon single crystal epi-wafer or a SOI-wafer can be used as the silicon single crystal substrate. It is preferred that the silicon single crystal substrate has a circular shape with a diameter which is not less than 150 mm. It is also preferred that the silicon single crystal substrate is provided with one or more orientation marks, e.g. with a flat or a notch.

It is further preferred to grow the AlN nucleation layer, the AlGaN buffer layer and, where appropriate, the device forming layer(s) using metal-organic chemical vapor deposition (MOCVD) in a conventional MOCVD-reactor. The temperature of the surface

on which the layer is deposited is preferably 700°C or more and 1200°C or less, if the deposited layer comprises Al, and preferably 550°C or more and 1150°C or less, if Al is absent in the deposited layer.

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The invention is further explained by referring to figures and examples.

Fig.1 represents a silicon single crystal substrate having an off-oriented top surface in accordance with the invention.

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Fig.2 shows a comparison in regard to the morphology of an AlN layer having 50 nm thickness revealed by AFM technique.

Fig.3 shows a silicon single crystal substrate which is covered by a stack of layers and represents a typical structure for the fabrication of power devices.

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Fig.4 shows the result of wafer bow measurements of a layered structure according to Fig.3.

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Fig.5 shows the plot of the bow of a layered structure according to Fig.3 depending on the inclination angle θ .

According to Fig.1, the silicon single crystal substrate has a top surface 1 which is off-oriented with respect to the {111}-plane. The normal N to the top surface is inclined with respect to the <111>-direction by an inclination angle θ which is not less than 0.3° and not more than 6°. The normal N to the top surface 1 is inclined toward the <11-2>-direction. An azimuthal variation tolerance range of the inclination of the normal N to the top surface is plus to minus angle ϕ , wherein $\phi=0.1^\circ$. Angle ϕ represents the angle between the projection of the normal N to the top surface onto the {111}-plane and the <11-2>-direction. The top surface 1 can have any off-orientation which

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is geometrically equivalent. For example, the normal N to the top surface can be inclined toward the [11-2]-direction, the [1-21]-direction or the [-211]-direction.

5 Examples:

Polished silicon single crystal wafers having a diameter of 150 mm have been used as a silicon single crystal substrate in accordance with the invention. Group-III nitride layers were deposited in a commercial MOCVD reactor.

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AlN nucleation layer:

The behavior of the formation of an AlN nucleation layer was studied by growing AlN nucleation layers having a thickness of 10nm, 50nm and 350nm, respectively. The growth was started with
15 a pre-flow of an Al metal-organic precursor, TMAI (trimethylaluminium), before introduction of ammonia into the growth chamber. The temperature of the substrate surface during AlN deposition was 1010°C. Fig.2 shows a comparison of the morphology of an AlN layer having a thickness of 50 nm revealed
20 by AFM (atomic force microscope) technique. The illustration on the left-hand side depicts an AFM image of an AlN layer which was grown on a (111)-oriented, polished silicon single crystal wafer which is called hereinafter an on-oriented substrate. The illustration on the right-hand side depicts an AFM image of an
25 AlN layer which was grown on a polished silicon single crystal wafer which was off-oriented in accordance with the invention. The inclination angle θ was 1° and the inclination was exactly toward the [11-2]-direction.

30 As can be derived from Fig.2, the pit density was significantly lower when the AlN nucleation layer was grown on the off-oriented substrate. Actually, the pit density was about $1.1 \times 10^{10}/\text{cm}^2$ in case the on-oriented substrate was used and about $2.7 \times 10^9/\text{cm}^2$ in case that the off-oriented substrate was used.

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Table 1 displays the results of Raman and x-ray diffraction (XRD) measurements which were performed in order to investigate the stress status and layer quality of a grown AlN nucleation layer having a thickness of 350 nm.

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Table 1

thickness (nm)	orientation	AlN E_2^2 phonon energy (cm^{-1})	stress (GPa)	XRD (002) FWHM (arc sec)
350	on-oriented	650.23	1.138	851
350	1° off-oriented	650.96	1.022	650

According to table 1, the layer stress was positive, i.e.

10 tensile, with regard to both samples, but less tensile stress was induced in case that the AlN nucleation layer was grown on the off-oriented substrate. After the AlN layer deposition the bow of the layered sample with on-orientation was $-29.15 \mu\text{m}$ (average bow value) and more concave than the bow of the
15 layered sample with off-orientation which was $-27.16 \mu\text{m}$. This corroborates that the AlN epi layer is less tensile strained on the off-oriented Si(111) substrate than on the on-oriented Si(111) substrate. The full width at half maximum (FWHM) data as determined by XRD can be related to the presence of layer
20 defects. The smaller FWHM is attributed to a lower number of crystal defects detected in the AlN layer covering the off-oriented substrate.

AlGaN buffer layer:

25 The influence of the substrate orientation on the AlGaN buffer layer was studied in a further experiment. First of all, the AlN nucleation layer was deposited as described in the previous experiment and then the AlGaN buffer layer was deposited on the

AlN nucleation layer and consisted of three layers:

Al_{0.75}Ga_{0.25}N/Al_{0.45}Ga_{0.55}N/Al_{0.19}Ga_{0.81}N. The growth temperature was 1010°C. The layers had a thickness of 400 nm, 400 nm and 450 nm, respectively, and the Al_{0.75}Ga_{0.25}N-layer covered the AlN nucleation layer.

Table 2 displays the results of deformation measurements determining the bow of the layered wafer resolved in x- and y-direction, i.e perpendicular and parallel to the [1-10]-direction.

Table 2

orientation	bow x (μm)	bow y (μm)
on-oriented	15.3	14.0
1° off-oriented	45.5	43.1

Higher positive bow values in x-direction and y-direction indicated an increased convex bow.

Power device stack of layers:

In a further experiment a layer stack typical for a source to produce double heterojunction-HEMT (DH-HEMT) devices was deposited on polished silicon single crystal wafers which were on-oriented or off-oriented in accordance with the invention. The sequence of layers is shown in Fig.3. Each layer was deposited at 1010°C.

The bow (B) of twenty one layered wafers (three different substrates in each runs) produced in consecutive growth runs (#1 to #7) resolved in x- and y-direction was determined after the deposition of the entire stack. Fig.4 shows the results of the measurement in relation to the orientation of the substrate, wherein "on" represents an on-oriented substrate, and "0.5 off" and "1° off" a substrate which was off-oriented

in accordance with the invention by an inclination angle $\theta = 0.5^\circ$ and $\theta = 1^\circ$, respectively. Left (open) and right (shaded) columns represent the bow values in x- and y-direction, respectively. As shown in Fig.4, the post-deposition bow values
5 monotonically increase in the favorable convex bow direction as the inclination angle θ increases.

Fig.5 shows the plot of the bow of a layered structure according to Fig.3 in relation to the inclination angle θ .

10 Displayed is the average bow (AB) which means the average of bow in x-direction and y-direction.

A maximum value of bow ($28\mu\text{m}$) of the layered wafer was observed for a substrate with 1° off-orientation. Then it decreases when the inclination angle θ is further increased from $\theta \geq 1.5^\circ$.

15 However, the impact of the off-orientation of the substrate on the post-deposition bow of the layered wafer also depends upon the growth condition of the AlN nucleation layer. The maximum value of the post-deposition bow displayed in Fig.5 can be shifted beyond an inclination angle θ of 1° if the AlN

20 nucleation layer deposition temperature is lower than 1010°C .

The bow of the substrate before deposition is generally within a range of $-5\mu\text{m}$ to $5\mu\text{m}$, and has negligible influence to the post-deposition wafer bow.

Claims

1. A semiconductor wafer comprising a silicon single crystal substrate having a top surface and a stack of layers covering
5 the top surface, the stack of layers comprising
an AlN nucleation layer which covers the top surface of the silicon single crystal substrate, wherein the top surface of the silicon single crystal substrate has a crystal lattice orientation which is off-oriented with respect to the {111}-
10 plane, the normal to the top surface being inclined with respect to the $\langle 111 \rangle$ -direction toward the $\langle 11\bar{2} \rangle$ -direction by an angle θ of not less than 0.3° and not more than 6° , the azimuthal tolerance of the inclination being $\pm 0.1^\circ$; and
an AlGaIn buffer layer which covers the AlN nucleation layer and
15 comprises one or more $\text{Al}_x\text{Ga}_{1-x}\text{In}$ layers, wherein $0 < x < 1$.

2. The semiconductor wafer according to claim 1, wherein the AlN nucleation layer has a thickness of not less than 20 nm and not more than 500 nm.

3. The semiconductor wafer according to claim 1 or claim 2, wherein the AlGaIn buffer layer comprises one or more AlN layers.

4. The semiconductor wafer according to claim 1 or claim 2, wherein the AlGaIn buffer layer comprises one or more GaIn layers.

5. The semiconductor wafer according to one of claims 1 to 4, wherein the stack of layers comprises one or more device forming layers covering the AlGaIn buffer layer and having a composition of a binary, ternary or quaternary Group III-nitride consisting of at least one of the elements Al, Ga and In .

6. The semiconductor wafer according to one of claims 1 to 5, wherein the silicon single crystal substrate is a silicon single crystal wafer having a diameter of 150 mm or more.

5 7. A method for producing a semiconductor wafer comprising a silicon single crystal substrate having a top surface and a stack of layers covering the top surface, the method comprising providing the silicon single crystal substrate having a top surface, the top surface of the silicon single crystal
10 substrate having a crystal lattice orientation which is off-oriented with respect to the {111}-plane, the normal to the top surface being inclined with respect to the <111>-direction toward the <11-2>-direction by an angle θ of not less than 0.3° and not more than 6° , the azimuthal tolerance of the
15 inclination being $\pm 0.1^\circ$;

depositing on the top surface of the silicon single crystal substrate an AlN nucleation layer which covers the top surface of the silicon single crystal substrate;
depositing an AlGa_xN buffer layer which covers the AlN
20 nucleation layer and comprises one or more Al_xGa_{1-x}N layers, wherein $0 < x < 1$.

8. The method according to claim 7, comprising depositing one or more device forming layers which cover the
25 AlGa_xN buffer layer and have a composition of a binary, ternary or quaternary Group III-nitride consisting of at least one of the elements Al, Ga and In.

9. The method according to claim 8, wherein the deposition
30 method comprises metal-organic chemical vapor deposition (MOCVD).