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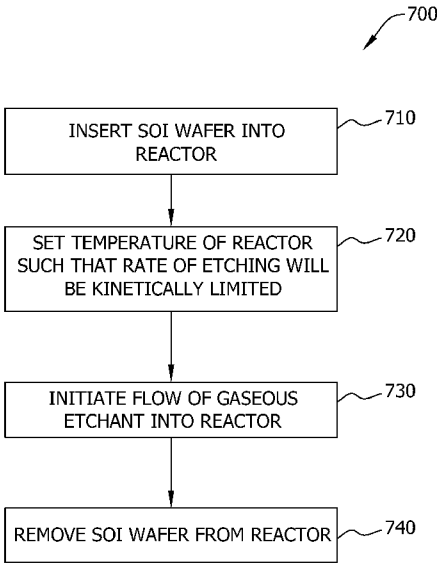
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(54) **Title**: METHODS FOR PROCESSING SILICON ON INSULATOR WAFERS

FIG. 7



(57) **Abstract**: Methods are provided for etching and/or depositing an epitaxial layer on a silicon-on-insulator structure comprising a handle wafer, a silicon layer, and a dielectric layer between the handle wafer and the silicon layer. The silicon layer has a cleaved surface defining an outer surface of the structure. The cleaved surface of wafer is then etched while controlling a temperature of the reactor such that the etching reaction is kinetically limited. An epitaxial layer is then deposited on the wafer while controlling the temperature of the reactor such that a rate of deposition on the cleaved surface is kinetically limited.

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