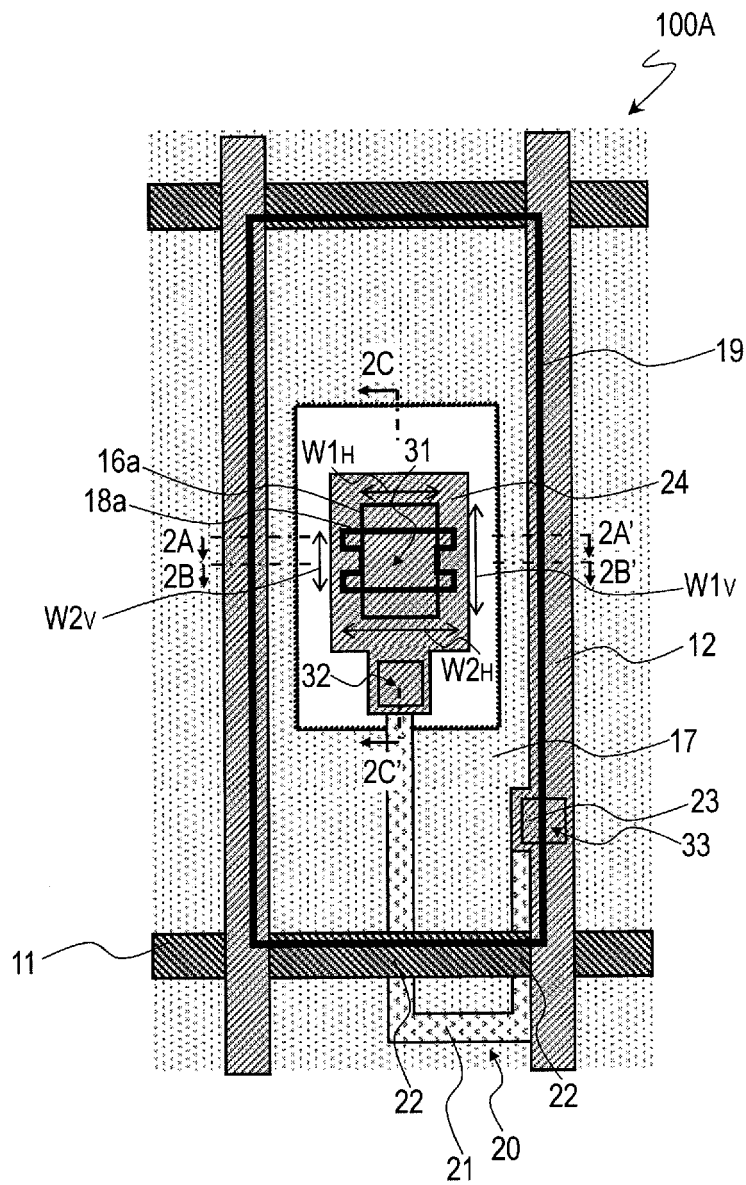


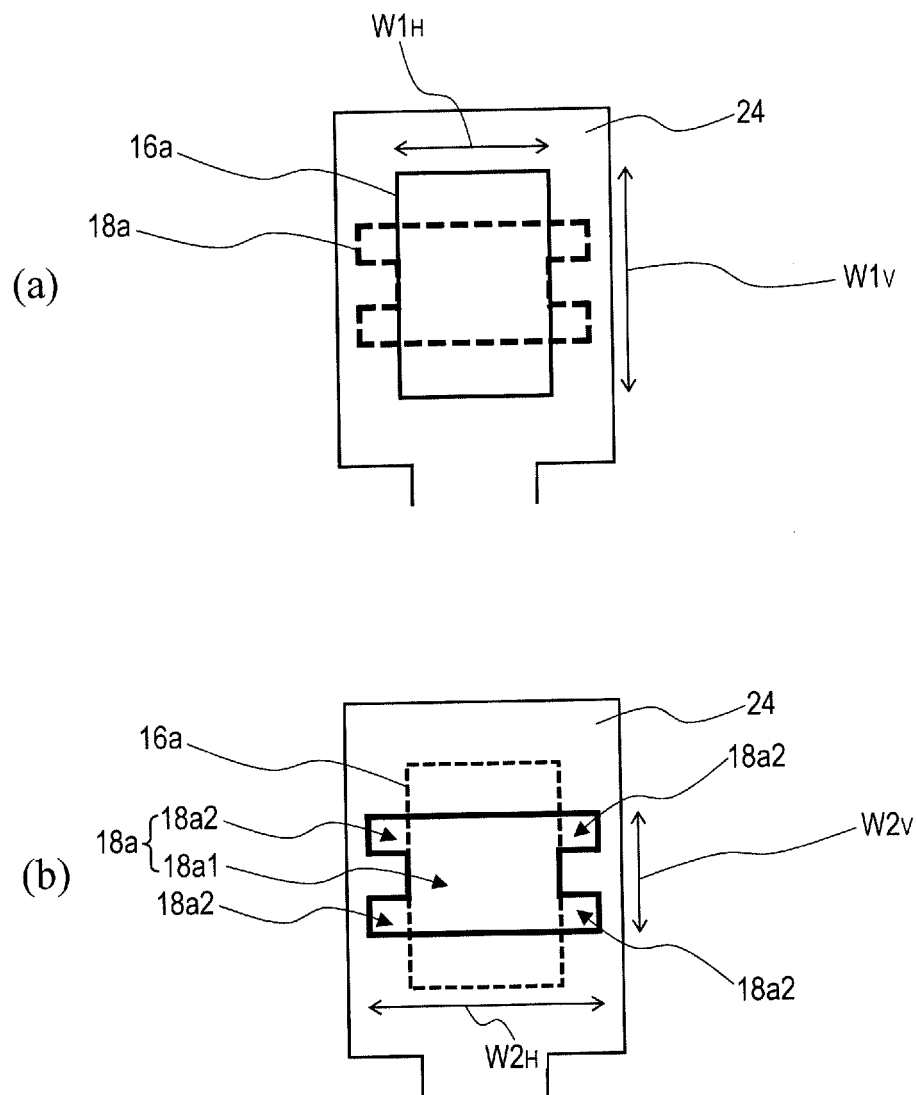
[図1]



The figure consists of three cross-sectional views labeled (a), (b), and (c), all showing a semiconductor device 100A.

- (a)** Shows a central gate stack 31 with a top layer 18 and a bottom layer 17. The gate stack is flanked by side walls 16a. Below the gate stack is a layer 16. The entire structure is supported by a substrate 10. A layer 12 is located below the gate stack, with regions S and SW indicated. A dimension W_{3H} 24 is shown across the width of the gate stack. Other layers include 13, 14, and 15.
- (b)** Shows a similar structure to (a), but with a different configuration of the gate stack 31 and the underlying layers 12, 13, 14, and 15. The label 24 is present near the base of the gate stack.
- (c)** Shows a more complex structure with additional features. It includes a layer 16, a gate stack 31, and various other layers like 12, 13, 14, 15, and 21. A specific feature 32 is highlighted on the right side of the gate stack.

[図3]



[図4]

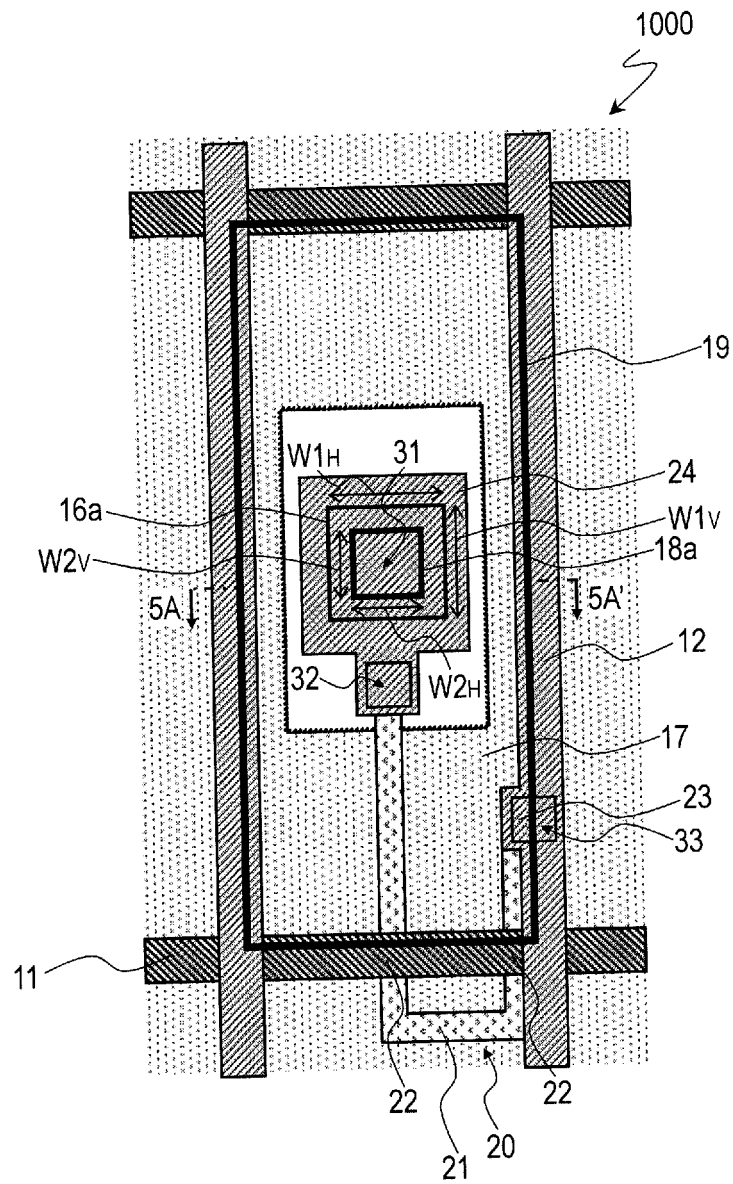
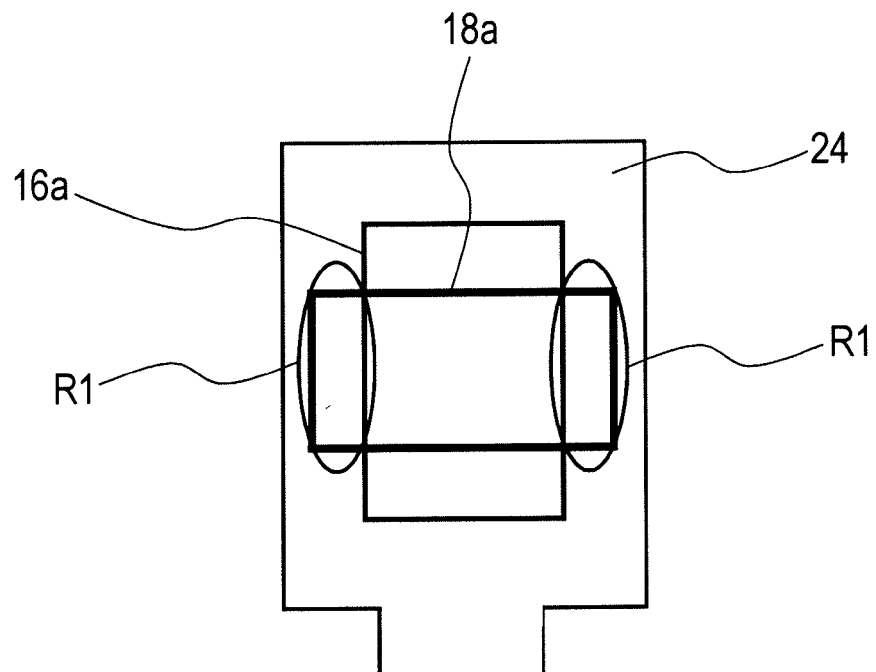
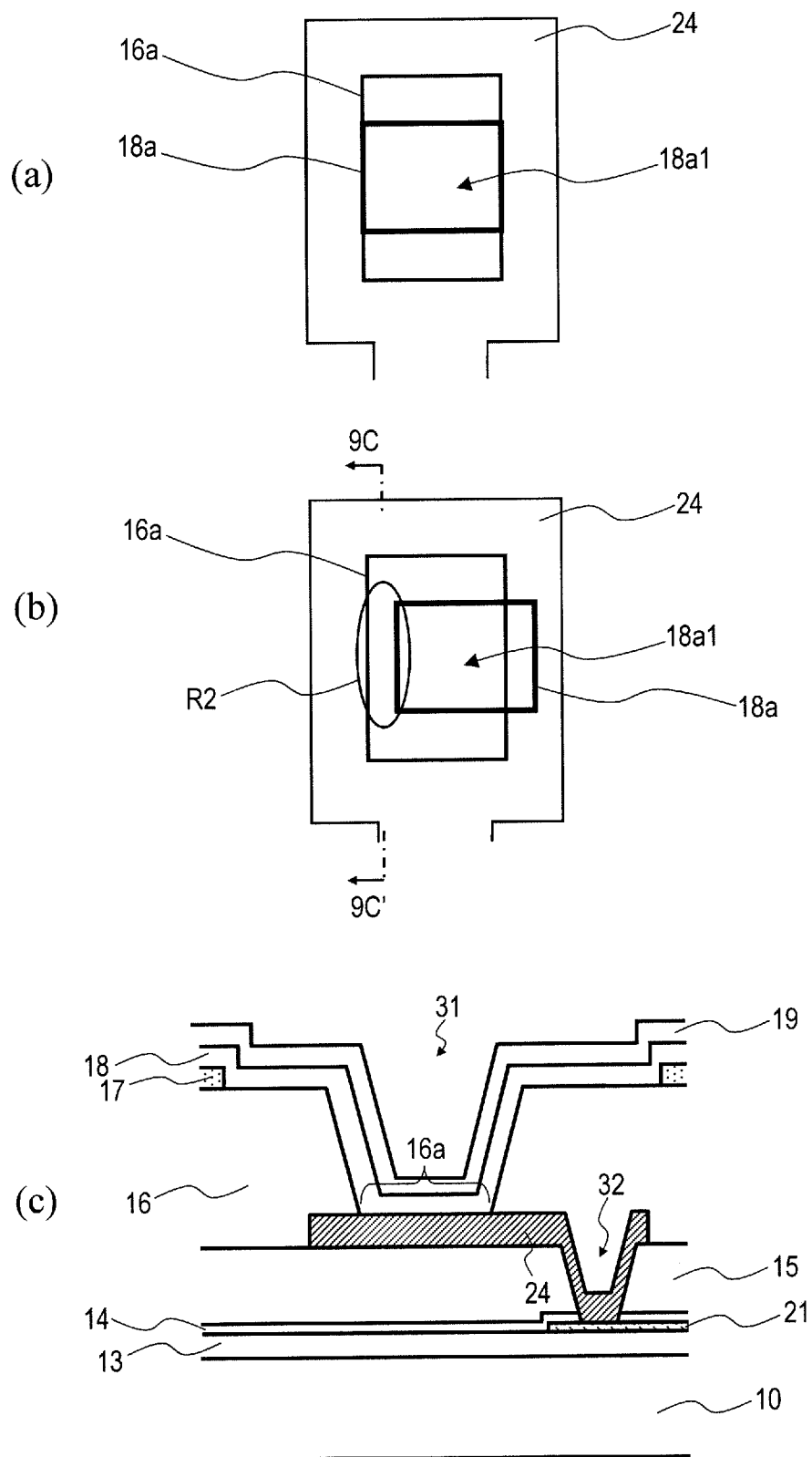


Figure 1 is a cross-sectional view of a semiconductor device 1000. The device features a central channel 31 with side walls 16a and 18a. The channel is formed in a base layer 12, which has a width W3H. The base layer 12 is surrounded by a gate stack 10 and a substrate 13. The gate stack 10 includes a gate dielectric layer 14 and a gate electrode layer 15. The substrate 13 is a silicon substrate. The device is surrounded by a gate stack 10 and a substrate 13. The gate stack 10 includes a gate dielectric layer 14 and a gate electrode layer 15. The substrate 13 is a silicon substrate. The device is surrounded by a gate stack 10 and a substrate 13. The gate stack 10 includes a gate dielectric layer 14 and a gate electrode layer 15. The substrate 13 is a silicon substrate.

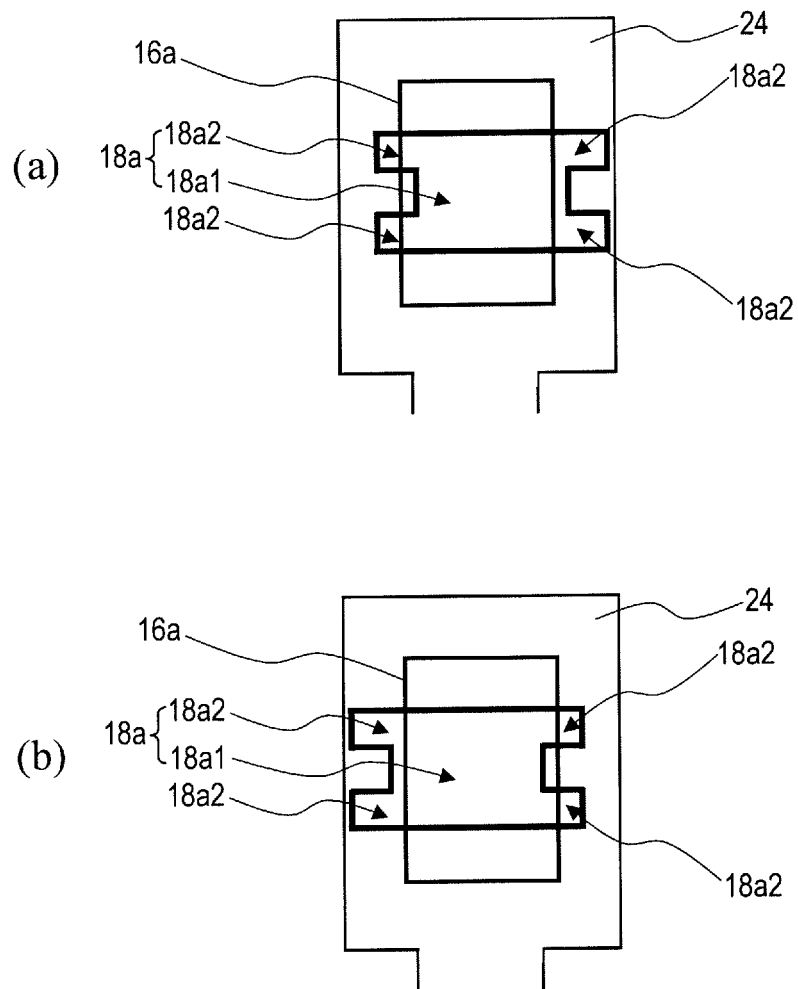
[図8]



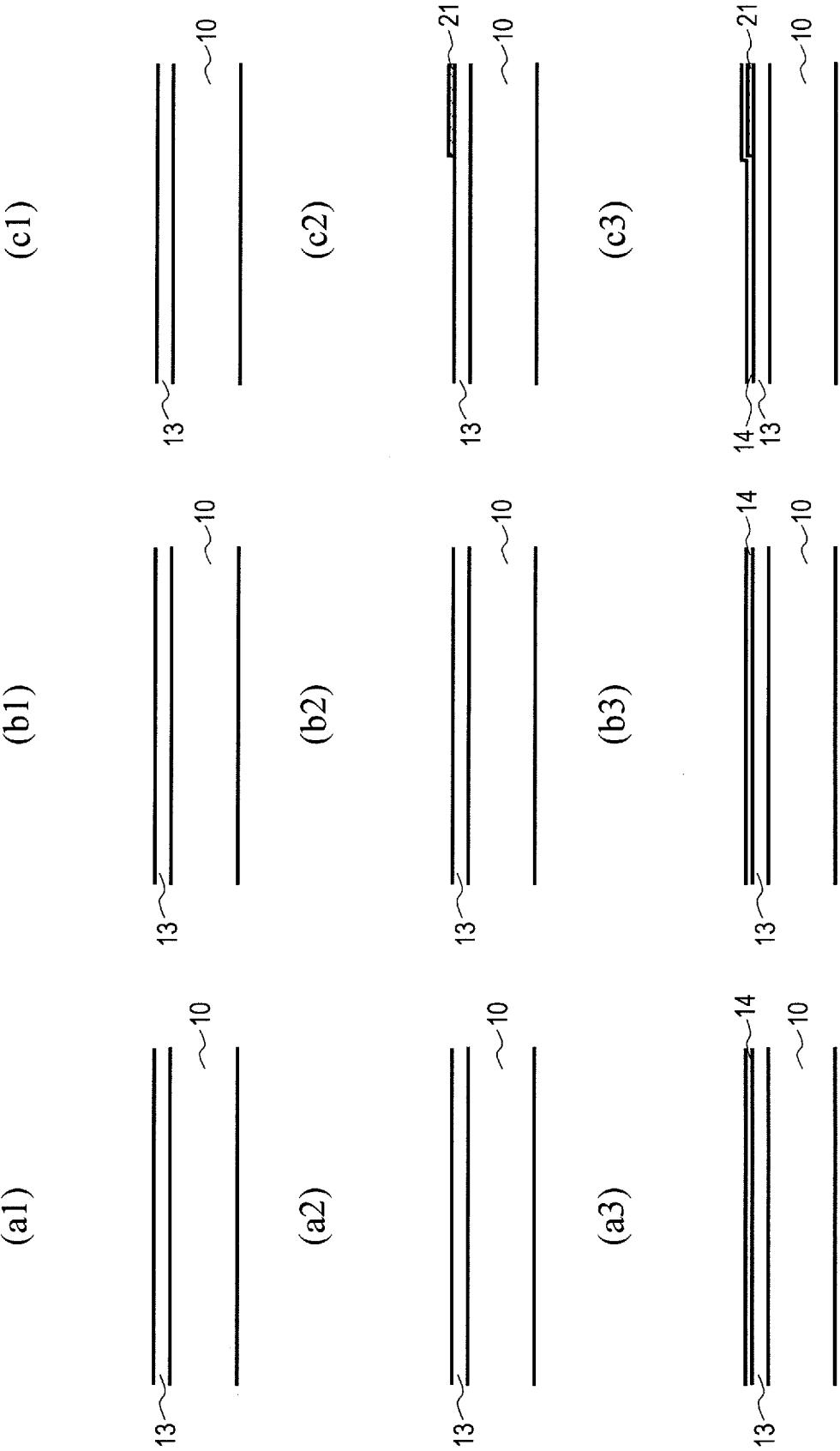
[図9]



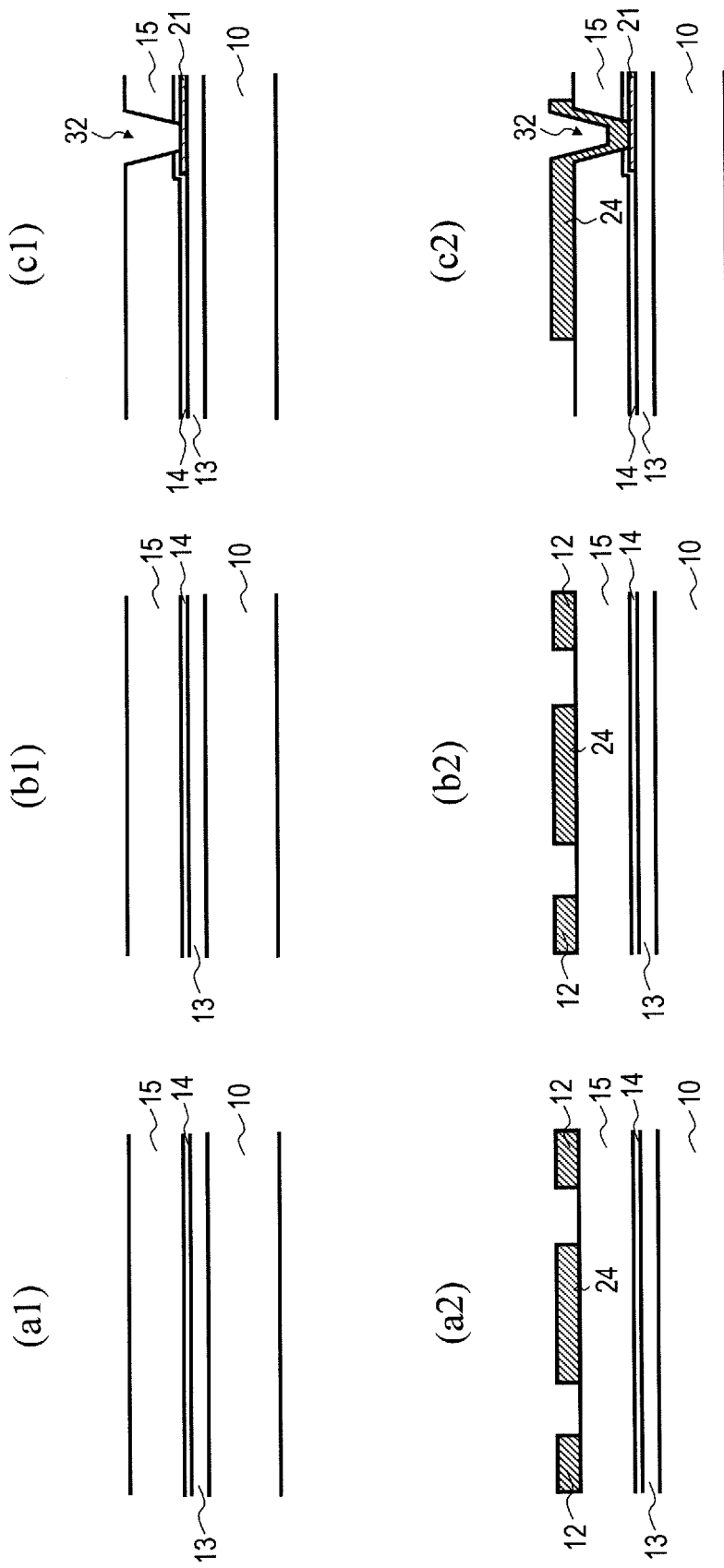
[図10]



[図11]

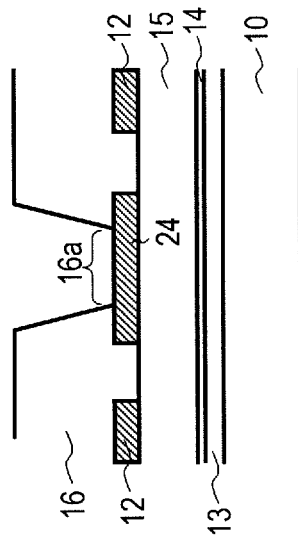


[図12]

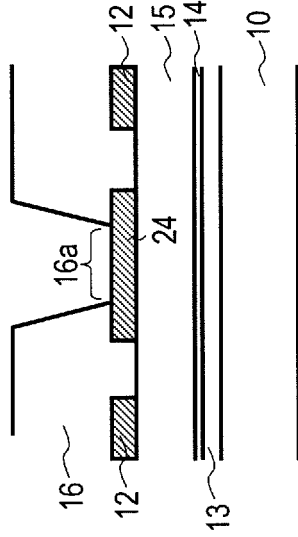


[図13]

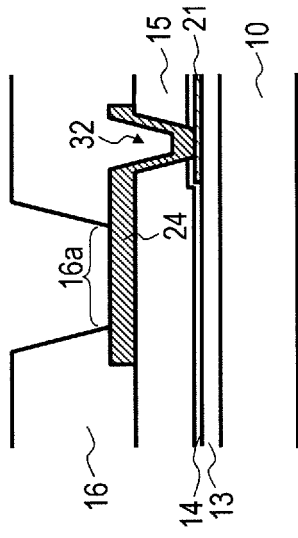
(a1)



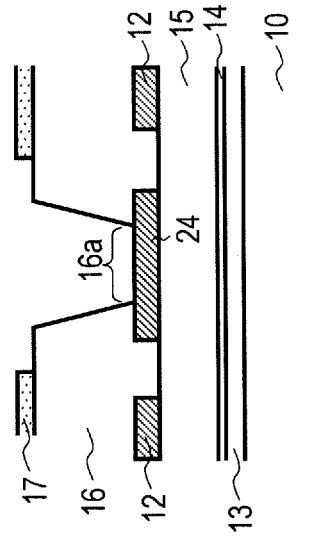
(b1)



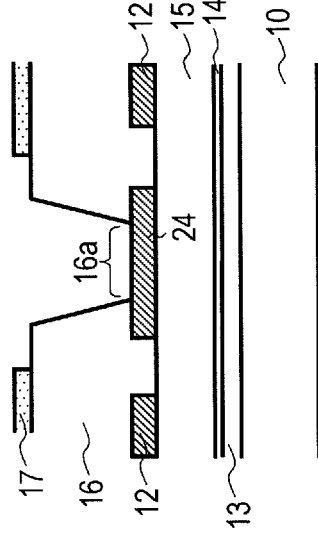
(c1)



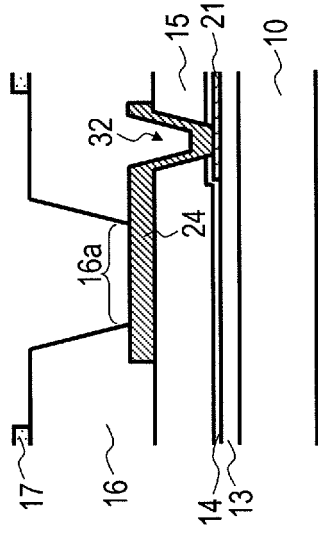
(a2)



(b2)

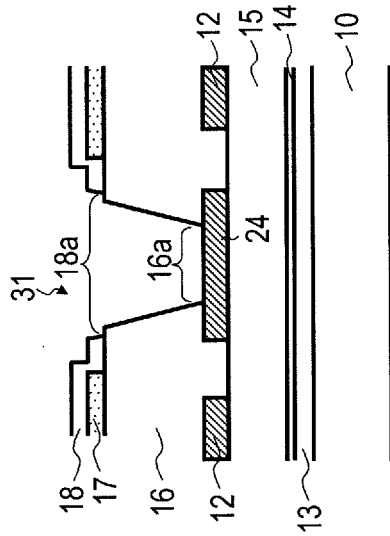


(c2)

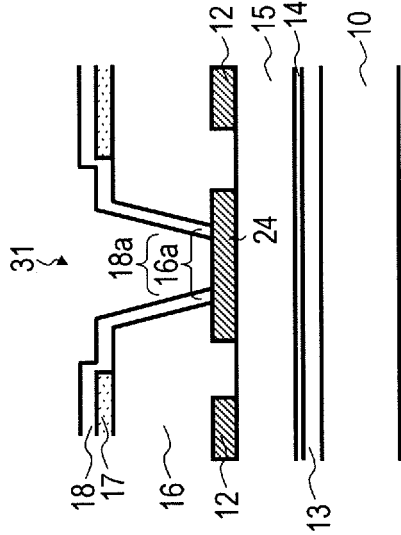


[図14]

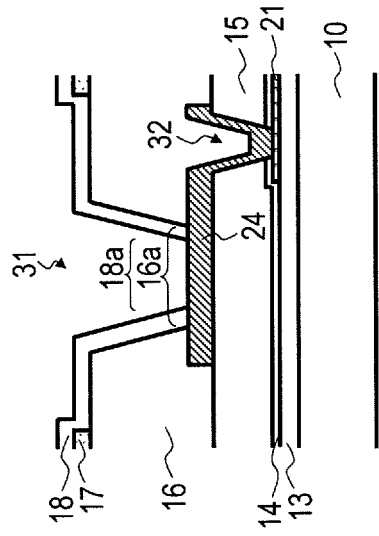
(a1)



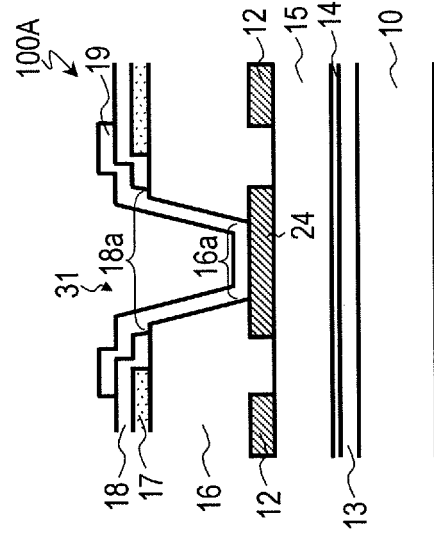
(b1)



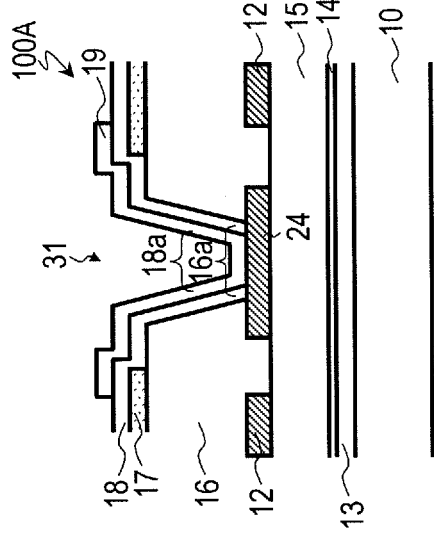
(c1)



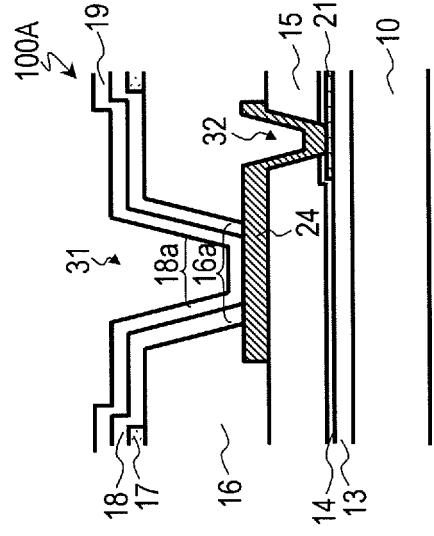
(a2)



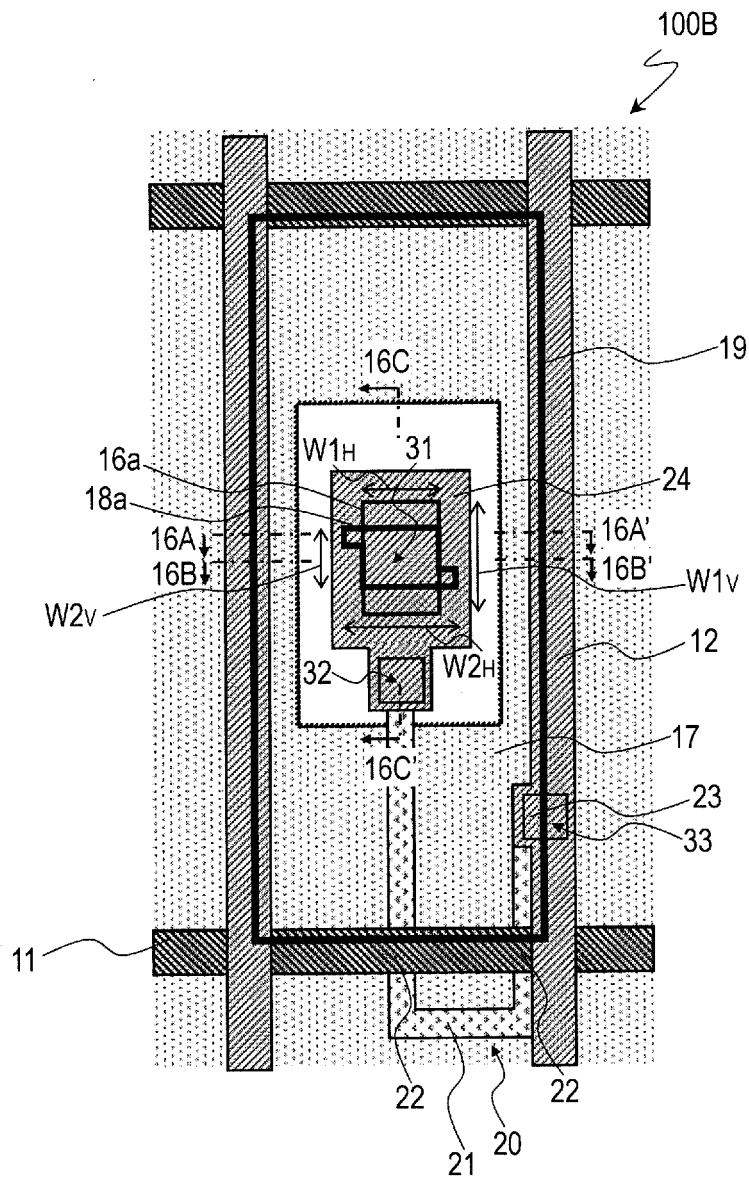
(b2)



(c2)

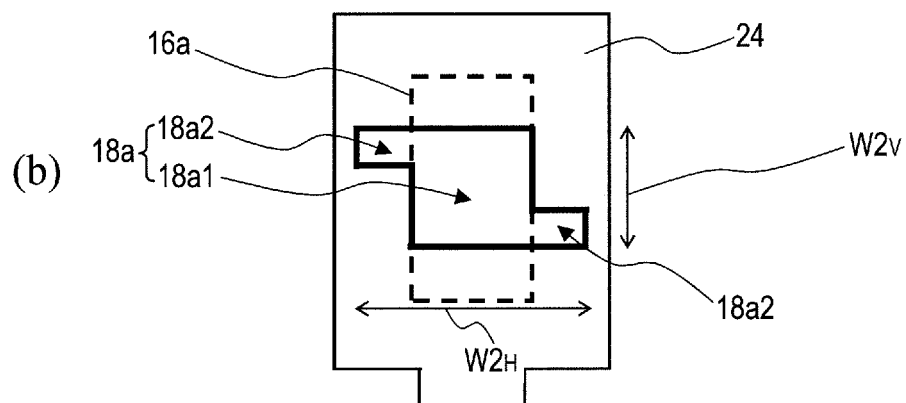
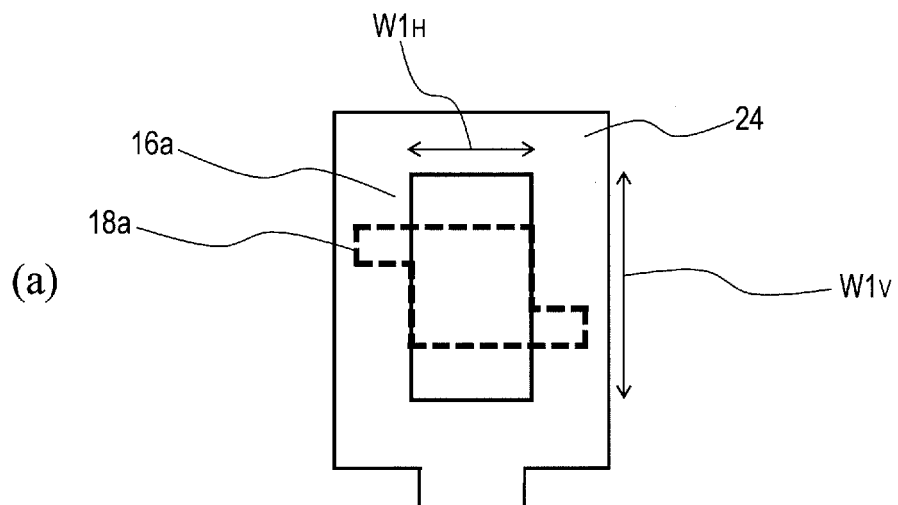


[図15]

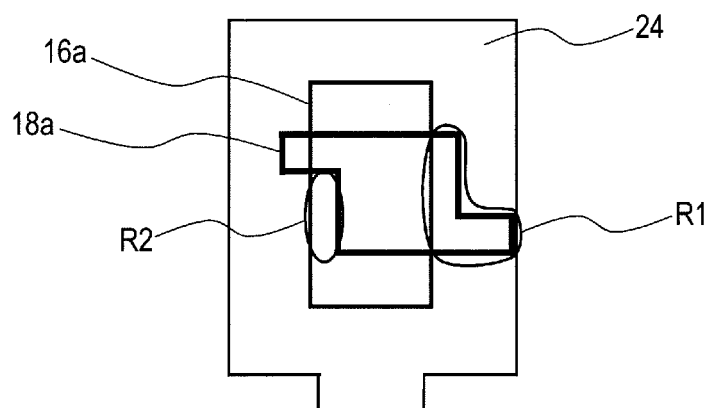


[illegible]

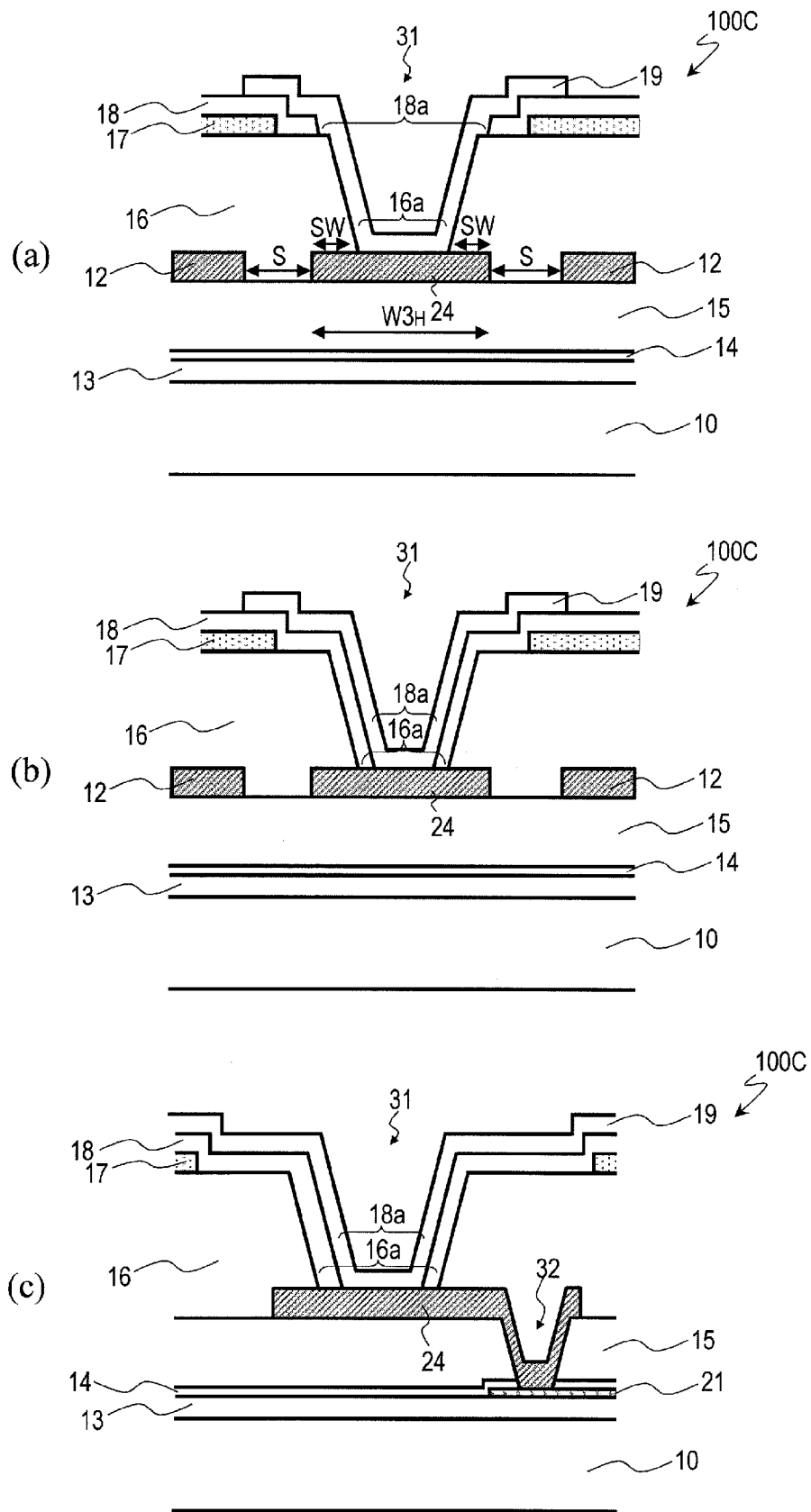
[図17]



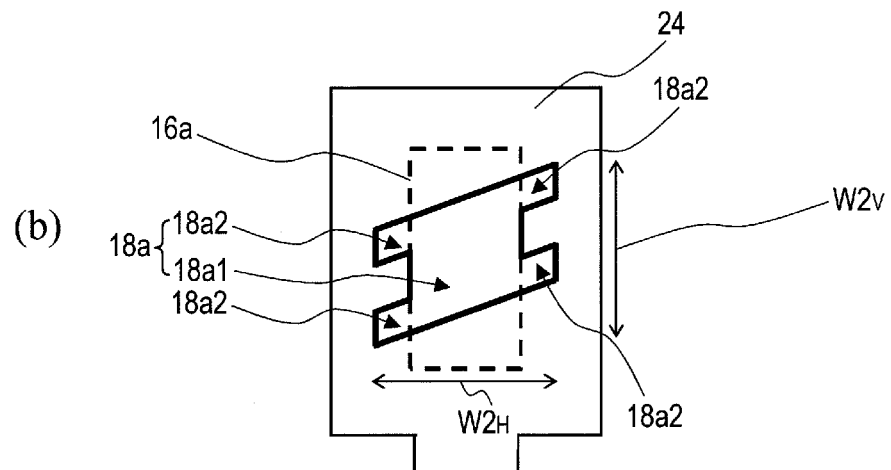
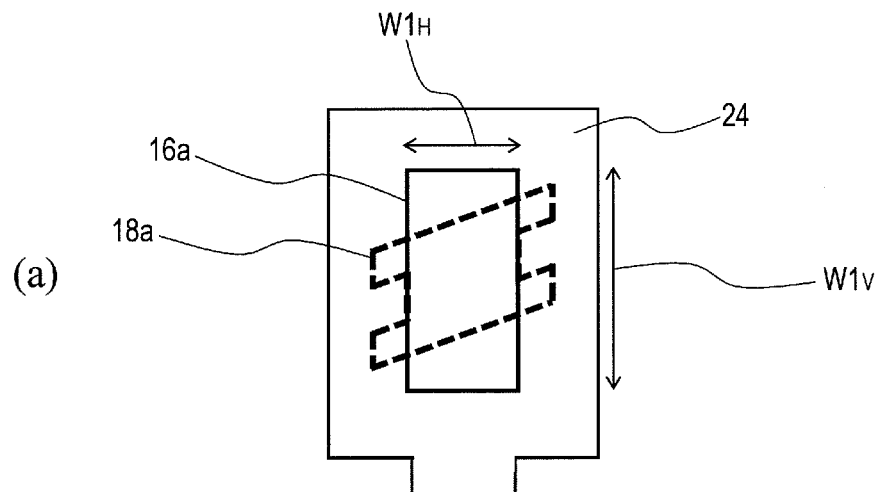
[図18]



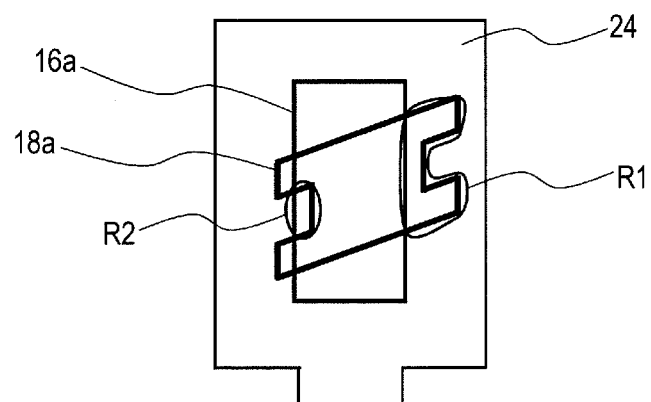
[図20]



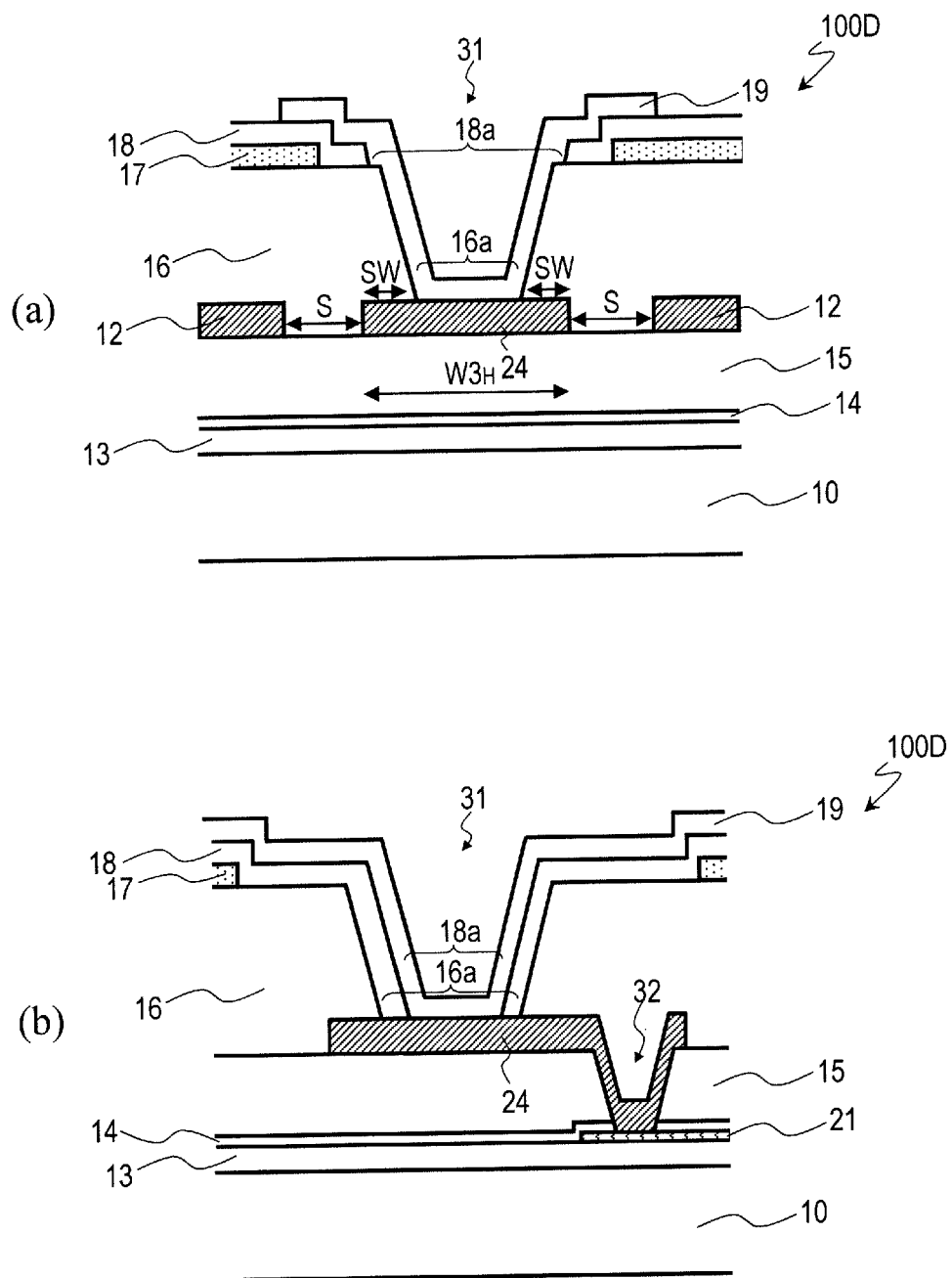
[図21]



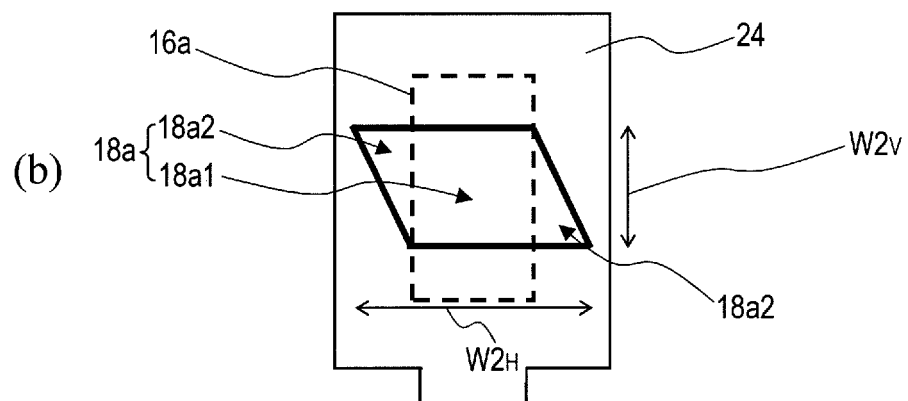
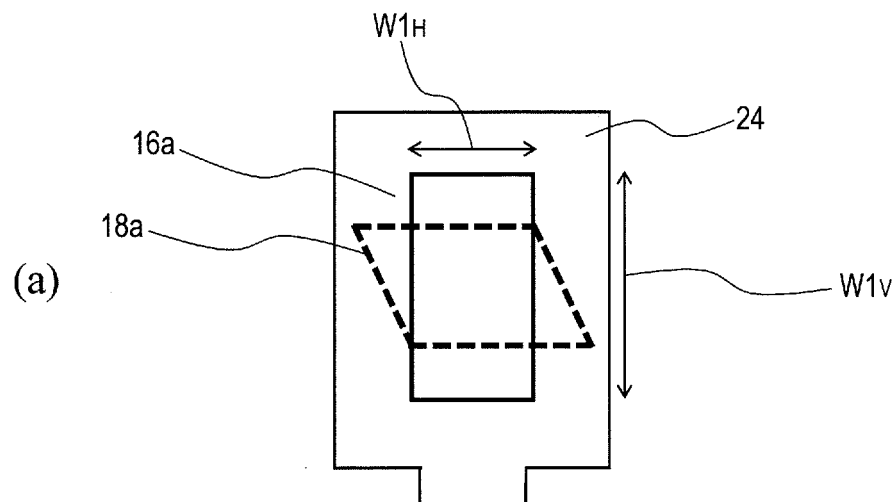
[図22]



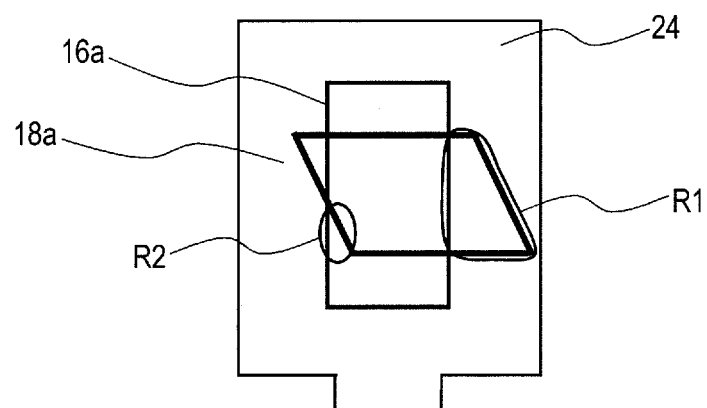
[図24]



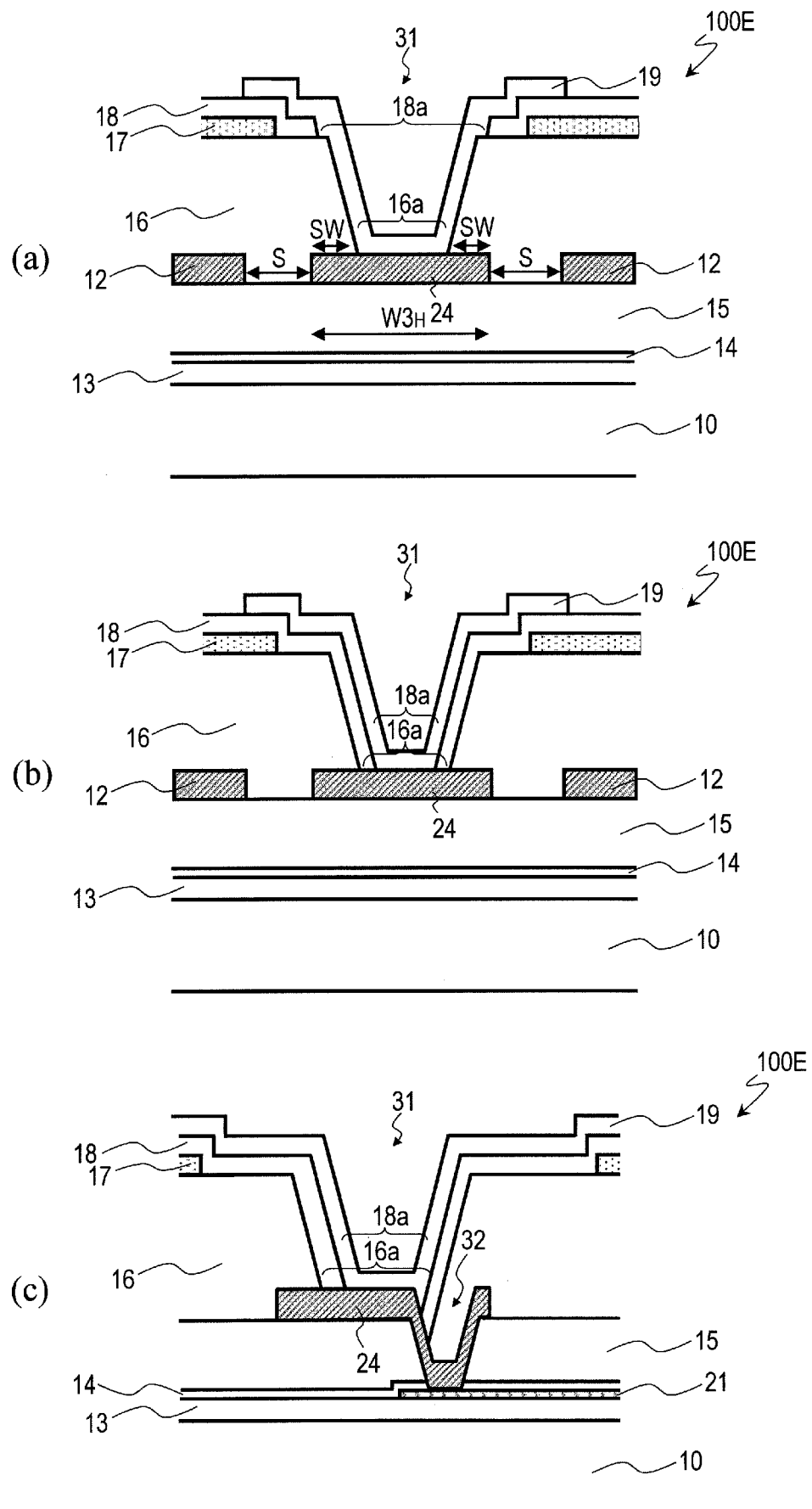
[図25]



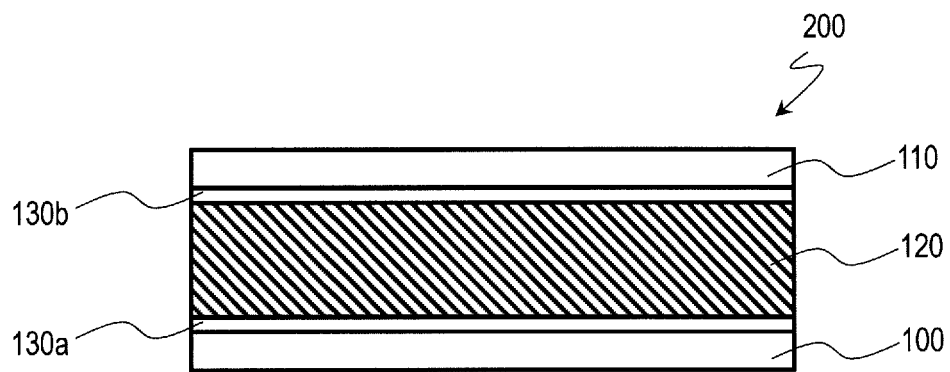
[図26]



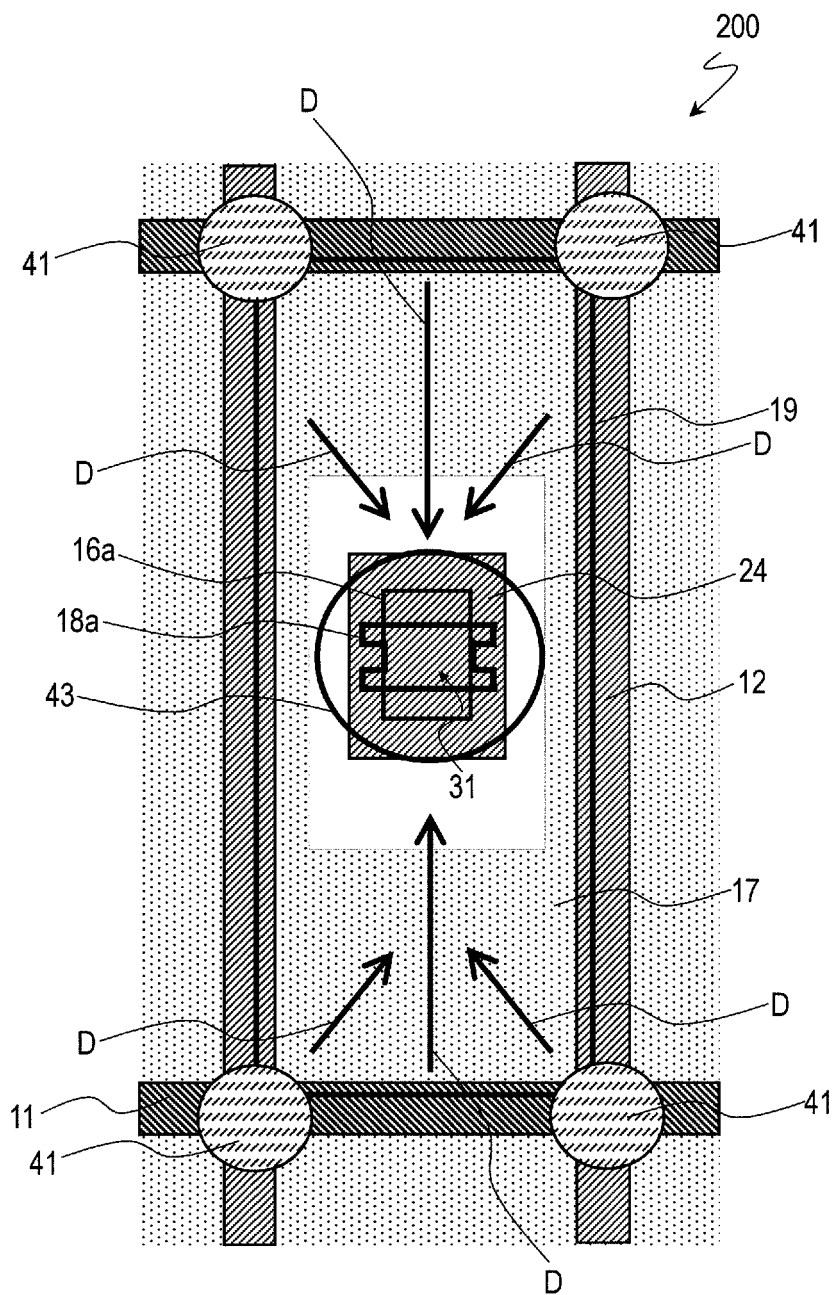
[図28]



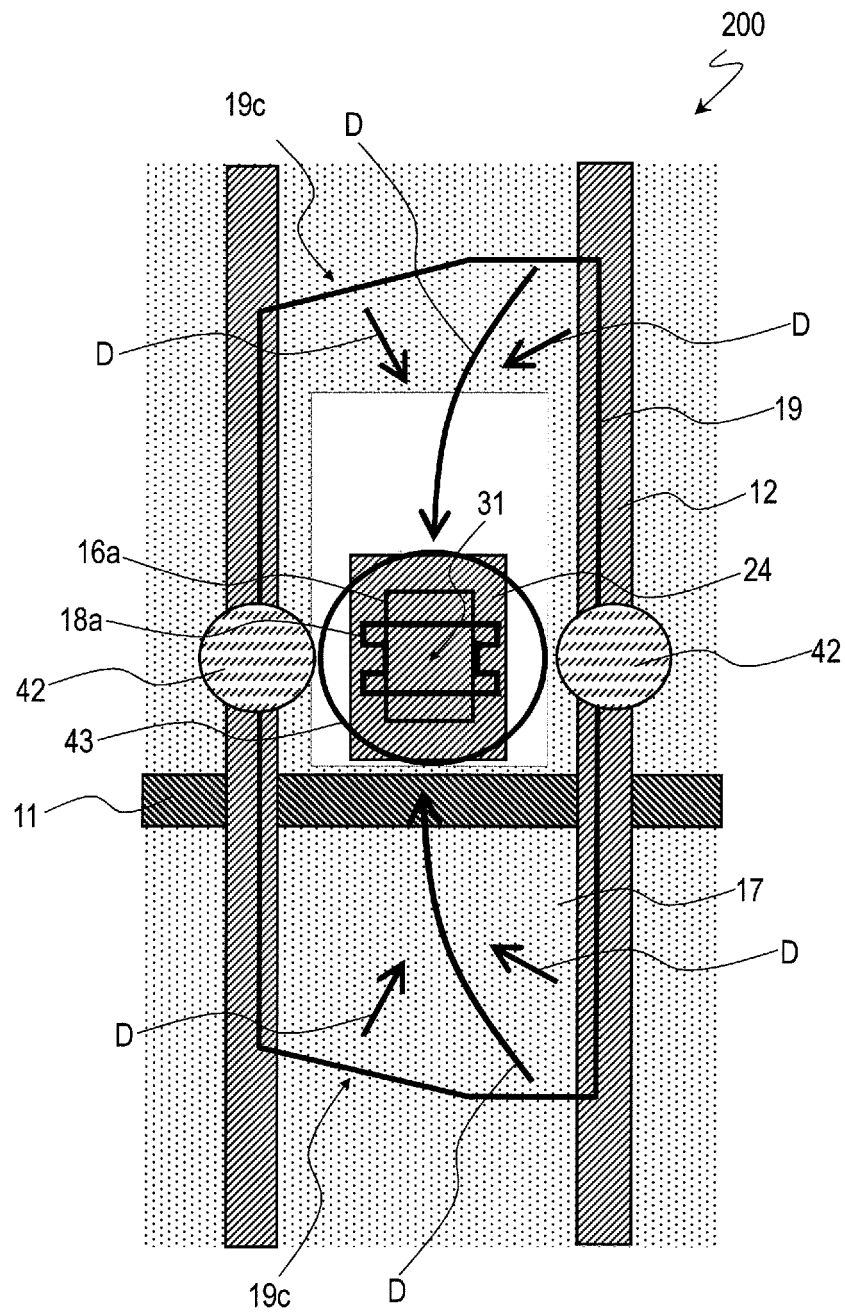
[図29]



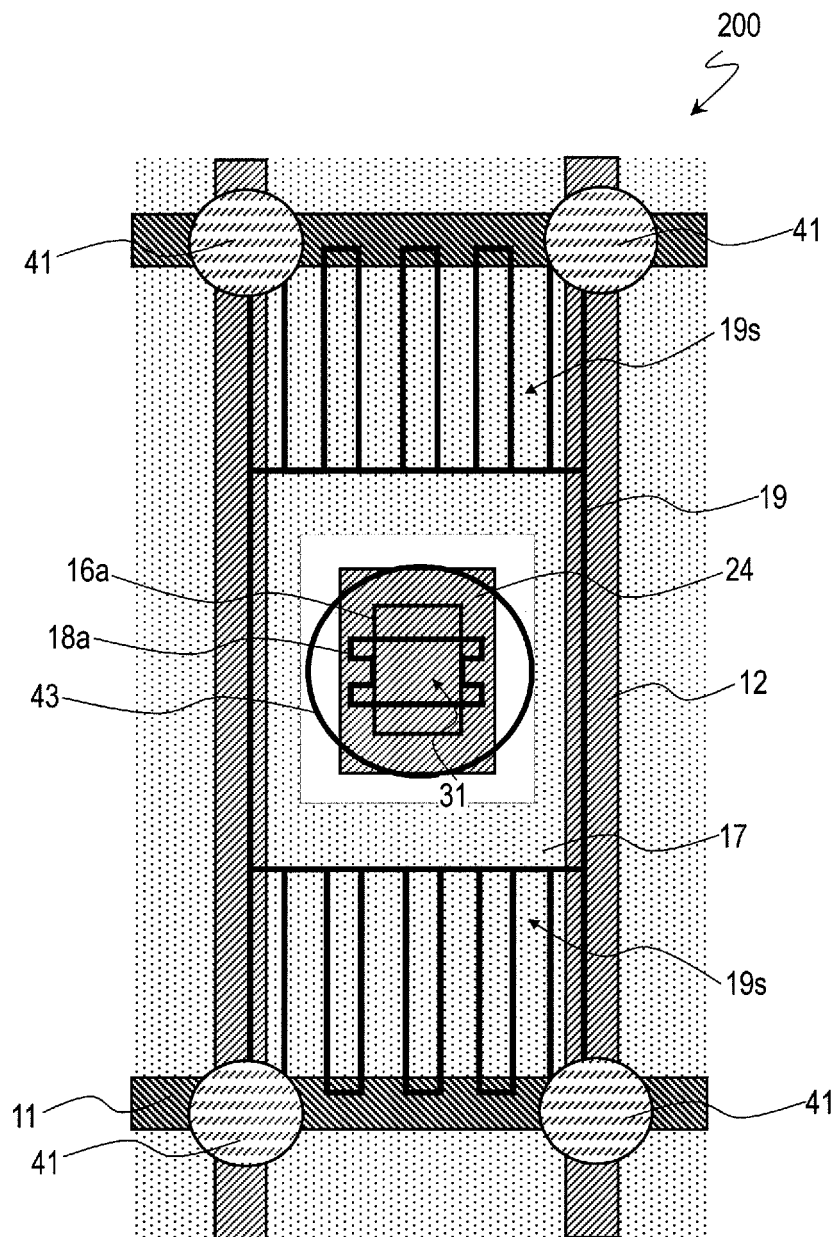
[図30]



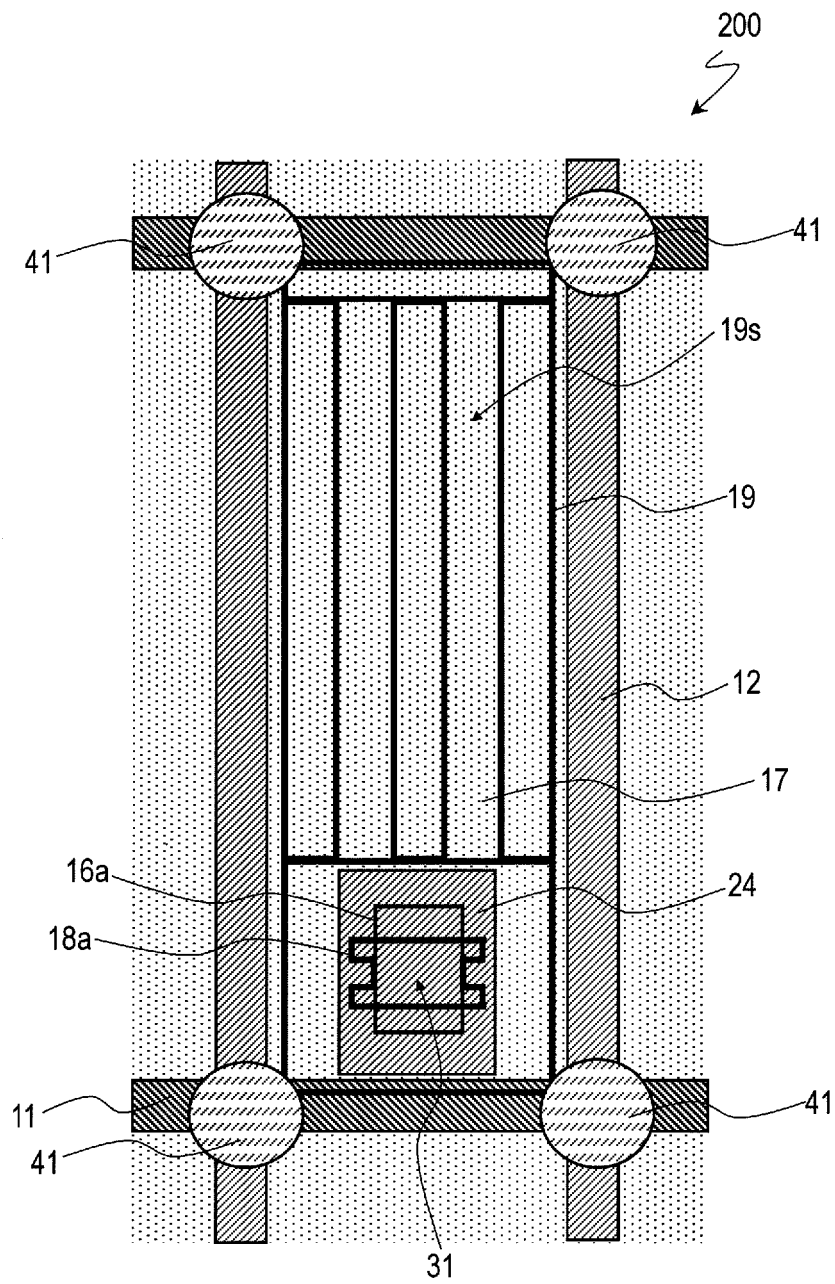
[図31]



[図33]



[図34]



[図35]

