SECONDARY DEVICE INTEGRATION INTO CORELESS MICROELECTRONIC DEVICE PACKAGES

BACKGROUND

Embodiments of the present description relate generally to the field of microelectronic device package designs and, more particularly, to microelectronic device packages having bumpless build-up layer (BBUL) designs.

BRIEF DESCRIPTION OF THE DRAWINGS

The subject matter of the present disclosure is particularly pointed out and distinctly claimed in the concluding portion of the specification. The foregoing and other features of the present disclosure will become more fully apparent from the following description and appended claims, taken in conjunction with the accompanying drawings. It is understood that the accompanying drawings depict only several embodiments in accordance with the present disclosure and are, therefore, not to be considered limiting of its scope. The disclosure will be described with additional specificity and detail through use of the accompanying drawings, such that the advantages of the present disclosure can be more readily ascertained, in which:

FIGs. 1-13 illustrate side cross-sectional views of a process of forming a bumpless build-up layer coreless (BBUL-C) microelectronic package with surface mounted device-side secondary devices, according to one embodiment of the present description.

FIGs. 14-25 illustrate side cross-sectional views of a process of forming a bumpless build-up layer coreless (BBUL-C) microelectronic package with embedded device-side secondary devices, according to another embodiment of the present description.

FIGs. 26-37 illustrate side cross-sectional views of a process of forming a bumpless build-up layer coreless (BBUL-C) microelectronic package with embedded device-side secondary devices, according to still another embodiment of the present description.

DETAILED DESCRIPTION

In the following detailed description, reference is made to the accompanying drawings that show, by way of illustration, specific embodiments in which the claimed subject matter may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the subject matter. It is to be understood that the various embodiments, although different, are not necessarily mutually exclusive. For

example, a particular feature, structure, or characteristic described herein, in connection with one embodiment, may be implemented within other embodiments without departing from the spirit and scope of the claimed subject matter. References within this specification to "one embodiment" or "an embodiment" mean that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one implementation encompassed within the present invention. Therefore, the use of the phrase "one embodiment" or "in an embodiment" does not necessarily refer to the same embodiment. In addition, it is to be understood that the location or arrangement of individual elements within each disclosed embodiment may be modified without departing from the spirit and scope of the claimed subject matter. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the subject matter is defined only by the appended claims, appropriately interpreted, along with the full range of equivalents to which the appended claims are entitled. In the drawings, like numerals refer to the same or similar elements or functionality throughout the several views, and that elements depicted therein are not necessarily to scale with one another, rather individual elements may be enlarged or reduced in order to more easily comprehend the elements in the context of the present description.

Embodiments of the present description relate to the field of fabricating microelectronic device packages and, more particularly, to microelectronic device packages having bumpless build-up layer (BBUL) designs, wherein at least one secondary device, such as a capacitor, a micro electro-mechanical device (such as an accelerometer, radio frequency switches, and the like), a GPS device, a passive device, and the like, is disposed within the thickness (i.e. the z-direction or z-height) of the microelectronic device of the microelectronic device package. In some embodiments of the present description, openings or cavity structures may be created using relatively thick dielectric materials, such as photo definable photoresist materials, wherein microelectronic devices and components may be mounted therein. Such a use of relatively thick dielectric material cavities may enable packaging architectures that can allow surface mounting or embedding a variety of device side secondary devices without sacrificing z-height (i.e. thickness) constraints. In addition, embodiments of the present description may allow for microelectronic device back surfaces being above the device side secondary devices, such that heat sinks may directly contact the microelectronic device back surfaces, or such that additional devices (e.g. memory, logic, etc) may be attached with through silicon vias to the microelectronic device back surfaces.

FIGs. 1-13 illustrate cross-sectional views of an embodiment of a process of forming a bumpless build-up layer coreless (BBUL-C) microelectronic package with surface mounted device-side secondary devices. As shown in FIG. 1, a carrier 100 may be provided. The carrier 100 illustrated may be a copper laminated substrate comprising an adhesion material 106 disposed between two opposing copper release layers (i.e. a first copper release layer 104 and a second copper release layer 104') with a two opposing copper layers (i.e. a first copper layer 102 and a second copper layer 102') abutting their respective copper release layers (i.e. the first copper release layer 104 and the second copper release layer 104') and abutting a portion of the adhesion material 106, wherein the exterior surface of the first copper layer 102 defines a first surface 108 of the carrier 100 and the exterior surface of the second copper layer 102' defines a second surface 108' of the carrier 100. The adhesion material 106 may be any appropriate material, including but not limited to an epoxy material. It is understood that although the layers laminated with the adhesion material 106 are specifically identified as copper layers (i.e. the copper layers and the copper release layers), the present description is not so limited, as the layers may be made of any appropriate material.

As shown in FIG. 2, a first sacrificial material layer 110, such as a photoresist material, may be formed on the carrier first surface 108 and a second sacrificial material layer 110', such as a photoresist material, may be formed on the carrier second surface 108'. A first protective layer 120, such as a metal foil (for example, copper foil), may be formed on the first sacrificial material layer 110, and a second protective layer 120', such as a metal foil (for example, copper foil), may be formed on the second sacrificial material layer 110', as shown in FIG. 3. The first sacrificial material layer 110 and the second sacrificial material layer 110' may be formed by any technique known in the art, including but not limited to spin coating, dry photofilm lamination, and chemical vapor deposition. The first protective layer 120 and the second protective layer 120' may be formed by any technique known in the art, including but not limited to deposition and foil lamination. In one embodiment, the first and second sacrificial material layer 110 and the second sacrificial material layer 110' may be deposited to thickness of between about 300μm and 600μm.

As shown in FIG. 4, secondary device pads may be formed on the protective layers. As illustrated, a first secondary device pad 124a and a second secondary device pad 124b may be formed on the first protective layer 120, and a third secondary device pad 124a' and a fourth secondary device pad 124b' may be formed on the second

protective layer 120'. Metallization layers (i.e. elements 122a, 122b, 122a', and 122b' may be disposed between their respective protective layers (i.e. elements 120 and 120') and their respective secondary device pads (e.g. elements 124a, 124b, 124a', and 124b'). The metallization layers (i.e. elements 122a, 122b, 122a', and 122b') will be subsequently discussed in further detail. As also shown in FIG. 4, package-on-package (PoP) pads may also be formed on the protective layers (e.g. elements 120 and 120') simultaneously with the formation of the secondary device pads (e.g. elements 124a, 124b, 124a', and 124b'), as will be understood to those skilled in the art. FIG. 4 illustrates a first package-on-package pad 128a and a second package-on-package pad 128b may also be formed on the first protective layer 120, and a third package-on-package pad 128a' and a fourth package-on-package pad 128b' may be formed on the second protective layer 120'. Metallization layers (i.e. elements 126a, 126b, 126a', and 126b' may also be disposed between their respective protective layers (e.g. elements 120 and 120') and their respective package-on-package pad (e.g. elements 128a, 128b, 128a', and 128b'). As will be understood those skilled in the art, the package-on-package pads may be used to form connections between microelectronic device packages in the z-direction for stacking (e.g. referred to as 3D stacking), without the need for through silicon vias. The secondary device pads and the package-on-package pads may be formed by any technique known in the art, including deposition, photolithography, and etching.

As shown in FIG. 5, an opening 132 may be formed through the first protective layer 120 to expose a portion of the first sacrificial material layer 110, and an opening 132' may be formed simultaneously in second protective layer 120' to expose a portion of the second sacrificial material layer 110'. The first protective layer opening 132 and the second protective layer opening 132' may be formed by any technique known in the art, including but not limited to photolithographic patterning and etching. It is understood that the first sacrificial material layer 110 and the second sacrificial material layer 110' may act as an etch stop during the formation of the first protective layer opening 132 and the second protective layer opening 132'.

As shown in FIG. 6, an opening 134 may be formed, using the first protective layer 120 as a mask, through the first sacrificial material layer 110 to expose a portion of the carrier first surface 108. An opening 134' may be formed simultaneously, using the second protective layer as a mask, through the second sacrificial material layer 110' to expose a portion of the carrier second surface 108'. The first sacrificial material layer opening 134 and the second sacrificial material layer opening 134' may be formed by any

technique known in the art, including but not limited to photolithographic processes and wet or dry etching, wherein the first copper layer 102 and the second copper layer 102' may act as etch stops.

As shown in FIG. 7, a first microelectronic device 142 may be attached by a back surface 150 thereof with an adhesive material 144 to the carrier first surface 108 within the first sacrificial material layer opening 134. The first microelectronic device 142 may have at least one contact land (shown as elements 146a and 146b) on an active surface 148 thereof. A second microelectronic device 142' may be attached by a back surface 150' with an adhesive material 144' to the carrier second surface 108' within the second sacrificial material layer opening 134'. The second microelectronic device 142' may have at least one contact land (shown as elements 146a' and 146b') on an active surface 148' thereof. The first microelectronic device 142 and the second microelectronic device 142' may be any desired device, including but not limited to a microprocessor (single or multi-core), a memory device, a chipset, a graphics device, an application specific integrated circuit, or the like. The adhesive material 144 and 144' may be any appropriate material, including but not limited to a die backside film.

As shown in FIG. 8, a first dielectric layer 152 may be formed on the first microelectronic device 142, the first protective layer 120, the first package-on-package pads 128a, the second package-on-package 128b, the first secondary device pad 124a, and the second secondary device pad 124b. A second dielectric layer 152' may be simultaneously formed on the second microelectronic device 142', the second protective layer 120', the third package-on-package pad 128a', the fourth package-on-package pad 128b', the third secondary device pad 124a', and the fourth secondary device pad 124b'. As also shown in FIG. 8, a plurality of openings 154 may be formed in the first dielectric layer 152 to expose at least a portion of each opening's 154 respective the first microelectronic device contact lands 146a and 146b, the first package-on-package pads 128a, the second package-on-package pads 128b, the first secondary device pads 124a, and the second secondary device pads 124b. A plurality of openings 154' may also be simultaneously formed in the second dielectric layer 152' to expose at least a portion of each opening's 154' respective the second microelectronic device contact lands 146a' and 146b', the third package-on-package pads 128a', the fourth package-on-package pads 128b', the third secondary device pads 124a', and the fourth secondary device pads 124b'. In one embodiment, the first dielectric layer 152 and the second dielectric layer 152' may comprise silica-filled epoxy, such as build-up films available from Ajinomoto Fine-

Techno Co., Inc., 1-2 Suzuki-cho, Kawasaki-ku, Kawasaki-shi, 210-0801, Japan (e.g. Ajinomoto ABF-GX13, Ajinomoto GX92, and the like). The openings 154 and 154' may be formed by any technique known in the art including but not limited to laser or ion drilling, etching, and the like.

As shown in FIG. 9, a conductive material, such as copper, aluminum, silver, gold, and alloys thereof, may be disposed within the openings 154, by any technique known in the art, to form a first microelectronic device contact land first conductive via 166a, a first microelectronic device contact land second conductive via 166b, a first package-on-package pad conductive via 162a, a second package-on-package pad conductive via 162b, a first secondary device pad conductive via 164a, and a second secondary device pad conductive via 164b. The conductive material may also be simultaneously disposed within the openings 154' to form a second microelectronic device contact land first conductive via 166a', a second microelectronic device contact land second conductive via 166b', a third package-on-package pad conductive via 162a', a fourth package-on-package pad conductive via 162b', a third secondary device pad conductive via 164a', and a fourth secondary device pad conductive via 164b'. As further shown in FIG. 9, conductive traces may be formed to electrically connect various conductive vias. As illustrated, a first conductive trace 168a may be formed to electrically connect the first secondary device pad conductive via 164a and the first microelectronic device contact land first conductive via 166a and a second conductive trace 168b may be formed to electrically connect the second secondary device pad conductive via 164b and the first microelectronic device contact land second conductive via 166b. Further, a third conductive trace 168a' may be formed to electrically connect the third secondary device pad conductive via 164a' and the second microelectronic device contact land first conductive via 166a' and a fourth conductive trace 168b' may be formed to electrically connect the fourth secondary device pad conductive via 164b' and the second microelectronic device contact land second conductive via 166b'. Thus, the connection of the various conductive vias and conductive traces form electrically conductive paths between the secondary devices pads and the microelectronic device. The conductive traces (e.g. elements 168a, 168b, 168a', and 168b') may be any appropriate conductive material, including but not limited to copper, aluminum, silver, gold, and alloys thereof.

It is understood that the additional dielectric layer, conductive vias, and conductive traces may be built up to form a desired number of layers. Once a desired number of layers are formed, exterior layers, such as a glass cloth layers, may be formed. As shown

in FIG. 9, a first exterior layer 172 may be formed on the first dielectric layer 152 and a second exterior layer 172' may be formed on the second dielectric layer 152'. The exterior layers (i.e. first exterior layer 172 and second exterior layer 172') may be used to engineer inherent warpages/stresses in microelectronic packages, as will be understood to those skilled in the art.

The structures thus formed on the carrier first surface 108 and on the carrier second surface 108' may be separated from one another with a depaneling process, as known in the art. FIG. 10 illustrates the structure formed on the carrier first surface 108 after depaneling. As shown in the FIG. 11, the first sacrificial material layer 110 may be removed, such as by plasma ashing or solvent release, as will be understood to those skilled in the art. The protective layer 120 may also be removed by any appropriate technique known in the art, as also shown in FIG. 11. The adhesive layer 144 may be removed from the first microelectronic device 142, such as by plasma ashing or a dissolution chemical, as shown in FIG. 12, to form a microelectronic device package 180. It is understood that if plasma ashing is used to remove the first sacrificial material layer 110, the adhesive layer 144 may also be removed in a single plasma ashing step.

At least one secondary device may then be attached to a secondary device pad. As shown in FIG. 13, a first secondary device 174a may be attached to the first secondary device pad 124a with the metallization layer 122a, and a second secondary device 174b may be attached to the second secondary device pad 124b with the metallization layer 122b. As can be seen in FIG. 13, the process of FIGs. 1-13 may result in a secondary device (e.g. elements 174a and 174b) which is disposed within a thickness T of the first microelectronic device 142 (i.e. between the first microelectronic device active surface 148 and the first microelectronic device back surface 150).

FIGs. 14-25 illustrate cross-sectional views of another embodiment of a process of forming a bumpless build-up layer coreless (BBUL-C) microelectronic package with embedded device side secondary devices. As shown in FIG. 14, a carrier, such as the carrier 100 of FIG. 1, may be provided, and at least one stand-off may be formed on the carrier. As illustrated, a first stand-off 202a and a second stand-off 202b may be formed on the carrier first surface 108, and a third stand-off 202a', and a fourth stand-off 202b' may be formed on the carrier second surface 108'. The stand-offs (e.g. elements 202a, 202b, 202a', and 202b') may be formed of any appropriate material, including but not limited to copper.

As shown in FIG. 15, a first sacrificial material layer 210, such as a photoresist material, may be formed on the carrier first surface 108 and over the first stand-off 202a and second stand-off 202b, and a second sacrificial material layer 210', such as a photoresist material, may be formed on the carrier second surface 108' and over the third stand-off 202a' and the fourth stand-off 202b'. A first protective layer 220 may be formed on the first sacrificial material layer 210, and a second protective layer 220', such as a metal foil may be formed on the second sacrificial material layer 210', as shown in FIG. 16. The first sacrificial material layer 210 and the second sacrificial material layer 210' may be formed by any technique known in the art, including but not limited to spin coating, dry photofilm lamination, and chemical vapor deposition. The first protective layer 220 and the second protective layer 220' may be formed by any technique known in the art, including but not limited to deposition and foil lamination. In one embodiment, the first sacrificial material layer 210 and the second sacrificial material layer 210' may be deposited to thickness of between about 300μm and 600μm.

As shown in FIG. 17, an opening 232 may be formed through the first protective layer 220 to expose a portion of the first sacrificial material layer 210, and an opening 232' may be formed simultaneously in second protective layer 220' to expose a portion of the second sacrificial material layer 210'. The first protective layer opening 232 and the second protective layer opening 232' may be formed by any technique known in the art, including but not limited to photolithographic patterning and etching. It is understood that the first sacrificial material layer 210 and the second sacrificial material layer 210' may act as an etch stop during the formation of the first protective layer opening 232 and the second protective layer opening 232'.

As shown in FIG. 18, an opening 234 may be formed, using the first protective layer 220 as a mask, through the first sacrificial material layer 210 to expose the first stand-off 202a, the second stand-off 202b, and a portion of the carrier first surface 108. An opening 234' may be formed simultaneously, using the second protective layer as a mask, through the second sacrificial material layer 210' to expose the third stand-off 202a', the fourth stand-off 202b', and a portion of the carrier second surface 108'. The first sacrificial material layer opening 234 and the second sacrificial material layer opening 234' may be formed by any technique known in the art, including but not limited to photolithography, wherein the first copper layer 102 and the second copper layer 102' may act as etch stops.

As shown in FIG. 19, package-on-package (PoP) pads may be formed on the protective layers (e.g. elements 220 and 220'). FIG. 19 illustrates a first package-on-package pad 228a and a second package-on-package pad 228b formed on the first protective layer 220, and a third package-on-package pad 228a' and a fourth package-on-package pad 228b' formed on the second protective layer 220'. Metallization layers (i.e. elements 226a, 226b, 226a', and 226b' may be disposed between their respective protective layers (e.g. elements 220 and 220') and their respective package-on-package pads (e.g. elements 228a, 228b, 228a', and 228b'). As will be understood those skilled in the art, the package-on-package pads may be used to form connections between microelectronic device packages in the z-direction for stacking (e.g. referred to as 3D stacking), without the need for through silicon vias. The package-on-package pads may be formed by any technique known in the art, including deposition, photolithographic patterning, and etching.

As shown in FIG. 20, a first microelectronic device 242 may be attached by a back surface 250 thereof with an adhesive material 244 to the carrier first surface 108 within the first sacrificial material layer opening 234. The first microelectronic device 242 may have at least one contact land (shown as elements 246a and 246b) on an active surface 248 thereof. A second microelectronic device 242' may be attached by a back surface 250' with an adhesive material 244' to the carrier second surface 108' within the second sacrificial material layer opening 234'. The second microelectronic device 242' may have at least one contact land (shown as elements 246a' and 246b') on an active surface 248' thereof. The first microelectronic device 242 and the second microelectronic device 242' may be any desired device, including but not limited to a microprocessor (single or multi-core), a memory device, a chipset, a graphics device, an application specific integrated circuit, or the like. The adhesive material 244 and 244' may be any appropriate material, including but not limited to a die backside film.

At least one secondary device may then be attached to a respective stand-off. As shown in FIG. 21, a first secondary device 274a may be attached to the first stand-off 202a with an adhesive material 276a, a second secondary device 274b may be attached to the second stand-off 202b with an adhesive material 276b, a third secondary device 274a' may be attached to the third stand-off 202a' with an adhesive material 276a', and a fourth secondary device 274b' may be attached to the fourth stand-off 202b' with an adhesive material 276b'.

As shown in FIG. 22, a first dielectric layer 252 may be formed on the first microelectronic device 242, the first protective layer 220, the first package-on-package pads 228a, the second package-on-package pads 228b, the first secondary device 274a, and the second secondary device 274b. A second dielectric layer 252' may be simultaneously formed on the second microelectronic device 242', the second protective layer 220', the third package-on-package pad 228a', the fourth package-on-package pad 228b', the third secondary device 274a', and the fourth secondary device 274b'. As also shown in FIG. 22, a plurality of openings 254 may be formed in the first dielectric layer 252 to expose at least a portion of each opening's 254 respective the first microelectronic device contact lands 246a and 246b, the first package-on-package pad 228a, the second package-on-package pad 228b, the first secondary device 274a, and the second secondary device 274b. A plurality of openings 254' may be simultaneously formed in the second dielectric layer 252' to expose at least a portion of each opening's 254' respective the second microelectronic device contact lands 246a' and 246b', the third package-on-package pad 228a', the fourth package-on-package pad 228b', the third secondary device 274a', and the fourth secondary device 274b'. In one embodiment, the first dielectric layer 252 and the second dielectric layer 252' may comprise silica-filled epoxy. The openings 254 and 254' may be formed by any technique known in the art including but not limited to laser drilling, ion drilling, etching, and the like.

As shown in FIG. 23, a conductive material may be disposed within the first dielectric layer openings 254 (see FIG. 22), by any technique known in the art, to form a first microelectronic device contact land first conductive via 266a, a first microelectronic device contact land second conductive via 266b, a first package-on-package pad conductive via 262a, a second package-on-package pad conductive via 262b, a first secondary device first conductive via 264_1a, a first secondary device second conductive via 264_2a, a second secondary device first conductive via 264_1b, and a second secondary device second conductive via 264_2b. The conductive material may also be simultaneously disposed within the second dielectric layer openings 254' to form a second microelectronic device contact land first conductive via 266a', a second microelectronic device contact land second conductive via 266b', a third package-on-package pad conductive via 262a', a fourth package-on-package pad conductive via 262b', a third secondary device first conductive via 264_1a', a third secondary device second conductive via 264_2a', a fourth secondary device first conductive via 264_1b', and a fourth secondary device second conductive via 264_2b'. As further shown in FIG. 23, conductive traces may

be formed to electrically connect various conductive vias. As illustrated, a first conductive trace 268a may be formed to electrically connect at least one of the first secondary device first conductive via 264_1a and the first secondary device second conductive via 264_2a, and the first microelectronic device contact land first conductive via 266a. A second conductive trace 268b may be formed to electrically connect at least one of the second secondary device first conductive via 264_1b and the second secondary device second conductive via 264_2b, and the first microelectronic device contact land second conductive via 266b. Further, a third conductive trace 268a' may be formed to electrically connect at least one of the third secondary device first conductive via 264_1a' and the third secondary device second conductive via 264_2a', and the second microelectronic device contact land first conductive via 266a'. A fourth conductive trace 268b' may be formed to electrically connect at least one of the fourth secondary device first conductive via 264_1b' and the fourth secondary device second conductive via 264_2b', and the second microelectronic device contact land second conductive via 266b'. Thus, the connection of the various conductive vias and conductive traces form electrically conductive paths between the secondary devices pads and the microelectronic device. The conductive traces (e.g. elements 268a, 268b, 268a', and 268b') may be any appropriate conductive material.

It is understood that the additional dielectric layer, conductive vias, and conductive traces may be built up to form a desired number of layers. Once a desired number of layers are formed, exterior layers, such as a glass cloth layer, may be formed. As shown in FIG. 23, a first exterior layer 272 may be formed on the first dielectric layer 252 and a second exterior layer 272' may be formed on the second dielectric layer 252'. The exterior layers (i.e. first exterior layer 272 and second exterior layer 272') may be used to engineer inherent warpages/stresses in microelectronic packages, as will be understood to those skilled in the art.

The structures thus formed on the carrier first surface 108 and on the carrier second surface 108' may be separated from one another with a depaneling process. FIG. 24 illustrates the structure formed on the carrier first surface 108 after depaneling, wherein the stand-offs 202a and 202b (see FIG. 23) may be removed by any appropriate technique known in the art. It is understood that if the stand-offs 202a and 202b are copper as is the carrier layers, the stand-offs 202a and 202b may be removed during the depaneling process. As shown in the FIG. 25, the first sacrificial material layer 210 (see FIG. 24) may be removed, such as by plasma ashing or solvent release, as will be understood to those skilled in the art, and the first microelectronic device adhesive layer 244 and the secondary

device adhesive layers 276a and 276b may also be removed from the first microelectronic device 242, such as by plasma ashing or a dissolution chemical, as also shown in FIG. 25, to form a microelectronic device package 280. It is understood that if plasma ashing is used to remove the first sacrificial material layer 210, the first microelectronic device adhesive layer 244 may also be removed in a single step.

As can be seen in FIG. 25, the process of FIGs. 14-25 may result in a secondary device (e.g. elements 274a and 274b) which is disposed within a thickness T of the first microelectronic device 242 (i.e. between the first microelectronic device active surface 148 and the first microelectronic device back surface 250).

It is noted that the secondary devices (i.e. elements 274a, 274b, 274a', and 274b' (see FIG. 21)) need not share the same opening (i.e. elements 234, 234' (see FIG. 18)) as the microelectronic devices 244 and 244' (see FIG.21)). Unique openings can be created for the secondary devices and the microelectronic devices separately to allow optimization, such as minimal build-up layer thickness variability or warpage engineering, as will be understood to those skilled in the art.

FIGs. 26-38 illustrate cross-sectional views of another embodiment of a process of forming a bumpless build-up layer coreless (BBUL-C) microelectronic package with embedded device-side secondary devices. As shown in FIG. 26, a carrier, such as the carrier 100 of FIG. 1, may be provided, wherein a first stand-off material layer 302 may be deposited over the carrier first surface 108 and a second stand-off material layer 302' may be simultaneously deposited over the carrier second surface 108'. The first stand-off material layer 302 and the second stand-off material layer 302' may be formed of any appropriate material, including but not limited to a photoresist material, and formed by any technique known in the art, including but not limited to spin coating, dry photofilm lamination, and chemical vapor deposition. In one embodiment, the first stand-off material layer 302 and the second stand-off material layer 302' may be deposited to thickness of between about 30μm and 100μm.

As shown in FIG. 27, an opening 304 may be formed through the first stand-off material layer 302 to expose a portion of the carrier first surface 108, and an opening 304' may be formed simultaneously in second stand-off material layer 302' to expose a portion of the carrier second surface 108'. The first stand-off material layer opening 304 and the second stand-off material layer opening 304' may be formed by any technique known in the art, including but not limited to photolithographic patterning and developing.

As shown in FIG. 28, when a photoresist material is used to form the first stand-off material layer 302 and the second stand-off material layer 302', the photoresist material may be flood exposed (e.g. crosslinked) by exposure to radiation (e.g. light), which is shown as arrows 306 and 306', respectively. As shown in FIG. 29, a first sacrificial material layer 310, such as a photoresist material, may be formed over the first stand-off material layer 302 and in the first stand-off material layer opening 304 (see FIG. 27) and a second sacrificial material layer 310', such as a photoresist material, may be formed over the second stand-off material layer 302' and in the second stand-off material layer opening 304' (see FIG. 27). The first sacrificial material layer 310 and the second sacrificial material layer 310' may be formed by any technique known in the art, including but not limited to spin coating, dry photofilm lamination, and chemical vapor deposition. In one embodiment, the first sacrificial material layer 310 and the second sacrificial material layer 310' may be deposited to thickness of between about 300μm and 600μm.

As shown in FIG. 30, an opening 332 may be formed through the first sacrificial material layer 310 to expose a portion of the first stand-off material layer 310 and a portion of the carrier first surface 108, and an opening 332' may be formed simultaneously in the second sacrificial material layer 310' to expose a portion of the second sacrificial material layer 310' and a portion of the carrier second surface 108'. The first sacrificial material layer opening 332 and the second sacrificial material layer opening 332' may be formed by any technique known in the art, including but not limited to photolithographic patterning and developing. It is understood that if photoresist materials are used for the stand-off material layers and the sacrificial material layers, the crosslinking of the first stand-off material layer 302 and second stand-off material layer 302', as shown in FIG. 28, may result in the first stand-off material layer 302 and second stand-off material layer 302' being substantially unaffected during the formation of the first sacrificial material layer opening 332 and the second sacrificial material layer opening 332'.

As shown in FIG. 31, a first microelectronic device 342 may be attached by a back surface 350 thereof with an adhesive material 344 to the carrier first surface 108 within the first sacrificial material layer opening 332. The first microelectronic device 342 may have at least one contact land (shown as elements 346a and 346b) on an active surface 348 thereof. A second microelectronic device 342' may be attached by a back surface 350' with an adhesive material 344' to the carrier second surface 108' within the second sacrificial material layer opening 332'. The second microelectronic device 342' may have at least one contact land (shown as elements 346a' and 346b') on an active surface 348'

thereof. The microelectronic devices may be any desired devices, including but not limited to a microprocessor (single or multi-core), a memory device, a chipset, a graphics device, an application specific integrated circuit, or the like.

At least one secondary device may then be attached to a respective stand-off material. As further shown in FIG. 31, a first secondary device 374a may be attached to the first stand-off material layer 302 with an adhesive material 376a, a second secondary device 374b may be attached to the first stand-off material layer 302 with an adhesive material 376b, a third secondary device 374a' may be attached to the second stand-off material layer 302' with an adhesive material 376a', and a fourth secondary device 374b' may be attached to the second stand-off material layer 302b' with an adhesive material 376b'.

As shown in FIG. 32, a first dielectric layer 352 may be formed on the first microelectronic device 342, the first secondary device 374a, and the second secondary device 374b. A second dielectric layer 352' may be simultaneously formed on the second microelectronic device 342', the third secondary device 374a', and the fourth secondary device 374b. As also shown in FIG. 32, a plurality of openings 354 may be formed in the first dielectric layer 352 to expose at least a portion of each opening's 354 respective the microelectronic device contact lands 346a and 346b, the first secondary device 374a, and the second secondary device 374b. A plurality of openings 354' may be formed in the second dielectric layer 352' to expose at least a portion of each opening's 354' respective microelectronic device contact lands 346a' and 346b', third secondary device 374a', or fourth secondary device 374b'. In one embodiment, the first dielectric layer 352 and the second dielectric layer 352' may comprise silica-filled epoxy. The openings 354 and 354' may be formed by any technique known in the art including but not limited to laser drilling, ion drilling, etching, and the like.

As shown in FIG. 33, a conductive material may be disposed within the first dielectric material layer openings 354 (see FIG. 32), by any technique known in the art, to form a first microelectronic device contact land first conductive via 366a, a first microelectronic device contact land second conductive via 366b, a first secondary device first conductive via 364_1a, a first secondary device second conductive via 364_2a, a second secondary device first conductive via 364_1b and a second secondary device second conductive via 364_2b. The conductive material may also be simultaneously disposed within the second dielectric material layer openings 354' (see FIG. 32) to form a second microelectronic device contact land first conductive via 366a', a second microelectronic

device contact land second conductive via 366b', a third secondary device first conductive via 364_1a', a third secondary device second conductive via 364_2b', a fourth secondary device first conductive via 364_1b', and a fourth secondary device second conductive via 364_2b'. As further shown in FIG. 33, conductive traces may be formed to electrically connect various conductive vias. As illustrated, a first conductive trace 368a may be formed to electrically connect at least one of the first secondary device first conductive via 364_1a and the first secondary device second conductive via 364_2a, and the first microelectronic device contact land first conductive via 366a. A second conductive trace 368b may be formed to electrically connect at least one of the second secondary device first conductive via 364_1b and the second secondary device second conductive via 364_2b, and the first microelectronic device contact land second conductive via 366b. Further, a third conductive trace 368a' may be formed to electrically connect at least one of the third secondary device first conductive via 364_1a' and the third secondary device second conductive via 364_2a', and the second microelectronic device contact land first conductive via 366a'. A fourth conductive trace 368b' may be formed to electrically connect at least one of the fourth secondary device first conductive via 364_1b' and the fourth secondary device second conductive via 364_2b', and the second microelectronic device contact land second conductive via 366b'. Thus, the connection of the various conductive vias and conductive traces form electrically conductive paths between the secondary devices pads and the microelectronic device. The conductive traces (e.g. elements 368a, 368b, 368a', and 368b') may be any appropriate conductive material.

It is understood that the additional dielectric layers, conductive vias, and conductive traces may be built up to form a desired number of layers. Once a desired number of layers are formed, exterior layers, such as a glass cloth layers, may be formed. As shown in FIG. 33, a first exterior layer 372 may be formed on the first dielectric layer 352 and a second exterior layer 372' may be formed on the second dielectric layer 352'. The exterior layers (i.e. first exterior layer 372 and second exterior layer 372') may be used to engineer inherent warpages/stresses in microelectronic packages, as will be understood to those skilled in the art.

The structures thus formed on the carrier first surface 108 and on the carrier second surface 108' may be separated from one another with a depaneling process, as known in the art. FIG. 34 illustrates the structure formed on the carrier first surface 108 after depaneling.

As shown in FIG. 35, the first stand-off material layer 302 and the first sacrificial material layer 310 may be removed, such as by a solvent release. The first microelectronic device adhesive material layer 344, the first secondary device adhesive material 376a, and the second secondary device adhesive material 376b (see FIG. 34) may then be removed, such as by plasma ashing, as shown in FIG. 36, to form a microelectronic device package 380.

It is understood that a controlled plasma ashing could be used to simultaneously remove the first stand-off material layer 302, the first sacrificial material layer 310, the first microelectronic device adhesive material layer 344, the first secondary device adhesive material 376a, and the second secondary device adhesive material 376b. It is further understood that a controlled plasma ashing could be used to remove the first stand-off material layer 302, the first microelectronic device adhesive material layer 344, the first secondary device adhesive material 376a, and the second secondary device adhesive material 376b, while leaving the first sacrificial material layer 310 in place, as shown in FIG. 37, to form a microelectronic device package 390.

As can be seen in FIG. 36 and 37, the process of FIGs. 26-37 may result in a secondary device (e.g. elements 374a and 374b) which is disposed within a thickness T of the first microelectronic device 342 (i.e. between the first microelectronic device active surface 348 and the first microelectronic device back surface 350).

Although the embodiment illustrated in FIGs. 28-37 show in stand-off layer being formed for a microelectronic device package, it is understood that multiple stand-off material layers could be formed and various pockets or cavities could be formed within the materials to allow for the creation of various package architectures for microelectronic device and package stacking and also multi-device embedding, as will be understood to those skilled in the art.

It is understood that the subject matter of the present description is not necessarily limited to specific applications illustrated in FIGs. 1-37. The subject matter may be applied to other microelectronic device packaging applications. Furthermore, the subject matter may also be used in any appropriate application outside of the microelectronic device fabrication field. Moreover, the subject matter of the present description may be a part of a larger bumpless build-up package, it may include multiple stacked microelectronic dice, it may be formed at a wafer level, or any number of appropriate variations, as will be understood to those skilled in the art.

Having thus described in detail embodiments of the present invention, it is understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.

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CLAIMS

What is claimed is:

1. A microelectronic device package comprising:
a microelectronic device having an active surface and an opposing back surface, wherein a thickness of the microelectronic device is defined by the distance between the microelectronic device active surface and the microelectronic device back surface;

at least one secondary device electrically connected to the microelectronic device, wherein the at least one secondary device is positioned proximate the microelectronic device within the thickness of the microelectronic device; and

a dielectric layer disposed over the microelectronic device active surface and the at least one secondary device;

wherein the dielectric layer abuts a portion of the microelectronic device between the microelectronic device active surface and the microelectronic back surface, and wherein the microelectron back surface and a portion of the microelectronic device between the microelectronic device active surface and the microelectronic back surface is exposed through the dielectric layer.

2. The microelectronic device package of claim 1, wherein the at least one secondary device comprises at least one capacitor.

3. The microelectronic device package of claim 1, further including an electrically conductive path between the at least one secondary device and the microelectronic device comprising:
a first conductive via extending through the dielectric layer electrically connected to the at least one secondary device;

a second conductive via extending through the dielectric layer electrically connected to the microelectronic device; and

a conductive trace electrically connecting the first conductive via to the second conductive via.

4. The microelectronic device package of claim 3, wherein the dielectric layer is disposed over the at least one secondary device.

5. The microelectronic device package of claim 3, wherein the dielectric layer comprises a silica-filled epoxy.