TRANSISTORS HAVING SELF-ALIGNED BODY TIE

CROSS-REFERENCE TO RELATED APPLICATION(S)

[0001] This application claims priority to U.S. Provisional Application No. 63/168,887 filed March 31, 2021, entitled TRANSISTORS HAVING SELF-ALIGNED BODY TIE, the disclosure of which is hereby expressly incorporated by reference herein in its respective entirety.

BACKGROUND

Field

[0002] The present disclosure relates to transistors having self-aligned body tie.

Description of the Related Art

[0003] In metal–oxide–semiconductor field-effect transistors (MOSFETs) such as silicon-on-insulator transistors, a floating-body configuration can provide lower parasitic effects than a body-connected configuration. Thus, floating-body silicon-on-insulator transistors tend to provide better performance than body-connected silicon-on-insulator transistors. However, floating-body effect can limit practical applications of floating-body silicon-on-insulator transistors.

SUMMARY

[0004] In accordance with an aspect, the present disclosure relates to a transistor includes a source and a drain each implemented in a first type active region, a gate implemented relative to the source and the drain, and a body implemented in the first type active region and substantially covered by the gate. The transistor further includes a body tie implemented in a second type active region and including a connecting portion substantially covered by the gate and engaging the body, with the first and second active regions dimensioned to provide a gap therebetween on each side of the gate.

[0005] In some embodiments, the first type active region can include an N+ active region, and the second type active region can include a P+ active region. In some embodiments, the gate can have a symmetric shape about a line

along a width direction of the gate. In some embodiments, the gate can have an I shape that covers the body and the connecting portion of the body tie.

[0006] In some embodiments, the connecting portion of the body tie can be aligned with the body based on a shape of the gate. In some embodiments, the aligned configuration of the connecting portion of the body tie and the body can result from formation of the gap between the first and second active region on each side of the gate. In some embodiments, the aligned engagement between the connecting portion of the body tie and the body can be the only engagement between the body tie and the body.

[0007] In an aspect, the present disclosure relates to a method for fabricating a transistor. The method includes forming or providing a first type active region and a second type active region, implementing a source and a drain with the first type active region, forming a body tie with the second type active region, and forming a gate relative to the source and the drain. The method further includes dimensioning either or both of the first and second type active regions to provide a gap between the first and second type active regions on each side of the gate, such that a connecting portion of the body tie engaging the body is substantially covered by the gate.

[0008] In some embodiments, the first type active region can include an N+ active region, and the second type active region can include a P+ active region. In some embodiments, the forming of the gate can include forming a symmetric shaped gate about a line along a width direction of the gate. In some embodiments, the gate can have an I shape that covers the body and the connecting portion of the body tie.

[0009] In some embodiments, the dimensioning can include removing portions of the first type active region to provide the gaps on both sides of the gate with a mask protecting the gate during the removing step. In some embodiments, the forming of the gaps with the mask protecting the gate can result in a body under the gate and the connecting portion of the body tie under the gate being aligned with each other based on a shape of the gate. In some embodiments, the aligned engagement between the connecting portion of the body tie and the body can be the only engagement between the body tie and the body.

[0010] According to an aspect, the present disclosure relates to a semiconductor die that includes a substrate and one or more transistors implemented on the substrate. Each transistor includes a source and a drain each implemented as a first type active region, and a gate implemented relative to the source and the drain such that application of a voltage to the gate results in formation of a conductive channel between the source and the drain. The transistor further includes a body configured to provide the conductive channel upon the application of the voltage to the gate. The body is implemented in the first type active region and substantially covered by the gate. The transistor further includes a body tie implemented as a second type active region and including a connecting portion substantially covered by the gate and engaging the body, with the first and second active regions being dimensioned to provide a gap therebetween on each side of the gate.

[0011] In some embodiments, the substrate can include a silicon-on-insulator substrate. In some embodiments, each transistor can be configured as a radio-frequency transistor. In some embodiments, each transistor can be configured as a digital cell transistor or a switching transistor.

[0012] In an aspect, the present disclosure relates to a packaged module that includes a packaging substrate and a semiconductor die mounted on the packaging substrate. The semiconductor die includes one or more transistors. Each transistor includes a source and a drain each implemented as a first type active region, and a gate implemented relative to the source and the drain such that application of a voltage to the gate results in formation of a conductive channel between the source and the drain. The transistor further includes a body configured to provide the conductive channel upon the application of the voltage to the gate. The body is implemented in the first type active region and substantially covered by the gate. The transistor further includes a body tie implemented as a second type active region and including a connecting portion substantially covered by the gate and engaging the body, with the first and second active regions being dimensioned to provide a gap therebetween on each side of the gate.

[0013] In an aspect, the present disclosure relates to an electronic device that includes a power source and an integrated circuit implemented on a semiconductor die and powered by the power source. The

integrated circuit includes one or more transistors. Each transistor includes a source and a drain each implemented as a first type active region, and a gate implemented relative to the source and the drain such that application of a voltage to the gate results in formation of a conductive channel between the source and the drain. The transistor further includes a body configured to provide the conductive channel upon the application of the voltage to the gate. The body is implemented in the first type active region and substantially covered by the gate. The transistor further includes a body tie implemented as a second type active region and including a connecting portion substantially covered by the gate and engaging the body, with the first and second active regions being dimensioned to provide a gap therebetween on each side of the gate.

[0014] In some embodiments, the integrated circuit can include a switching circuit, and each of the one or more transistors can be implemented as a switching transistor. In some embodiments, the electronic device can be a wireless device.

[0015] In some embodiments, each of the one or more transistors can be implemented as digital cell.

[0016] For purposes of summarizing the disclosure, certain aspects, advantages and novel features of the inventions have been described herein. It is to be understood that not necessarily all such advantages may be achieved in accordance with any particular embodiment of the invention. Thus, the invention may be embodied or carried out in a manner that achieves or optimizes one advantage or group of advantages as taught herein without necessarily achieving other advantages as may be taught or suggested herein.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] Figure 1 depicts a transistor having one or more features as described herein.

[0018] Figure 2 shows that in some embodiments, the transistor of Figure 1 can be implemented in a circuit and/or a device.

[0019] Figure 3 shows an example of a silicon-on-insulator (SOI) transistor having a T-shaped gate and a conventional body tie configuration.

[0020] Figures 4A and 4B show sectional views as indicated in Figure 3.