

**A Method and Apparatus for Fabricating a Circuit Board with a Three Dimensional
Surface Mounted Array of Semiconductor Chips**

5 RELATED APPLICATIONS

The present application claims priority under 35 USC §119(e) from United States provisional application serial number 60/275,843, filed March 14, 2001 and entitled "A Method and Apparatus for Fabricating a Circuit Board with a Three Dimensional Surface Mounted Array
10 of Semiconductor Chips".

FIELD OF THE INVENTION

15 The present invention relates to a semiconductor manufacturing process and more particularly to a method and system for fabricating semiconductor chips in a three-dimensional array on a printed circuit board.

BACKGROUND OF THE INVENTION

20 Semiconductor chips are typically connected to a printed circuit board that in turn interconnects the chip into the rest of circuitry with which the chip will operate including other chips on the printed circuit board. In the past the chips were spread out across the printed circuit board on their large flat sides in a simple two-dimensional array. Over the years the trend in the computer industry has been towards more densely packed printed circuit boards. Among the
25 causes for this are the increasing demand for larger random access computer memories, demand for faster computers, demand for more compact computers and a push to decrease costs of printed circuit boards by increasing the circuit density on the printed circuit board. In the mid to late 1980's the industry switched over from a technology that attached computer chips to a printed circuit board through holes in the printed circuit board to one that used a surface mounting
30 technology. With the advent of surface mount technology, conventional through-holes on printed circuit boards have been replaced with conductive mounting pads on the surface of the printed circuit board. This allows for multiple layered circuit boards with a complex network of

interconnect lines running between the layers of the board. In turn this has allowed for the increase in the density of chips on a printed circuit board which not only decreases the size of the board but increases the operating speed of the computer by reducing the distance signals have to travel between chips on the board.

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The move to surface mount technology has consequently resulted in the practice of positioning the chips on the printed circuit board in a variety of configurations to increase chip density on the circuit board and thereby decrease the distance between the chips to speed up operation of the overall system. Generally, conventional configurations stack the chips on one another to increase density. The practice of stacking the chips on one another is particularly adaptable to memory chips given the redundancies in their circuits. Up until the present, in order for the chips to be stacked on one another to increase chip density and achieve a three-dimensional array on the circuit board, computer makers had to send the chips to a third party manufacturer that specialized in the technique of permanently bonding chips in a stacked fashion. Stacking the chips generally consisted of soldering them together. This in turn created a variety of problems including time delays inherent in having to rely on an outside manufacturing facility and potential damage to the chip as a result of directly soldering the chips together.

Recent developments, in particular those of the applicant of the present invention have resulted in new and much more efficient means for stacking chips on a printed circuit board in a three dimensional array. These developments are described in detail in copending patent applications owned by the applicant herein, they being: United States patent application for a "Circuit Board Assembly Having A Three Dimensional Array of Integrated Circuit Packages" serial number 09/285,354 filed April 4, 1999, and United States patent application for a "Electronic Module Having a Three Dimensional Array of Carrier-Mounted Integrated Circuit Packages" serial number 09/524,324 filed March 3, 2000. Both of these applications are incorporated herein by reference and made part hereof as if set forth herein at length. The two referenced applications describe a unique electronic module that in effect provides a platform that is placed over a chip on a circuit board and connects to contact pads on the circuit board that the platform shares with the chip underneath it. The second chip is then connected to the top of the

platform to achieve a stacked three-dimensional array as more fully described in the above referenced patent applications. 21A and 21B of Fig. 1 depict two different variations of the chip carriers described and claimed in the two above referenced applications. 21A depicts a chip carrier made in the form of a printed circuit board and 21B depicts a chip carrier made in a molded packaging.

However, in order to maximize the advantages of the electronic chip carrying modules described in the two above mentioned copending applications what is needed is a manufacturing process and apparatus which will automate and optimize their installation. Additionally, it should be a manufacturing process and apparatus that can be used in house by a computer or circuit board manufacturer without the need to use the services of a third party manufacturer.

SUMMARY

It is an object of the present invention to provide an efficient and cost effective manufacturing process and apparatus that utilize new developments that allow the placing chips in a three dimensional array on a printed circuit board. It is a further object of the present invention to provide an apparatus and method that can be utilized with current methods and semiconductor manufacturing machines used in the assembly of printed circuit boards.

These and other objects are achieved by providing a method for populating a circuit board with a three dimensional array of semiconductor chips with the following steps: a) verifying electrical contacts on a plurality of chip carriers are properly aligned for an assembly process; b) preparing a chip receiving side of said chip carriers to receive a chip and passive components; c) preparing a circuit board for a chip assembly process; d) populating said circuit board with a first layer of chips and passive components said chips and passive components being positioned to make contact with preselected predetermined electrical contact points; e) positioning said chip carriers over said first layer of chips so that said chip carriers make contact with pre-selected electrical contact points on said circuit board; f) placing on each of said chip carriers a semiconductor chip with passive components; and g) interconnecting in a permanent fashion

said chips, passive components and chip carriers to said circuit board.

In another aspect of the invention it provides a system for populating a circuit board with a three dimensional array of semiconductor chips comprising: a) a plurality of chip carriers attachable to a circuit board with space for a chip to be positioned directly on the circuit board beneath of each chip carrier as well as for positioning a chip on top of the chip carrier to thereby create a three dimensional array of chips on the circuit board; b) a pallet for holding and moving a plurality of chip carriers during a circuit board assembly process, the pallet having a matrix of chambers in a frame like form with the chambers being open at least at a top side of the pallet each chamber being formed to hold a chip carrier during the circuit board assembly process, the chip carriers being positioned in each of the chambers of the pallet with a top, chip receiving side, of the chip carrier facing out from the top of the pallet to thereby make the top side of the chip carrier accessible during the circuit board assembly process; and c) a mechanism to move and position the pallet during the assembly process so that the plurality of chip carriers held by the pallet can be prepared to receive a chip during the assembly process and easily accessed, removed from the pallet and positioned on the circuit board over chips positioned directly on the circuit board with chips positioned on each chip carrier to thereby create a three dimensional array of chips on the circuit board.

In still another aspect of the invention it provides an apparatus for positioning and securely but detachably holding a chip module during a semiconductor fabrication process comprising: a) a pallet for holding chip modules the pallet having a two dimensional matrix of chambers, the chambers being open at a first and second opposing parallel sides of the pallet, the chambers having at a base adjacent to the opening on the second side of the pallet a flange around the inside of the chamber to allow the chamber to retain a chip module of approximately the same dimensions as the chamber when the first side of the pallet faces up; b) a print fixture pedestal with a two dimensional matrix of raised portions that match the matrix of the chambers of the pallet such that the raised portions are sized such that the raised portions fit on a one for one basis into the chambers of the pallet from the second side of the pallet; and c) wherein when the chambers are filled with chip modules and a the print fixture pedestal is joined with the pallet at

the pallets second side the raised portions elevate chip modules located in the chambers to a work position from which they can be worked on from the first side of the pallet.

BRIEF DESCRIPTION OF THE DRAWINGS

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The invention will be better understood by an examination of the following description, together with the accompanying drawings, in which:

Fig. 1 depicts two different versions of the electronic chip carrying modules;

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Fig. 2 is a raised perspective view of the pallet that holds the electronic chip carrying modules during the manufacturing process of the present invention;

Fig. 2A is a cross sectional view of the pallet depicted in Fig. 2 along line I-I;

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Fig. 3 is a raised perspective view of a print fixture pedestal of the present invention used in the stenciling step of the chip carrying modules;

Fig. 3A is a cross sectional view of the print fixture pedestal depicted in Fig. 3 along

20 line II-II;

Fig. 4 is a view of the bottom the print fixture pedestal of the present invention;

Fig. 5 is top view of a stencil used in the manufacturing process of the present

25 invention;

Fig. 6 is a side view of the pallet and print fixture pedestal joined together for one of the stages of the manufacturing process of the present invention;

30 Fig. 6A is a cross sectional view from Fig. 6 at III of one chamber of the pallet with a

raised portion inserted therein supporting a chip carrier;

Fig. 7 is a view of the stenciling step of the present invention;

Fig. 8 is a view of the circuit board assembly step of the present invention; and

Fig. 9 is a side view of an oven used in the single reflow process of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The method of the preferred embodiment of the present invention uses a three step fabrication process that automates the surface mounting on a printed circuit board of the chip carriers similar to those depicted as 21A and 21B in Fig. 1 and as described in the above two copending applications referenced above that have already been incorporated herein by reference.

The first step involves the stenciling (the depositing of solder paste) on a large number of chip carriers 21 at one time. The second step involves moving the chip carriers to an assembly stage where they are placed on the circuit board over the chips and passive devices that have been placed directly onto the circuit board. Chips together with appropriate passive devices are then placed on the chip carriers. In the third and final stage the circuit board with components attached is passed through a single reflow process to complete permanent interconnection with solder of the various components on the board and chip carriers.

The preferred embodiment of the present invention uses two new devices to aid in the movement and stenciling of a large number of chip carriers at one time. During the fabrication process the chip carriers 21 are held by a chip carrier pallet 23 as depicted in Fig. 2. The preferred embodiment of pallet 23 as depicted has a total of fifty-four chambers 25 each one of which holds a chip carrier 21. In Fig. 2 only chambers 25A, 25B and 25C have chip carriers 21. Each of the chambers 25 in pallet 23 are open at the top 23A and bottom 23B of the pallet. The size of each of the chip carriers are approximately the same size as each chamber 25 in pallet 23

with the exception of four corner projections or flanges 22 on chip carriers 21. Each chip carrier is thus sized such that when a chip carrier is positioned in a chamber 25 the flanges 22 project beyond the chamber and rest on the top surface 23A of the pallet as demonstrated by 25A, 25B and 25C in Fig. 2. Thus, each chip is prevented from falling through chamber 25 when placed in the chamber.

Each chamber 25 in the preferred embodiment has four abutments 27 around the top outside edge as depicted in fig. 2. The abutments 27 are designed to hold the chip carriers 21 and protect the chip carriers when positioned in a chamber 27. The abutments 27 provide protection because a chip carrier 21 when positioned in a chamber 25 is located in a recessed position below the top of the surrounding abutments 27. The pallet 23 can be made of a variety of materials including durable plastic, aluminum or any other suitable material. Fig. 2A is a cross sectional view of the pallet along line I-I that clearly shows the open tops 23A and bottoms 23B of chambers 25. The abutments 27 protect the top of each chip carrier 21 during the fabrication process while the chip carriers are in the chambers 25 of pallet 23. The tops of the chip carriers 21 are protected so that after solder paste is deposited on top of the carrier, as will be described below the pallets can be stacked and moved about without disturbing the solder paste on top of the chip carriers.

The second new device is the print fixture pedestal 31 shown in a raised perspective view in Fig. 3. The print fixture pedestal 31 has series of raised block like areas 33. The block like areas 33 are in a nine by six matrix that matches the nine by six matrix of chambers 25 of pallet 23. The matrix of raised areas 33 are designed and sized to fit into the bottom of the corresponding chamber 25 in the pallet 23. Print fixture pedestal 31 is hollow inside and each raised block area 33 has a top opening 35 that opens into the hollow interior of print fixture pedestal 31. Fig. 4 provides a bottom view of the print fixture pedestal 31. Some of the top openings 35 can be seen through circular opening 39 of the bottom plate 41 of the print fixture pedestal 31. Fig. 3A is a cross sectional view of print fixture pedestal 31 along line II-II of Fig. 3. The hollow interior 36 can be seen in Fig. 3A. The bottom plate 41 secures to a movable hollow shaft, not shown. The hollow portion of the shaft opens into the hollow interior 36 of print fixture pedestal 31. Print

fixture pedestal 31 can be made of cast aluminum or any other of a number of suitable materials.

Print fixture pedestal 31 is designed to fit like a glove into the bottom of pallet 23 and raise and secure the chip carriers 21 in the chambers 25 of pallet 23. When print fixture pedestal 31 is joined with pallet 23 (Fig. 6), top openings 35 are flush against the bottoms of the chip carriers located in chambers 25 and a sealed space 36 is created in print fixture pedestal 31 to create a slight vacuum to hold chip carriers 21 during the stenciling process as will be explained in more detail below. Fig. 6A is a cross section along line III of Fig. 6 of one chamber 25 with a raised portion 33 inserted therein supporting a chip carrier 21. As can be seen raised area 33 positioned in a chamber 25 has its top opening 35 flush against the bottom 29 of a chip carrier 21.

Fig 5 provides a top view of a stencil 47 used in the stenciling process. Stencil 47 is a template used to deposit solder on the connector pads 46 (Figs. 1 and 2) of the chip carriers 21 when they are positioned in the chambers 25 of pallet 23 and chip carriers 21 are securely held by the print fixture pedestal 31. As will be shown below, stencil 47 is placed over the pallet 23 when it is filled with chip carriers 21 and the matrix of rows of holes 49 on stencil 47 match up with the contact pads 46 on top of the chip carriers in each of the chambers 25 of the pallet 23. Stencil 47 is usually a made of a sheet of stainless steel or some other similarly suitable material.

The preferred embodiment of the present invention uses an automated stencil printer for the stenciling process. As depicted in Fig. 6 pallet 23 filed with chip carriers 21 with print fixture pedestal 31 positioned underneath it is positioned on the work nest 51. Also, as noted above when print fixture pedestal is joined to pallet 23 this raises chip carriers 21 partially out of the top of chambers 25 of pallet 23. Referring next to Fig. 7 work nest 51 with the joined print fixture pedestal 31 and pallet 23 are positioned below the stencil 47. Stencil 47 is positioned by an appropriate positioning apparatus with the aid of a special bi-directional camera not shown that is inserted between the stencil 47 and pallet 23 in a process well known in the art. The camera lines up the stencil and pallet by keying off of fiducials located on the stencil 47 and pallet 23. Once the machine assures correct alignment, print fixture pedestal 31 and pallet 23 are raised by work nest 51 towards stencil 47 until the tops of the chip carriers 21, positioned in pallet 23, abut up

against stencil 27. Work nest 51 has pneumatic means to raise and lower the enter structure. At this point solder deposition mechanism 59 is lowered onto the top of stencil 47 and the solder is deposited through the array of matrix holes 49 of the stencil. Matrix holes 49 expose the contact pads 46 of chip carriers 21 so that mechanism 59 can precisely deposit the solder on the contact pads. Once completed, mechanism 59 is raised from stencil 47 and stencil 47 is retracted upward. Since the chip carriers are being securely held by the vacuum created between raised area 33 of print fixture pedestal 31 and the bottom of each of chip carriers 21 (see Fig. 6A) none of the chip carriers 21 will inadvertently stick to the stencil 47 pallet 23 is retracted or lowered.

Once the stenciling process has been completed pallet 23 is disengaged from print fixture pedestal 31 and the pallet 23 with stenciled chip carriers 21 is moved onto the next stage, the circuit board assembly process as depicted in Fig. 8. In the preferred embodiment of the circuit board assembly process a standard Pick and Place machine 60 is used. During the assembly process a gantry 61 with various pick and place nozzles 63 first places semiconductor computer chips 73 onto circuit board 65 together with various passive devices. The chips in Fig. 8 are being taken from tray 67 or alternatively a tape in a manner standard to the industry. Also, passive devices, i.e. resistors, capacitors, etc. are coming from rolls 69 in a manner standard to the industry. Once circuit board 65 is populated with the first layer of chips and passive devices gantry 61 then begins placement of the chip carriers 21 that it takes from pallet 23. Upon completion of placement of all of the chip carriers 21 on circuit board 65 it begins placing the chips on the chip carriers 21 together with appropriate passive devices. Fig. 9 depicts a portion of a completed circuit board 65 with first layer of chips 73, passive devices 75, chip carrier 21 and second layer of chips 77 and passive devices 79 on the chip carriers 21. During the placement process each chip, chip carrier and passive device placed on circuit board 65 is momentarily present to camera 81 (Fig. 8) for inspection. Any of these devices that appear on their surface to be defective are then discarded.

The third and final step is a single reflow process during which the circuit board 65 with components attached is passed through an oven 87 to permanently attach the components to the board by melting the solder previously placed on the board and chip carriers. Fig. 9 depicts board

65 entering oven 87. Use of a single reflow process avoids unduly stressing the circuit board and components attached to it since circuit board 65 has all of the components placed on it before going through oven 87. In the preferred embodiment a standard reflow oven is used. As is well known in the art the single reflow oven causes the solder paste to melt and thus fuse the various components placed on the board to the board including the chip carriers. Naturally, the components placed on each chip carrier to fuse to that chip carrier at the same time. One of the advantages of the present invention is that it allows all of the components, chips, chip carriers and passive components to be positioned in one step on the printed circuit board. Once in place the board is sent through an oven to melt the solder paste holding the components on the board and permanently to the board. This avoids the need to put the board through an oven a multiple number of times. However, those skilled in the art once they have reviewed this specification and understand the concepts of this invention will be able to adapt any number of commercially available fabrication machines for the stenciling, assembly or single reflow process.

While the invention has been particularly shown and described with reference to a preferred embodiment thereof, it will be understood by those skilled in the art that various changes in form and detail may be made to it without departing from the spirit and scope of the invention.

CLAIMS

1. A method for populating a circuit board with a three dimensional array of semiconductor chips comprising the steps of:

- 5 a) preparing a chip receiving side of a plurality of chip carriers to receive chips and passive components;
- b) positioning said chip carriers over a first layer of chips positioned on said board so that said chip carriers make contact with preselected electrical contact points
10 on said circuit board;
- c) placing on each of said chip carriers a semiconductor chip with passive components; and
- 15 d) interconnecting in a permanent fashion said chips, passive components and chip carriers to said circuit board.

2. The method of claim 1 further comprising the steps of:

- 20 a) verifying electrical contacts on a plurality of chip carriers are properly aligned for an assembly process;
- b) preparing a circuit board for a chip assembly process; and
- 25 c) populating said circuit board with a first layer of chips and passive components said chips and passive components being positioned to make contact with preselected predetermined electrical contact points.

3. The method of claim 1 wherein the additional step of holding said plurality of chip
30 carriers in a chip carrier pallet wherein said chip carriers are positioned in a flat matrix array with the chip receiving side of each of said plurality of chip carriers are exposed at a

top of said pallet so that during said stenciling step said chip carrying side of each chip can be accessed and so that during said positioning step each chip can be retrieved during said positioning step.

- 5 4. The method of claim 3 wherein said step of holding said chip carriers in a chip carrier pallet includes providing a matrix of chambers open at the top side and bottom side of said pallet, said pallet having a protective barrier that protects the chip carrier in a recessed position when the chip carriers are positioned in a chambers.
- 10 5. The method of claim 4 including the step of securing and positioning said chip carriers during said stenciling process with a print fixture pedestal having a matrix like array of protrusions, each protrusion being positioned and sized to fit into the bottom of a chamber in said pallet and engage securely but detachably the bottom side of a chip carrier in said chamber and thereby lift said chip carrier above said protective barrier
15 during said stenciling process, assure said chip carrier will disengage from said stenciling process when completed and return said chip carriers to said recessed position.
- 20 6. The method of claim 5 wherein said step of securing said chip carrier comprises said protrusion securing said bottom side of said chip carrier by a vacuum created by an aperture at the top of said protrusion surface which abuts against the bottom side of said chip carrier.
- 25 7. A system for populating a circuit board with a three dimensional array of semiconductor chips comprising:
30 a) a plurality of chip carriers attachable to a circuit board with space for a chip to be positioned directly on said circuit board beneath each chip carrier as well as for positioning a chip on top of said chip carrier to thereby create a three dimensional array of chips on said circuit board; and
b) a pallet for temporarily holding and moving said plurality of chip carriers during a

circuit board assembly process, said pallet having a matrix of chambers in a frame like form with the chambers being open at least at a top side of said pallet, each chamber being formed to hold a chip carrier during the circuit board assembly process, said chip carriers being positioned in each of said chambers of the pallet with a top, chip receiving side, of said chip carrier facing out from the top of said pallet to thereby make said top side of said chip carrier accessible during the circuit board assembly process.

8. The system of claim 7 further including a protective barrier to protect said chip carriers from unintended alteration during said assembly process.

9. The system of claim 8 wherein:

a) said chambers of said pallet are also open at a bottom side of said pallet and said protective barrier comprises a plurality of abutments around the outside top periphery of each of said chambers, said chip carriers having retaining flanges to allow them to rest in a chamber on said pallet and not fall through and said abutments being positioned such that when a chip carrier is in said chamber its top is below the top of said abutments and is thereby protected by said abutments from unintentional alteration; and

b) said system further comprising a print fixture pedestal having a matrix like array of raised portions with the matrix array of raised portions being positioned and formed such that each raised portion corresponds to a chamber of said pallet so that when said print fixture pedestal is positioned under said pallet with said raised portions facing said pallet each raised portion fits into the bottom opening of an adjacent chamber, a circumference of said raised portion being less than the inside circumference of said chamber so that a top surface of said raised portion can be positioned up against the bottom surface of a chip carrier in said chamber and securely but detachably hold said chip carrier during a circuit board assembly process.

10. The system of claim 9 wherein said raised portions each have an aperture at its top side which abuts against the bottom side of a chip carrier positioned in said chamber so that a vacuum can be created between said raised portion and said chip carrier to securely but detachably hold said chip carrier during said stenciling process.

5 11. The system of claim 9 wherein said print fixture pedestal during said circuit board assembly process is attached to a moving and positioning mechanism during said circuit board assembly process so that it can be positioned under said pallet with chip carriers to securely hold said chip carriers during said stenciling step and properly position said chip carriers during said stenciling step and assure that said chip carriers disengage at the completion of said stenciling step.

10 12. The system of claim 7 further including a mechanism to move and position said pallet during said assembly process so that said plurality of chip carriers held by said pallet can be prepared to receive a chip during said assembly process and easily accessed, removed from said pallet and positioned on said circuit board over chips positioned directly on said circuit board with chips positioned on each chip carrier to thereby create a three dimensional array of chips on said circuit board.

20 13. An apparatus for positioning and securely but detachably holding a chip module during a semiconductor fabrication process comprising:

25 a pallet for temporarily holding chip modules said pallet having a two dimensional matrix of chambers, said chambers being open at a first and second opposing parallel sides of said pallet, said chambers having said chambers being sized to accept and hold a chip carrier and said chambers further comprising a protective barrier to protect a chip carrier positioned within said chamber;

30 a print fixture pedestal with a two dimensional matrix of raised portions that match said matrix of said chambers of said pallet such that said raised portions are sized such that

said raised portions fit on a one for one basis into said chambers of said pallet from said second side of said pallet; and

5 wherein when said chambers are filled with chip modules and a said print fixture pedestal is joined with said pallet at said pallets second side said raised portions elevate chip modules located in said chambers to a work position from which they can be worked on from said first side of said pallet.

10 14. The apparatus of claim 13 wherein said raised portions have an opening at a top of each which leads into an interior space in said print fixture pedestal and when said print fixture pedestal is joined to said pallet the top of said raised portions are positioned against a bottom of a chip module located in each chamber and a vacuum can be created between said top of said raised portion and said chip module bottom to detachably but securely hold said chip module while it is being worked on, the vacuum being created by attaching
15 a bottom portion of said print fixture pedestal to a vacuum machine through a hollow shaft that attaches at an opening at the bottom of said print fixture pedestal said opening leading into the interior space of said print fixture pedestal.

20 15. The apparatus of claim 13 wherein said chip module is a chip carrier.

25 16. The apparatus of claim 13 wherein when said chambers of said pallet have chip modules positioned in them and the print fixture pedestal is not joined to said pallet the top of the modules are completely concealed in said chamber below a top surface of said first side of said pallet and when said print fixture pedestal is joined to said pallet to thereby raise the modules the top of each module projects above the top surface of the first side of said pallet.

30 17. The system of claim 13 wherein said protective barrier is a series of raised abutments located around the top outside edge of said chamber and said chip carriers having retaining flanges to allow said chip carriers to rest in the chamber below the height of the abutments.