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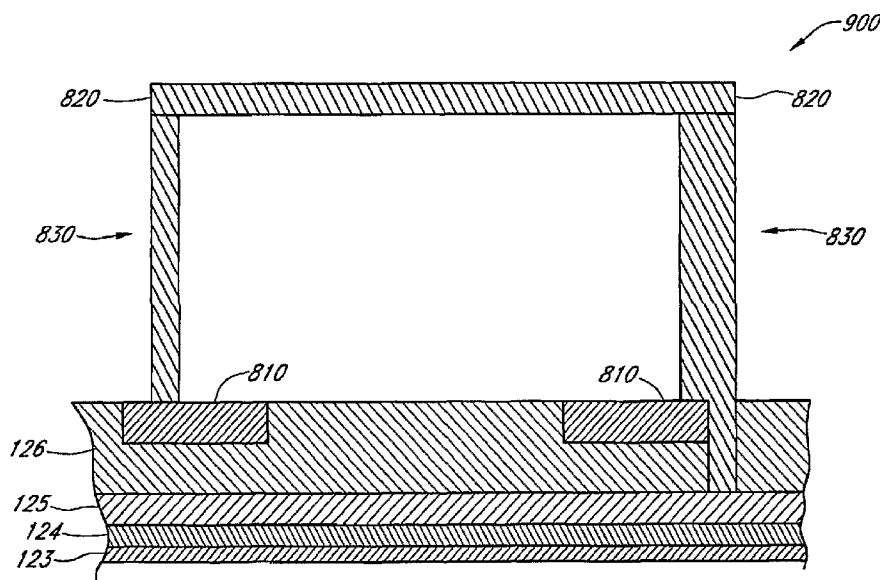
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(54) Title: SYSTEMS AND METHODS FOR FORMING ADDITIONAL METAL ROUTING IN SEMICONDUCTOR DEVICES



(57) Abstract: Memory devices, such as DRAM memory devices, may include one or more metal layers above a local interconnect of the DRAM memory that make contact to lower gate regions of the memory device. As the size of semiconductor components decreases and circuit densities increase, the density of the metal routing in these upper metal layers becomes increasingly difficult to fabricate. By providing additional metal routing in the lower gate regions that may be coupled to the upper metal layers, the spacing requirements of the upper metal layers may be eased, while maintaining the size of the semiconductor device. In addition, the additional metal routing formed in the gate regions of the memory devices may be disposed parallel to other metal contacts in a strapping configuration, thus reducing a resistance of the metal contacts, such as buried digit lines of a DRAM memory cell.

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