METHOD AND APPARATUS FOR BLOCKING LIGHT TO PERIPHERAL CIRCUITRY OF AN IMAGER DEVICE

FIELD OF THE INVENTION

[0001] The present invention relates generally to integrated circuits having imager devices formed thereon, and the methods of making said integrated circuits.

BACKGROUND OF THE INVENTION

[0002] Solid state imager dies, such as a CMOS imager die, typically contain thousands of pixel cells in a pixel cell array on a single chip. Pixel cells convert radiant energy into an electrical signal that can then be stored and recalled by an electrical device such as, for example, a processor. The electrical signals that are stored may be recalled to produce an image on, for example, a computer screen or a printable media.

[0003] Exemplary CMOS imaging circuits, processing steps thereof, and detailed descriptions of the functions of various CMOS elements of an imaging circuit are described, for example, in U.S. Patent Nos. 6,140,630; 6,376,868; 6,310,366; 6,326,652; 6,204,524; 6,333,205 each of which being assigned to Micron Technology, Inc. The disclosures of each of the forgoing patents are hereby incorporated by reference in their entirety.

[0004] FIG. 1 illustrates a block diagram of a conventional integrated circuit 10. The integrated circuit includes a die 12 having an imager device 8 included thereon; as illustrated and for exemplary discussions, the imager device is a CMOS device 8. The imager device 8 has a pixel cell array 14 that comprises a plurality of pixel cells arranged in a predetermined number of columns and rows. The pixel cells of each row in the pixel cell array 14 are all turned on at the same time by a row select line, and the pixel cells of each column are selectively output by respective column select lines. A plurality of row and column lines are provided for the entire pixel cell array 14. The row lines are selectively activated in sequence by a row driver 1 in response to row address decoder 2 and the column select lines are selectively activated in sequence for each row activation by a column driver 3 in response to column address decoder 4. The imager device 8 is operated by the control circuit 5, which controls address decoders 2, 4 for selecting the appropriate row and column lines for pixel cell readout, and row and column driver

circuitry 1, 3 to apply driving voltage to the drive transistors of the selected row and column lines.

[0005] The pixel cell output signals typically include a pixel reset signal V_{rst} taken from a charge storage node when it is reset and a pixel image signal V_{sig}, which is taken from the storage node after charges generated by an image are transferred to the node. The V_{rst} and V_{sig} signals are read by a sample and hold circuit 6 and are subtracted by a differential amplifier 7, which produces a difference signal ($V_{rst} - V_{sig}$) for each pixel cell, which represents the amount of radiant energy impinging on the pixel cell. The signal difference is digitized by an analog-to-digital converter 9. The digitized signal difference is then fed to an image processor 11 to form and output a digital image. In addition, as depicted in FIG. 1, the imager device 8 components may all be included on a single die 12 to form the integrated circuit 10 or the components may be integrated on a plurality of dies. The integrated circuit(s) 10 can be included in a number of image capture and/or reproduction applications, including, but not limited to, sensors, cameras, personal digital assistants (PDAs), scanners, facsimile machines, and copiers.

[0006] Radiant energy directed towards the pixel cell array 14 during image capture also strikes the peripheral circuitry of the imager device 8, which can interfere with proper image capture. For example, radiant energy could strike the circuitry, e.g., transistors and capacitors (not shown), of the row driver 1, decoders 2, 4, analog-to-digital converter 9, image processor 11, timing and control circuit 5, and/or the column driver 3. The peripheral circuitry typically comprises transistors, capacitors, and other components that are susceptible to noise when exposed to varying amounts of radiant energy. This can lead to image artifacts, such as column-banding, significantly degrading imager device performance.

[0007] Accordingly, there is a desire and need for a solid state imager device that has eliminated or reduced the amount of radiant energy striking the peripheral circuitry of the imager device, thereby decreasing the amount of noise in the image, and leading to better image quality.

BRIEF SUMMARY OF THE INVENTION

[0008] Exemplary embodiments of the present invention provide integrated circuits having solid state imager devices formed thereon, with a light blocking material layer formed over peripheral circuitry associated with the imager devices, to eliminate or reduce the amount of radiant energy

striking the peripheral circuitry. The present invention also relates to the methods of making such integrated circuits.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The above-described features and advantages of the invention will be more clearly understood from the following detailed description, which is provided with reference to the accompanying drawings in which:

[0010] FIG. 1 illustrates a block diagram of a conventional integrated circuit having an imager device;

[0011] FIG. 2 illustrates a block diagram of an integrated circuit constructed in accordance with an exemplary embodiment of the invention;

[0012] FIG. 3 illustrates a partial cross-sectional view of the FIG. 2 integrated circuit;

[0013] FIGS. 4-6 illustrate partial cross-sectional views of an exemplary method of fabricating the FIG. 2 integrated circuit;

[0014] FIG. 7 illustrates a partial cross-sectional view of an integrated circuit constructed in accordance with a second exemplary embodiment of the invention;

[0015] FIG. 8 illustrates a partial cross-sectional view of an integrated circuit constructed in accordance with a third exemplary embodiment of the invention;

[0016] FIG. 9 illustrates a block diagram of an integrated circuit constructed in accordance with a fourth exemplary embodiment of the invention;

[0017] FIG. 10 illustrates a block diagram of an integrated circuit constructed in accordance with a fifth exemplary embodiment of the invention;

[0018] FIG. 11 illustrates a partial cross-sectional view of an integrated circuit constructed in accordance with a sixth exemplary embodiment of the invention; and

[0019] FIG. 12 is a block diagram of a processor system incorporating the FIG. 2 integrated circuit in accordance with an exemplary embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0020] In the following detailed description, reference is made to the accompanying drawings, which form a part hereof and show by way of illustration specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized, and that structural, logical, and electrical changes may be made without departing from the spirit and scope of the present invention. The progression of processing steps described is exemplary of embodiments of the invention; however, the sequence of steps is not limited to that set forth herein and may be changed as is known in the art, with the exception of steps necessarily occurring in a certain order.

[0021] The terms "wafer," "die," and "substrate" are to be understood as a semiconductor-based material including silicon, silicon-on-insulator (SOI) or silicon-on-sapphire (SOS) technology, doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. Furthermore, when reference is made to a "wafer," "die," and "substrate" in the following description, previous process steps may have been utilized to form regions or junctions in or over the base semiconductor structure or foundation. In addition, the semiconductor need not be silicon-based, but could be based on silicon-germanium, silicon-on-insulator, silicon-on-sapphire, germanium, or gallium arsenide, or other semiconductor materials.

[0022] The term "pixel cell" refers to a picture element unit cell containing a photosensor and other devices for converting radiant energy into an electrical signal and providing pixel cell output. For purposes of illustration, portions of representative pixel cells are illustrated in the figures and description herein and, typically, fabrication of all imager pixel cells in an imager array will proceed simultaneously in a similar fashion. Although exemplary embodiments of the invention are discussed below in relation to a CMOS imager device, the invention is not so limited, and is applicable to any solid state imagers having an array of imaging pixel cells.

[0023] The term "opaque material" or "substantially opaque material" refers to any material layer capable of substantially blocking the passage of radiant energy and especially light.

[0024] Referring now to the figures, where like reference numbers designate like elements, FIG. 2 illustrates an embodiment of an integrated circuit 100 constructed in accordance with an embodiment of the invention. Specifically, FIG. 2 illustrates the integrated circuit 100 having a CMOS imager device 180 formed on a die 125. The imager device 180 includes a pixel cell array 145, and peripheral readout circuitry 122 that includes a row driver 110, column driver 130, row decoder 120, column decoder 140, timing and control circuit 150, analog-to-digital converter 190, sample and hold circuit 160, amplifier 170, and image processor 114.

[0025] Notably, the FIG. 2 integrated circuit 100 includes a substantially opaque material layer 124 formed over the peripheral circuitry 122. The material layer 124 is coupled to a first frame 116 that forms a perimeter around the peripheral circuitry 122 and a second frame 118 that forms a perimeter around the pixel cell array 145. The illustrated first and second frames 116, 118 are formed such that the second frame 118 is formed within a perimeter of the first frame 116. The material layer 124 protects the peripheral circuitry 122 from impinging radiant energy, while allowing radiant energy to strike the pixel cell array 145. The material layer 124 may reduce noise during pixel cell readout by protecting the transistors and capacitors (not shown) of the various components of the peripheral circuitry 122 from radiant energy. The material layer 124 could be formed of any substantially opaque material, including, but not limited to, a negative photoresist.

[0026] FIG. 3 illustrates a partial cross sectional view of the FIG. 2 integrated circuit 100. As illustrated, the integrated circuit 100 has a substantially opaque material layer 124 formed over the peripheral circuitry 122 that prevents radiant energy from striking the peripheral circuitry 122, resulting in the reduction of noise during the readout process and the elimination or reduction of image artifacts such as column banding. FIG. 3 also illustrates a partial cross sectional view of the pixel cell array 145 having an array of microlenses 141, which direct radiant energy onto respective photoreactive areas 147 formed in an epitaxial layer 121 on the die 125. The illustrated microlenses 141 are formed over a planarization layer 191, which is

formed over a color filter array 117 and other conventional dielectric and electrode material layers 120a, 120b, 120c, 120d.

[0027] Color filter arrays (e.g., color filter array 117) are typically used in pixel cell arrays (e.g., pixel cell array 145) to allow radiant energy within a particular wavelength range, which corresponds to a particular color, to reach the pixel cells. For example, color filter arrays include filters that allow wavelengths of light associated with the colors red, blue, or green (RBG) to create corresponding red, blue, or green pixel cells. Yet other color filter arrays allow wavelengths of light associated with the colors, cyan, magenta, and yellow (CMY) to create corresponding cyan, magenta, and yellow pixel cells.

[0028] The FIG. 3 material layer 124 is coupled to first and second frames 116, 118, which are formed as mesas over the planarization layer 191. The illustrated material layer 124 is formed only over the peripheral circuitry 122, thereby allowing radiant energy to strike the microlenses 141. Although illustrated as being formed on the same material layer (i.e., planarization layer 191) as the microlens array 141, the material layer 124 and first and second frames 116, 118 are not limited to the illustrated embodiment, and could be formed on other material layers of the integrated circuit 100, as is further discussed below with respect to FIGS. 6-8.

[0029] FIGS. 4-6 illustrate an exemplary method of fabricating the FIG. 2 integrated circuit 100. As illustrated in FIG. 4 an intermediate structure 100a includes the die 125 having an epitaxial layer 121 formed thereon. Photoreactive areas 147 and peripheral circuitry 122 are formed in association with the epitaxial layer 121. The planarization layer 191 is formed over the color filter array 117 and other material layers 120a, 120b, 120c, 120d, which are formed over the epitaxial layer 121. Although the photoreactive areas 147 and peripheral circuitry 122 are illustrated as being formed within and over the epitaxial layer 121, respectively, this is only exemplary and not intended to be limiting in any way.

[0030] Precursor blocks 141a are patterned over the planarization layer 191. The precursor blocks 141a could be any material of sufficient thickness suitable for direct lithographic patterning (e.g., generally photoresist or specifically the material typically used in the formation of microlenses (e.g., microlens array 141 of FIG. 3). For example, the precursor blocks 141a

could be formed of materials selected from the group consisting of polymethylmethacrylate, polycarbonate, polyolefin, cellulose acetate butyrate, or polystyrene; a polyimide; a thermoset resin such as an epoxy resin; a photosensitive gelatin; or a radiation curable resin such as acrylate, methacrylate, urethane acrylate, epoxy acrylate, or polyester acrylate.

[0031] The precursor blocks 141a that are patterned to form the first and second frames 116, 118 (e.g., FIG. 2), can be selectively treated with UV light such they are less susceptible to subsequent reflow processes, as discussed below with respect to FIG. 5. The precursor blocks 141a that are patterned over the photoreactive areas 147 are selectively protected by a mask 155 from the UV light.

[0032] FIG. 5 illustrates the precursor blocks 141a (FIG. 4) that were patterned over the photoreactive areas 147, and not treated with UV light are reflowed to form an array of microlenses 141. A negative photoresist layer 124a is formed over the intermediate structure 100a. A mask 155 is provided over selected portions of the material layer 124a (e.g., over the pixel cell array 145) over which the material layer 124 (FIG. 3) is not desired. UV light is directed upon the negative photoresist such that the negative photoresist exposed to light cross links, and becomes insoluble to a developer.

[0033] FIG. 6 illustrates the removal of the mask, and subsequent exposure of the intermediate structure 100a (FIG. 5) to a developer (not shown). The developer attacks the portions of the photoresist 124a (FIG. 5) that were not exposed to UV light (i.e., not cross linked), while the portion of the photoresist 124a (FIG. 5) that was previously properly cross linked remains as material layer 124.

[0034] Creating the first and second frames 116, 118 allows for a thinner portion 124p of the material layer 124 to be formed in these areas; the thinner portion 124p of the material layer 124 requires less exposure to UV light for proper cross linking than a middle portion 124m that is located between the first and second frames 116, 118. For example, the thinner portions 124p of the material layer 124 may have a thickness of about 0.5 μm and the middle portion 124m of the material layer 124 may have a thickness of about 1 μm or more. During the treatment of the photoresist 124a (FIG. 5), the thinner portions 124p may require an exposure of about 200 mJ to

properly cross link the photoresist 124a (FIG. 5). On the other hand, the middle portion 124m may require an exposure of about 1600 mJ for proper cross linking. An exposure of 1600 mJ would significantly reduce the production throughput of the exposure tool, and increase the device cost. It can also lead to material outgassing and exposure tool damage. Finally, a high exposure like this could lead to an increased level of stray light and cause photoresist residue issues in the active array area which can negatively impact the performance of the imager.

[0035] In addition, the first and second frames 116, 118 prevent developer from attacking the middle portion 124m of the photoresist 124a (FIG. 5). Any photoresist 124a (FIG. 5) that is not properly cross linked would likely be localized in the middle portion 124m due to the possibility that the UV light may not penetrate the top surface 124s of the photoresist 124a (FIG. 5) deep enough to reach the middle portion 124m. Therefore, the first and second frames 116, 118 act as barriers to subsequent processes using a developer. As long as the top surface of the material layer 124 and the thinner portions 124p of the material layer 124 over the first and second frames 116, 118 are exposed to sufficient UV dosages to sufficiently cross link, a high quality material layer 124 can be formed to block light from striking the peripheral circuitry 122.

[0036] Although the FIG. 6 material layer 124 is described as having a thickness of 0.5 μm at thinner portions 124p of the material layer 124 and 1 μm at a middle portion 124m of the material layer 124, it is not intended to be limiting in any way. For example, the thinner portions 124p could be greater than or less than 0.5 μm, and the middle portion 124m could similarly be greater than or less than 1 μm, depending upon the application. Similarly the exposure dose of the photoresist 124a (FIG. 5) to UV light could be greater than or less than 200 mJ, depending upon the desired thickness of the material layer 124 and its exposure sensitivity.

[0037] It should be noted that although the first and second frames 116, 118 are illustrated as having a substantially rectangular shape in the cross-sectional illustration, it is not intended to be limiting. For example, the first and second frames could have a substantially semi-elliptical, substantially semi-circular, or substantially trapezoidal shape (if desired), depending on the area of the pixel cell array 145 and that of the peripheral circuitry 122.

[0038] It should also be noted that the treatment of the precursor blocks 141a with UV, as discussed above with respect to FIG. 4, is optional, and not intended to be limiting. For example, the precursor blocks 141a (FIG. 4) that are patterned to create the first and second frames 116, 118 (FIG. 6) could be reflowed along with the precursor blocks 141a (FIG. 4) patterned to form the array of microlenses 141 (FIG. 6), such that the first and second frames 116, 118 (FIG. 6) are formed to have a semi-circular shape (e.g., Fig. 11).

[0039] It should further be noted that the first and second frames 116, 118 need not be formed of the same material as the array of microlenses 141. For example, the first and second frames 116, 118 could be formed of a positive or negative resist material, or any other material.

[0040] FIG. 7 illustrates a partial cross-sectional view of an integrated circuit 200 constructed in accordance with a second embodiment of the invention in which first and second frames 216, 218 are formed as mesas of a color filter array 217. The first and second frames 216, 218 are formed by providing a color filter array precursor layer, and forming trenches in the precursor layer, thereby creating corresponding mesas that form the first and second frames 216, 218. The planarization layer 191 is selectively formed over the color filter array 217 such that the planarization layer 191 is formed within the trenches formed in the color filter array precursor layer (i.e., not over the mesas that form the first and second frames 216, 218). A microlens array 141 is formed over the planarization layer 191. The material layer 124 is formed over the first and second frames 216, 218, and in between the first and second frame 116, 118, in a substantially similar fashion as discussed above with respect to FIGS. 5 and 6.

[0041] FIG. 8 illustrates a partial cross-sectional view of an integrated circuit 300 constructed in accordance with a third embodiment of the invention in which first and second frames 316, 318 are formed as mesas of a planarization layer 391. The first and second frames 316, 318 could be formed by forming a planarization precursor layer, and etching trenches within the planarization precursor layer, thereby creating corresponding mesas that form the first and second frames 316, 318. FIG. 8 illustrates a color filter array 317 formed beneath the planarization layer 391. A microlens array 141 is subsequently formed over the planarization layer 391. The material layer 124 is formed in a substantially similar fashion as discussed above with respect to FIGS. 5 and 6.

[0042] It should be noted that although FIGS. 6-8 illustrate first and second frames 116, 118 (FIG. 6), 216, 218 (FIG. 7), 316, 318 (FIG. 8) formed as mesas of microlens material, color filter array material, and planarization layer material, respectively, any other material layer of the integrated circuits (100, 200, 300 of FIGS. 6-8) could be used to form the first and second frames. For example, as illustrated in FIG. 8, the planarization layer 391 is formed over various material layers 320a, 320b, 320c, 320d. Any of the various material layers 320a, 320b, 320c, 320d, which are typically inter-layer dielectric materials, could be formed with mesas to form first and second frames (e.g., first and second frames 316, 318) as long as subsequent processing does not planarized the mesa structures.

[0043] FIG. 9 illustrates an integrated circuit 400 constructed in accordance with a fourth exemplary embodiment of the invention. The integrated circuit 400 has an imager device 480 formed on a die 425. Like the FIG. 2 imager device 180 (FIG. 2), the FIG. 9 imager device 480 includes a pixel cell array 445, and peripheral readout circuitry 422 comprising a row driver 410, column driver 430, row decoder 420, column decoder 440, timing and control circuit 450, analog-to-digital converter 490, sample and hold circuit 460, differential amplifier 470, and an image processor 414. Unlike the FIG. 2 embodiment, however, the FIG. 9 integrated circuit 400 has a single frame 416 forming a perimeter around the peripheral circuitry 422. The single frame 416 is a continuous frame that forms a perimeter around the peripheral circuitry within which a material layer 424 is subsequently formed, as illustrated in FIG. 9. The material layer 424 is coupled to the single frame 416 in a substantially similar manner as described above with respect to FIGS. 5 and 6.

[0044] The FIG. 9 integrated circuit 400 is constructed in a substantially similar fashion as the FIG. 2 integrated circuit 100. The FIG. 9 integrated circuit 400 could have a single frame 416 that is formed of a material layer, such as the planarization precursor layer, color filter array precursor layer, or microlens array precursor layer, used in the fabrication of the integrated circuit.

[0045] FIG. 10 illustrates an integrated circuit 500 constructed in accordance with a fifth embodiment of the invention. The integrated circuit 500 includes an imager device 580 formed on a die 525. The imager device 580 includes components that comprise peripheral circuitry

522. Each component of the peripheral circuitry 522 has a respective frame forming a perimeter around the component. The FIG. 10 integrated circuit 500 includes a row driver 510, column driver 530, row decoder 520, column decoder 540, timing and control circuit 550, analog-to-digital converter 590, sample and hold circuit 560, differential amplifier 570, and an image processor 514. Accordingly, the integrated circuit 500 includes a row driver frame 511, column driver frame 531, row decoder frame 521, column decoder frame 541, timing and control circuit frame 551, analog to digital converter frame 591, sample and hold circuit frame 561, amplifier frame 571, and an image processor frame 581. A material layer 524 is formed over each component of the peripheral circuitry 522, and coupled to a respective frame, as discussed above with respect to FIGS. 5 and 6.

[0046] FIG. 11 illustrates an integrated circuit 600 constructed in accordance with a sixth embodiment of the invention. The illustrated integrated circuit 600 has a first frame 616 having first and second portions 616a, 616b and a second frame 618 having first and second portions 618a, 618b formed over a planarization layer 691, which is formed over a die 625. A material layer 624 is formed over and coupled to the first and second frames 616, 618 in a substantially similar fashion as the FIG. 6 integrated circuit 100. The material layer 624 may be secured at four separate points by dividing each of the first and second frames 616, 618 into two portions 616a, 616b and 618a, 618b, respectively, thereby providing greater durability to the overall integrated circuit 600.

[0047] Although illustrated as having a semi-spherical cross-sectional shape, the first and second portions 616a, 616b and 618a, 618b of the first and second frames 616, 618, respectively, are not so limited. For example, as discussed above with respect to FIG. 6, the first and second frames 616, 618 could be formed to have first and second portions 616a, 616b and 618a, 618b, respectively, that have a substantially semi-elliptical, substantially semi-circular, or substantially trapezoidal shape. Similarly, any of the material layers 620a, 620b, 620c, 620d could comprise the first and second frames 616, 618, each having first and second portions 616a, 616b and 618a, 618b, respectively.

[0048] FIG. 12 is a block diagram of a system 900 having an integrated circuit in accordance with one of the embodiments (e.g., integrated circuits 100, 200, 300, 400, 500, 600 of FIGS. 2,

7, 8, 9, 10, 11) of the invention. Without being limiting, such a system 900 could include a computer system, camera system, scanner, machine vision, vehicle navigation, video phone, surveillance system, auto focus system, star tracker system, motion detection system, image stabilization system, and other systems employing an integrated circuit having an imager device (e.g., imager device 180, 480, 580 of FIGS. 2, 9, 10). For the sake of clarity, FIG. 12 is further discussed as incorporating the integrated circuit 100 of FIG. 2. It should be noted, however, that any of the integrated circuits discussed with respect to FIGS. 2, 7, 8, 9, 10 and 11 (i.e., integrated circuits 200, 300, 400, 500, 600) could be incorporated into the FIG. 12 system 900, and that the description is not intended to be limiting in any way.

[0049] System 900, for example a camera system, generally comprises a central processing unit (CPU) 902, such as a microprocessor, that communicates with an input/output (I/O) device 906 over a bus 904. Integrated circuit 100 also communicates with the CPU 902 over the bus 904. The processor-based system 900 also includes random access memory (RAM) 910, and can include removable memory 914, such as flash memory, which also communicate with the CPU 902 over the bus 904. The integrated circuit 100 may be combined with a processor, such as a CPU, digital signal processor, or microprocessor, with or without memory storage on a single integrated circuit or on a different chip than the processor.

[0050] The above description and drawings illustrate preferred embodiments which achieve the objects, features, and advantages of the invention. Although certain advantages and preferred embodiments have been described above, those skilled in the art will recognize that substitutions, additions, deletions, modifications and/or other changes may be made without departing from the spirit or scope of the invention. Accordingly, the invention is not limited by the foregoing description but is only limited by the scope of the appended claims.

CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. An integrated circuit, comprising:

a die;

a pixel cell array formed in association with said die;

peripheral circuitry formed in association with said die and electrically connected to said pixel cell array;

a first frame forming a perimeter around said peripheral circuitry; and

a substantially opaque material layer over said circuitry, said material layer being coupled to said frame.

2. The integrated circuit of claim 1, further comprising a second frame forming a perimeter around said pixel array, wherein said substantially opaque material layer is coupled to said second frame.

3. The integrated circuit of claim 2, wherein at least one of said first and second frames is formed as a mesa of a material layer included within said integrated circuit.

4. The integrated circuit of claim 3, wherein said material layer is a planarization layer.

5. The integrated circuit of claim 2, wherein said first frame forms a perimeter around said second frame.

6. The integrated circuit of claim 5, wherein said substantially opaque material layer over said circuitry is coupled to said first and second frames, and localized to an area between said first and second frames.

7. The integrated circuit of claim 1, wherein said substantially opaque material layer comprises a negative photoresist.

8. The integrated circuit of claim 1, wherein said pixel cell array further comprises an array of microlenses, and said first frame and said array of microlenses are comprised of the same material.

9. The integrated circuit of claim 1, wherein said first frame and said array of microlenses are formed on the same level of a material layer.

10. The integrated circuit of claim 1, wherein said pixel cell array further comprises a color filter array, and said first frame and said color filter array are comprised of the same material.

11. The integrated circuit of claim 1, wherein said first frame and said color filter array are formed on the same level of a material layer.

12. The integrated circuit of claim 1, further comprising a planarization layer, said first frame and said planarization layer are comprised of the same material.

13. The integrated circuit of claim 1, wherein said first frame and said planarization layer are formed on the same level of a material layer.

14. An imager processor system, comprising:

a processor; and

an integrated circuit, comprising;

a die;

a pixel cell array formed in association with said die;

circuitry formed in association with said die and electrically connected to said pixel cell array;

a first frame forming a perimeter around said circuitry; and

a substantially opaque material layer over said circuitry, said material layer being coupled to said frame.

15. The processor system of claim 14, further comprising a second frame forming a perimeter around said pixel array, wherein said substantially opaque material layer is further coupled to said second frame.

16. The processor system of claim 15, wherein said first frame forms a perimeter around said second frame.

17. The processor system of claim 14, wherein said substantially opaque material layer over said circuitry is coupled to said first and second frames, and localized to an area between said first and second frames.

18. The processor system of claim 14, wherein said substantially opaque material layer comprises a negative photoresist.

19. The processor system of claim 14, wherein said first frame is formed as a mesa of a material layer included within said integrated circuit.

20. A method of fabricating an integrated circuit, comprising:

providing a die;

forming a pixel cell array in association with said die;

forming circuitry in association with said die and electrically connected to said pixel cell array;

forming a first frame such that said first frame forms a perimeter around said circuitry;

forming a substantially opaque material layer over said circuitry; and

coupling said substantially opaque material layer to said frame.

21. The method of claim 20, further comprising the step of forming a second frame such that said second frame a perimeter around said pixel array.

22. The method of claim 21, wherein said second frame is formed such that said first frame forms a perimeter around said second frame.

23. The method of claim 21, further comprising the step of coupling said substantially opaque material layer to said second frame.

24. The method of claim 23, wherein said substantially opaque material layer is formed as being limited to an area between said first and second frames.

25. The method of claim 20, wherein said first frame is formed by the steps of:

patterning precursor blocks; and

treating said precursor blocks with radiation.

26. The method of claim 20, wherein said substantially opaque material layer is coupled to said first frame by the steps of:

forming a material layer precursor over said die;

selectively treating said material layer precursor with radiation, thereby cross linking said treated material layer precursor; and

exposing said material layer precursor to developer.