

ABSTRACT

The present disclosure relates to a memory device and the operating method thereof. A memory device comprising: a memory cell array, and a controller configured
5 to connect, in a first interval equal to or longer than a bit line setup interval, each of first and second bit lines, which are connected to cells respectively having first and second program states, to a node of a first permission voltage, connect, in the first interval, a third
bit line, which is connected to a cell having a program prohibition state, to a node of a prohibition voltage, maintain, in a second interval that is equal to or shorter than a program
10 pulse application interval, the respective connections of the first bit line and the third bit line, and disconnect, in the second interval, the second bit line from the node of the first permission voltage to apply the second bit line with a second permission voltage.

FIG. 1