# SENSING SCHEMES FOR FLASH MEMORY WITH MULTILEVEL CELLS

## FIELD OF THE INVENTION

The present invention relates generally to determining the state of a semiconductor memory cell and specifically to sensing the state of a flash memory cell that stores more than a single bit of data.

## BACKGROUND OF THE INVENTION

Nonvolatile semiconductor memory devices are fundamental building blocks in prior art computer system designs. The primary mechanism by which data is stored in nonvolatile memory is the memory cell. Typical prior memory technologies provide a maximum storage capacity of one bit, or two states, per cell. Semiconductor memory cells having more than two possible states are known in the prior art, and specific references are cited at the close of the Background of the Invention.

One type of prior nonvolatile semiconductor memory is the flash electrically-erasable programmable read-only memory ("flash EEPROM"). Prior art flash EEPROMs typically allow for the simultaneous reading of several flash cells. Further, typical prior flash EEPROMs have a storage capacity that is much greater than the amount of data that can be output at any one time. Accordingly, each output of a flash EEPROM is typically associated with an array of flash cells that is arranged into rows and columns, where each flash cell in an array is uniquely addressable. When a user provides an address, row and column decoding logic in the flash EEPROM selects the corresponding flash cell.

A typical prior flash memory cell is comprised of a single field effect transistor ("FET") including a select gate, a floating gate, a source, and a drain. Information is stored in the flash cell by altering the amount of charge on the floating gate, which causes the threshold voltage $V_t$ of the flash cell to be varied. The typical prior art flash memory cell is in

one of two possible states, being either "programmed" or "erased." Figure 1 illustrates flash cell distribution as a function of $V_t$ for a prior art flash device. As can be seen, the erased state and the programmed state each specify a range of $V_t$ voltages. The flash cell can theoretically possess a separate identifiable state for each electron that is added to the floating gate. Practically speaking, however, prior flash cells typically have only two possible states because of inconsistencies in flash cell structure, charge loss over time, thermal considerations and inaccuracies in sensing the charge on the floating gate that affect the ability to determine the data stored in the flash cell.

To distinguish between the two possible states, the states are separated by a separation range. According to one prior method, when a flash cell is read, the current conducted by the flash cell is compared to a current conducted by reference flash cell having a threshold voltage $V_t$ set to a predetermined reference voltage that is a voltage in the separation range. A single comparator typically makes the comparison and outputs the result.

When a flash cell is selected for reading, a biasing voltage is applied to the select gate. Simultaneously, the same biasing voltage is applied to the select gate of the reference cell. If the flash cell is programmed, excess electrons are trapped on the floating gate, and the threshold voltage $V_t$ of flash cell has increased such that the selected flash cell conducts less drain current than the reference flash cell. The programmed state of the prior flash cell is typically indicated by a logic 0. If the prior flash cell is erased, little or no excess electrons are on the floating gate, and the flash cell conducts more drain-source current than the reference cell. The erased state of the prior flash cell is typically indicated by a logic 1.

When a flash cell has three or more possible states, the prior art sensing schemes and circuits similar to that described above are inadequate. First, as a general rule, there must be at least (n-1) references

for n states. This can be implemented as (n-1) reference cells. Thus, for three states, there must be two references. Typical prior art sensing schemes discriminate between two states and provide only one voltage reference. Second, the use of a single comparator in typical prior sensing schemes, without more, is not adequate to retrieve data from a multi-level flash cell.

U.S. Patent No. 4,415,992 describes a sensing scheme for sensing the state of a memory cell capable of storing n states in which (n-1) comparators and (n-1) voltage references are used in parallel to determine the state of the memory cell. Each comparator compares a corresponding one of the (n-1) voltage references to a voltage determined by the drain-source current of the memory cell. Decoding logic is required to translate the outputs of the (n-1) comparators into ($\log_2 n$) binary bits.

U.S. Patent No. 5, 163,021 describes a sensing scheme in which n comparators are sequentially used to compare the state of a memory cell capable of storing n states to a corresponding n references. Again, decoding logic is required to translate the outputs of the (n-1) comparators into ($\log_2 n$) binary bits.

SUMMARY AND OBJECTS OF THE INVENTION

Therefore, one object of the present invention is to provide a method for determining the state of a memory cell having more than two possible states.

Another object of the present invention is to provide a circuit for determining the state of a memory cell having n possible states, wherein the circuit uses one comparator per bit stored in the memory cell.

A sensing circuit for determining a state of a memory cell having n possible states, where n is greater than 2, is described. The sensing circuit includes a first reference corresponding to a first threshold voltage level and a first comparator coupled to the memory cell and to the first reference. The first comparator compares a threshold voltage level of the memory cell to the first reference. The first comparator outputs a first result of the comparison. The sensing circuit further includes a second reference corresponding to a second threshold voltage level and a third reference corresponding to a third voltage level. A second comparator has one of its inputs coupled to the memory cell and its second input is selectively coupled to either the second reference or the third reference. A selector circuit selects between the second and third references in response to the first result. The selector circuit couples the second reference to the second comparator if the threshold voltage level of the memory cell is less than the first threshold voltage level. The selector circuit couples the third reference to the second comparator if the threshold voltage level of the memory cell is greater than the first voltage level.

The above-mentioned objects and other objects of the invention are also provided for by sensing circuit that includes a single comparator. A selector circuit selects between n-1 voltage references. At least two data latches are provided for storing and outputting the result of comparisons made between the cell voltage level and the voltage levels of selected voltage references.

Other objects, features, and advantages of the present invention will be apparent from the accompanying drawings and from the detailed description which follows below.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the figures of the accompanying drawings, in which like references indicate similar elements, and in which:

**FIGURE 1** illustrates flash cell distribution as a function of $V_T$ for a prior art flash device.

**FIGURE 2** is a block diagram of a computer system according to one embodiment

**FIGURE 3** illustrates a distribution of multi-level flash cells as a function of $V_T$ wherein each flash cell has four possible states.

**FIGURE 4A** shows a flow chart for performing a binary search of reference cells for a flash cell having four possible states.

**FIGURE 4B** is a more conventional flow chart of the binary search method

**FIGURE 5** illustrates a sensing circuit using two comparators for sensing the state of a flash cell having four possible states.

**FIGURE 6** illustrates a distribution of multi-level flash cells as a function of $V_T$ wherein each flash cell has eight possible states.

**FIGURE 7** shows a flow chart for performing a binary search of reference cells for a flash cell having eight possible states.

**FIGURE 8** shows a sensing circuit utilizing a single comparator to determine the state of a flash cell having four possible states.

DETAILED DESCRIPTION

Illustrative embodiments of the present invention relate to determining the state of a semiconductor memory cell having n possible states, wherein n is greater than two. According to one embodiment, a comparator is provided for every two states stored in the memory cell. In a second embodiment, a single comparator is used. Both embodiments implement a binary search method for selecting which of the (n-1) references are compared to the state of the memory cell.

**Figure 2** shows a computer system of one embodiment. The computer system generally includes a bus 11, to which may be coupled a processor 12, main memory 14, static memory 16, mass storage device 17, and integrated circuit controller 18. Static memory 16 may include a flash electrically eraseable programmable read only memory ("flash EEPROM") or other nonvolatile memory device that stores multiple bits of data per cell. Similarly, mass storage device 17 may be a solid state hard drive 17 using multiple bit per cell nonvolatile memory devices for storing data.

Integrated circuit cards 19 and 20 may be included in the computer system and are coupled to a Personal Computer Memory Card Industry (PCMCIA) bus 26. PCMCIA bus 26 is coupled to bus 11 and to integrated circuit (IC) controller 18 for providing communication information between cards 19 and 20 and the remainder of the computer system. IC controller 18 provides control and address information to IC cards 19 and 20 via PCMCIA bus 26 and is coupled to bus 11.

The computer system may further include a display device 21, a keyboard 22, a cursor control device 23, a hard copy device, and a sound sampling device 25. The specific components and configuration of the computer system is determined by the particular applications for which the computer system is to be used. For example, the computer system of **Figure 2** may be a personal digital assistant (PDA), a pen-based computer system, a mainframe computer, or a personal computer.

For each embodiment, each memory cell is a flash cell. Each flash cell in the array is capable of being in one of four analog states, and the state of the flash cell is indicated by two binary bits. Figure 3 shows a distribution of multi-level flash cells as a function of threshold voltage $V_t$. As can be seen, each state is separated by a separation range, and three references, $Ref_1$, $Ref_2$ and $Ref_3$, are provided, one each from the three separation ranges. The references are provided to distinguish between the analog states. State 1 encompasses the lowest range of $V_t$ voltages of the four states and is indicated by both bits being logic 1's (both erased). State 2 is indicated when the high order bit (Bit 1) is a logic 1 and the lower order bit (Bit 0) is a logic 0. State 3 is indicated by Bit 1 being a logic 0 and Bit 0 being a logic 1. State 4 is indicated by both bits being logic 0's (both programmed). The number n of possible states is not limited to four. For example, the number of states can be three, five, sixteen, etc. Further, the mapping of binary bits to analog states may be varied. For example, the lowest range of $V_t$ voltages can be indicated by both bits being logic 0's.

It should be noted that nonvolatile memory devices other than flash EEPROM's and volatile memory devices such as Dynamic Random Access Memories (DRAM) are capable of storing three or more analog states. Further, it should be noted that the analog states of nonvolatile devices having a floating gate may be expressed in terms other than the threshold voltage $V_t$. For example, analog states may be expressed as ranges of threshold voltages $V_t$ as shown in Figure 3, as ranges of drain currents $I_D$, or as ranges of charge stored on the floating gate. Volatile memory cells such as DRAM memory cells are typically comprised of a capacitor and may similarly be expressed as ranges of charge, currents or voltages.

A nonvolatile memory cell that has a floating gate behaves as a field effect transistor having a threshold voltage $V_t$ that increases as charge is added to the floating gate. The memory cell drain current $I_D$

("cell current") decreases as the threshold voltage Vt and cell charge level increase. The memory cell threshold voltage $V_t$ is related to the memory cell drain current $I_D$ by the expression:

$I_D \alpha G_m \times (V_G - V_t)$ for $V_D > V_G - V_t$

$G_m$ is the transconductance of the memory cell;

$V_G$ is the memory cell gate voltage;

$V_D$ is the memory cell drain voltage; and

$V_t$ is the memory cell threshold voltage.

Given this relationship, there are a number of different ways to sense the amount of charge stored on of the floating gate of the memory cell including: sensing the cell current of a memory cell when a constant voltage is applied to the select gate of the memory cell; sensing the amount of voltage required at the select gate to give rise to an expected cell current for the memory cell; sensing a voltage drop across a load that is coupled to the drain of the memory cell when a constant voltage is applied to the select gate of the memory cell, wherein the cell current determines the amount of the voltage drop across the load; and sensing the amount of voltage required at the select gate to give rise to an expected voltage drop across a load that is coupled to the drain of the memory cell. To determine the analog state of the memory cell, however, it is not necessary to quantify the precise amount of charge stored on the floating gate. It is sufficient to compare a characteristic of the memory cell to a known reference.

One type of reference is a reference memory cell programmed to have a known threshold voltage $V_t$ that is typically between defined states. Sensing circuitry for the memory cell may be replicated for the reference memory cell and the outputs of the sensing circuitry and reference sensing circuitry may be compared using a differential comparator. Because sensing the cell charge level of a memory cell typically requires the comparison of either voltages or currents, the reference may be provided by using voltage supplies or current sources to

supply voltages or currents that correspond to reference memory cells having a cell charge level between defined analog states. For this reason, the references $Ref_1$, $Ref_2$, and $Ref_3$ are not specified as being threshold voltages, cell currents, or levels of charge stored on a floating gate. Instead, it is to be understood that the references shown in **Figure 3** correspond to the characteristics of the memory cell as defined by the relationship between cell charge level, cell current $I_D$, and threshold voltage $V_t$. For the purposes of simplifying the remaining discussion, the references $Ref_1$, $Ref_2$, and $Ref_3$ will expressed as threshold voltages $V_{R1}$, $V_{R2}$ and $V_{R3}$, respectively.

**Figure 4A** is a block diagram showing a binary search method for determining the state of a memory cell having more than two possible states. In step 301, the cell charge level of the selected cell is sensed and compared to a first reference flash cell having its $V_t$ equal to $V_{R2}$. Depending on the result of the initial comparison, the sensed cell charge level of the selected cell is compared to a selected one of a second reference flash cell having its $V_t$ equal to $V_{R1}$ and a third reference flash cell having its $V_t$ equal to $V_{R3}$. If the sensed cell charge level of the selected flash is less than that of the first reference flash cell, the sensed cell charge level is compared to the second reference flash cell at step 2, and the selected flash cell is either in state 1 or state 302. If the sensed cell charge level of the selected flash is greater than that of the first reference flash cell, the sensed cell charge level is compared to the third reference flash cell at step 303, and the selected flash cell is either in state 3 or state 4. Sensing of the cell charge level may be done according to any of the methods previously discussed.

**Figure 4B** is a conventional flow chart showing the binary search method of the present embodiment. At step 311, the cell charge level of the memory cell is sensed. At step 312, it is determined whether the cell charge of the memory cell is less than the cell charge level of the reference $Ref_2$. If the cell charge level of the memory cell is less than the

cell charge level of the reference $Ref_2$, the threshold voltage $V_t$ of the memory cell is less than that of a reference memory cell having a $V_t$ equal to $V_{R2}$. Similarly, the cell current $I_D$ of the memory cell is greater than the cell current $I_{R2}$ of a reference memory cell having a cell current of $I_{R2}$. If the cell charge level of the memory cell is less than the cell charge level of reference $Ref_2$, $Ref_1$ is selected at step 313. At step 314, it is determined whether the cell charge of the memory cell is less than the cell charge level of the reference $Ref_1$. If the cell charge level of the memory cell is less than the cell charge level of the reference $Ref_1$, the memory cell is indicated as being in state 1 at step 315. If the cell charge level of the memory cell is greater than the cell charge level of the reference $Ref_1$, the memory cell is indicated as being in state 2 at step 316.

If the cell charge level of the memory cell is less than the cell charge level of reference $Ref_2$, $Ref_3$ is selected at step 317. At step 318, it is determined whether the cell charge of the memory cell is less than the cell charge level of the reference $Ref_3$. If the cell charge level of the memory cell is less than the cell charge level of the reference $Ref_3$, the memory cell is indicated as being in state 3 at step 319. If the cell charge level of the memory cell is greater than the cell charge level of the reference $Ref_3$, the memory cell is indicated as being in state 4 at step 320.

**Figure 5** shows a sensing circuit for determining the state of a memory cell having more than two possible states. This circuit implements the method of **Figures 4A-4B**. The circuit uses a constant-gate-voltage/variable-cell-current sensing scheme wherein a constant biasing voltage $V_S$ is applied to the select gates of a selected flash cell 401 and reference flash cells 486, 487 and 488. The state of the selected flash cell 401, as a function of the level of charge on floating gate 142 of the flash cell 141, is determined by comparing the cell current of the selected flash cell 401 to the reference cell currents of a reference flash cell 486 and a selected one of the reference flash cells 487 and 488. To sense the respective cell currents, a load is coupled to the drains of the respective

flash cells to give rise to a voltage drop. In this manner, the cell charge level of the selected flash cell is sensed and used to determine the analog state of the selected flash cell.

The multi-level flash cell 401 of the present embodiment includes a select gate, a floating gate 402, a drain and a source. The selected flash cell 401 is one of an array 410 of such multi-level flash cells arranged in a matrix of rows and columns. The selected flash cell 401 is selected when column decoder 420 and row decoder 430 select the selected flash cell 401 in response to a user-provided address. When the selected flash cell 401 is selected, a biasing voltage $V_S$ is applied to the select gate of flash cell 401 and the drain of flash cell 401 is coupled to the drain bias circuit 440 via column decoder 420. It will be understood that several flash cells of the array 410 can be concurrently selected in a similar manner such that multiple bits of data may be read simultaneously. Accordingly, each selected cell would be coupled to sensing circuitry similar to that shown in **Figure 5**.

The cell charge level on the floating gate 402 of the selected flash cell 401 determines the amount of cell current that flows through selected flash cell 401 when the biasing voltage $V_S$ is applied to the select gate of selected flash cell 401 by defining the cell threshold voltage $V_t$. When the selected flash cell 401 is conducting current, a corresponding current is produced across the column load 445, resulting in a voltage drop from VCC to the node 450. The voltage at node 450 is sensed by the differential comparators 460 and 470 used to determine the state of the flash cell 401.

In **Figure 5**, the column load 445 is shown as an n-channel FET 446 coupled as a resistor having its source coupled to node 450, its drain coupled to VCC and its gate coupled to a constant voltage $V_{CL}$. The constant voltage $V_{CL}$ is preferably such that the FET 446 operates in the saturated region. Alternatively, the column load may be a resistor. A drain bias circuit 440 is also coupled between the array 410 and node 450. The function of the drain bias circuit 440 is to isolate the column load 445

from the drain of the selected flash cell 401 while biasing the drain of the selected flash cell 401. The drain bias circuit includes an n-channel FET 441 having its drain coupled to node 450, its source coupled to the selected flash cell 401 via the column decode 420, and its gate coupled to the output of an inverter 442 which has an input coupled to the source of FET 441. Alternatively, the n-channel FET 441 may be coupled as a static gate cascode.

The voltage at node 450 is a function of the drain-source current of the selected flash cell 401. In turn, the cell current of the selected flash cell 401 is a function of the amount of charge on the floating gate 402. As $V_t$ increases, the cell current decreases. Similarly, the cell current increases as $V_t$ decreases. Thus, if the selected flash cell 401 is in state 1, the voltage at node 450 is less than if the selected flash cell 401 is in state 2.

In this circuit, comparators 460 and 470 determine the state of the selected flash cell 401 by comparing the voltage at node 450 to the voltages at reference nodes 465 and 475, respectively. In this embodiment, the voltage at reference node 465 is determined by a reference flash cell 486 that has a $V_t$ set to at $V_{R2}$. Thus, the voltage at reference node 465 is greater than the voltage at node 450 if the selected flash cell 401 is programmed to state 1 or state 2. The voltage at node 465 is less than the voltage at node 450 if the selected flash cell 401 is programmed to state 3 or state 4. The reference flash cell 486 has its source coupled to ground, its gate coupled to the biasing voltage $V_S$, and its drain coupled to a reference drain bias circuit 467, which is preferably identical to the drain bias circuit 440. The drain bias circuit 467 is coupled to a reference column load circuit 466, which is preferably identical to column load 445. For the comparator 470, the voltage at reference node 475 is determined by a selected one of reference flash cells 487 and 488 having $V_t$s equal to $V_{R1}$ and $V_{R3}$, respectively. Reference node 475 is similarly coupled to a reference column load 466 and a reference drain bias 467.

There are a number of different ways for providing a reference voltage to sense the state of the selected flash cell. For example, one scheme is to provide two reference cells having different threshold voltages $V_t$ with their drains coupled together. Two identical column load circuits are coupled in parallel to the drains of the two reference cells at the reference node. Assuming that the same voltage is applied to the select gates of the reference cells, the voltage at the reference node is equivalent to a single reference cell having a cell current equal to the average of the cell currents of the two reference cells multiplied by the resistance of a single column load circuit. Also, the voltage reference may be generated using a single reference cell with its gate driven to one of (n-1) different values by a digital-to-analog converter. For a further discussion of one reference circuit, see U.S. Patent No. 5,289,412, of Frary et al., and commonly assigned to Intel Corporation of Santa Clara, California.

Additionally, the current across the reference column load 466 may be produced by circuits other than reference flash cells. For example, a constant current source or current mirror may be used. The use of current mirror circuits in conjunction with an array of reference flash cells provides the needed reference currents for sensing multiple flash cells simultaneously without having to reproduce the array of reference flash cells for each output of the memory device.

The negative terminals of comparators 460 and 470 are both coupled to node 450 for sensing the voltage resulting from applying the biasing voltage $V_S$ to the select gate of the selected flash cell 401. Comparator 460 has its positive terminal coupled to reference node 465. The positive terminal of comparator 470 is coupled to reference node 475. The selection between the reference flash cells 487 and 488 is made in response to the output of comparator 460. A selector circuit 480 is coupled between the output signal line 491 of the comparator 460 and the first and second reference cells.

The selector circuit 480 includes a first n-channel FET 481 coupled between the drain bias circuit 467 and the reference flash cell 487, and a second n-channel FET 482 coupled between the drain bias circuit 467 and the reference flash cell 488. The signal line 490, which is the output of the comparator 460, is coupled to the gate of FET 481. An inverter 483 is coupled between the output signal line 490 and the gate of the second FET 477. If the output of the first comparator 460 is a logic 1, indicating that the selected flash cell 401 has a lower $V_t$ than the reference flash cell 486, the first FET 481 is switched on, and the second comparator 470 is coupled to the reference flash cell 487. If the output of the first comparator 460 is a logic 0, the inverter inverts the output to switch the FET 482 on, coupling the second comparator 470 to the reference flash cell 488. The second comparator 470 outputs the result of the second comparison via output signal line 491. For this embodiment, the output signal line 490 outputs the high order bit Bit 1 and the output signal line 491 outputs the low order bit Bit 0. In this manner, no decoding logic is necessary as the outputs of the comparators 460 and 470 correspond directly to the state of the selected flash cell 401. Output signal lines 490 and 491 may thus be mapped directly to the outputs of a memory device such that both bits of athe selected flash cell 401 are read out in a parallel fashion.

The sensing circuit of this embodiment is especially useful when the number n of possible states is a power of two, i.e. when ($\log_2$ n) is an integer, because the circuit is configured to perform a binary search. When n is equal to 4 the threshold voltage $V_t$ of the first reference cell is preferably in the separation range between the (n/2) state and the (n/2 + 1) state. If the threshold voltage $V_t$ voltage of the first reference cell is greater than the threshold voltage $V_t$ of the selected flash cell, the threshold voltage $V_t$ of the second reference cell is preferably in the separation range between the (n/4) state and the (n/4 + 1) state. If the threshold voltage $V_t$ of the first reference cell is less than the threshold voltage $V_t$ of the selected flash cell, the threshold voltage $V_t$ of the

second reference cell is preferably in the separation range between the (3n/4) state and the ((3n/4) + 1)) state. For each additional bit of stored per cell, a single comparator is preferably added and the selector circuit is modified.

When n is equal to 8, 16, 32, etc., the selection of reference cells continues in a similar manner, the remaining states being bisected until the states of all bits stored in the flash cell are determined. **Figure 6** is a distribution of flash cells versus $V_t$ for a flash device capable of having eight states. **Figure 7** shows a flow chart for a binary search when the number of states is equal to 8. According to **Figure 7**, the binary search of the eight reference cells begins at step 711 with the initial comparison of the cell charge level of the selected cell to the cell charge level of a first reference cell having a $V_t$ equal to $V_{R4}$. If the sensed cell charge level is less than that of the first reference cell, the search continues in steps 712, 713 and 714 as described in steps 301, 302 and 303 of **Figure 4A**. If the sensed cell charge level is greater than that of the first reference cell, the search continues as shown in steps 722, 723 and 724. Each state is represented by three binary bits.

**Figure 8** illustrates a sensing circuit utilizing a single comparator to determine the state of a flash cell having four possible states. Unlike the first embodiment, this embodiment is a synchronous circuit. Like the first embodiment, the negative terminal of comparator 460 is coupled to node 450, and the positive terminal of comparator 460 is coupled to reference node 465. A decode circuit 563 determines which one of the three reference flash cells 486, 487, and 488 is to be coupled to the reference drain bias circuit 467. When the number of states is equal to four, the counter 566 starts with a count of 0 and has a maximum count of one. The maximum count is increased by one for each additional bit of data stored in a flash cell. For a three bit cell, the maximum count would be two. The clock generator 567 provides a clock signal to the counter 566, which increases its count by one, each clock cycle. The frequency of the

clock generator may be determined by methods that are well-known in the art.

The decode circuit 563 has the output of the counter 566 and the output of the first latch 580 as inputs. An exemplary truth table for the decode circuit 563 is illustrated in Table 2. The FETs 610, 615, 620 and 625, along with the inverters 605 and 630, implement the truth table of Table 2, which is a binary search similar to that shown in **Figures 4A-4B**.

Table 2

| COUNT | FIRST RESULT | $V_{REF}$ |
|---|---|---|
| 0 | X | $V_{R2}$ |
| 1 | 1 | $V_{R1}$ |
| 1 | 0 | $V_{R3}$ |

During a read operation, the counter is initialized to 0 such that the drain bias 467 is coupled to reference flash cell 486. The reference flash cell 486 has a threshold voltage $V_t$ equal to $V_{R2}$. The result of the first comparison is stored in latch 580. The first result is output by the latch 580 via signal line 590, which is fed back to the decoding circuit 563. If the first result is a logic 1, the reference flash cell 487, which has a threshold voltage $V_t$ equal to $V_{R1}$, is selected, and the voltage at node 555 is compared to the voltage at node 550. If the first result is a logic 0, the reference flash cell 488 having a threshold voltage $V_t$ equal to $V_{R3}$ is selected. The second result is output by the comparator 560 and stored in the latch 585. The second result is output by the latch 585 via signal line 591. Output signal line 590 outputs the high order bit Bit 1, and output signal line 591 outputs the low order bit Bit 0.

In the foregoing specification the invention has been described with reference to specific exemplary embodiments thereof. It will,

however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than restrictive sense.

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CLAIMS

What is claimed is:

1. In a memory device including at least one memory cell having a cell charge level that indicates one of n possible states, wherein n is greater than 2, each state corresponding to a predetermined range of charge levels, a method for determining a state of the memory cell, the method comprising the steps of:

sensing the cell charge level of the memory cell;

comparing the cell charge level of the memory cell to a first reference;

outputting a first result of comparing the cell charge level of the memory cell to the first reference;

comparing the cell charge level of the memory cell to a selected one of a second reference and a third reference, wherein selection between the second and third references is done in response to the first result; and

outputting a second result of comparing the cell charge level of the memory cell to the selected one of the second and third references.

2. The method of claim 1, wherein the step of comparing the cell charge level of the memory cell to the selected one of the second reference and the third reference includes the further steps of:

comparing the cell charge level of the memory cell to the second reference if the cell charge level of the memory cell is less than the first reference as indicated by the first result; and

comparing the cell charge level of the memory cell to the third reference if the cell charge level of the memory cell is greater than the first reference as indicated by the first result.

3. The method of claim 2, wherein n is equal to four, the steps of outputting the first and second results comprising the steps of:

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indicating that the memory cell is in a first state if the cell charge level of the memory cell is less than both the first and second references;

indicating that the memory cell is in a second state if the cell charge level of the memory cell is less than the first reference and greater than the second reference;

indicating that the memory cell is in a third state if the cell charge level of the memory cell is greater than the first reference and less than third reference; and

indicating that the memory cell is in a fourth state if the cell charge level of the memory cell is greater than both the first and third references.

4. The method of claim 2, wherein the memory cell is a nonvolatile memory cell having a floating gate for storing charge.

5. The method of claim 4, wherein the first reference is a first reference memory cell and the second reference is a second reference memory cell, the first and second references memory cells having floating gates for storing charge.

6. The method of claim 5, wherein the first reference memory cell has a first cell charge level corresponding to a level of charge between the second and third states.

7. The method of claim 6, wherein the second reference memory cell has a second cell charge level corresponding to a level of charge between the first and second states.

8 The method of claim 7, wherein the step of sensing the cell charge level of the memory cell comprises the step of generating a cell current for the memory cell.

9. The method of claim 8, wherein the step of comparing the cell charge level of the memory cell to the first reference comprises the steps of generating a reference cell current for the first reference memory cell, and comparing the cell current to the reference cell current.

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10. The method of claim 7, wherein the step of sensing the cell charge level of the memory cell comprises the steps of generating a cell current for the memory cell, and generating a voltage in response to the cell current.

11. The method of claim 10, wherein the step of comparing the cell charge level of the memory cell to the first reference comprises the steps of:

generating a reference cell current for the first reference memory cell;

generating a reference voltage in response to the reference cell current; and

comparing the voltage to the reference cell voltage.

12. The method of claim 7, wherein the first reference is a first current source for generating a current equal to a cell current of a memory cell that stores a level of charge between the second and third states.

13. The method of claim 4, wherein the first reference is provided by applying a first gate voltage to a first reference cell, the second reference is provided by applying a second gate voltage to the first reference cell, and the third reference is provided by applying a third gate voltage to the first reference cell, the first reference cell having a floating gate for storing charge.

14. In a memory device including at least one memory cell having a cell charge level that indicates one of three possible states, each state corresponding to a predetermined range of charge levels, a method for determining a state of the memory cell, the method comprising the steps of:

sensing the cell charge level of the memory cell;

comparing the cell charge level of the memory cell to a first reference;

selecting a second reference if the cell charge level of the memory cell is less than the first reference;

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comparing the cell charge level of the memory cell to the second reference;

indicating that the memory cell is in a first state if the cell charge level is less than the second reference;

indicating that the memory cell is in a second state if the cell charge level is greater than the second reference; and

indicating that the memory cell is in a third state if the cell charge level is greater than the first reference.

15. The memory device of claim 14, wherein the memory cell is a nonvolatile memory cell having a floating gate for storing charge.

16. The memory device of claim 15, wherein the first reference is a first reference memory cell and the second reference is a second reference memory cell, the first and second references memory cells having floating gates for storing charge.

17. The memory device of claim 16, wherein the first reference memory cell has a first cell charge level corresponding to a level of charge between the second and third states.

18. The memory device of claim 17, wherein the second reference memory cell has a second cell charge level corresponding to a level of charge between the first and second states.

19. The memory device of claim 18, wherein the step of sensing the cell charge level of the memory cell comprises the step of generating a cell current for the memory cell.

20. The memory device of claim 19, wherein the step of comparing the cell charge level of the memory cell to the first reference comprises the steps of generating a reference cell current for the first reference memory cell, and comparing the cell current to the reference cell current.

21. The memory device of claim 18, wherein the step of sensing the cell charge level of the memory cell comprises the steps of generating a cell current for the memory cell, and generating a voltage in response to the cell current.

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22. The memory device of claim 21, wherein the step of comparing the cell charge level of the memory cell to the first reference comprises the steps of generating a reference cell current for the first reference memory cell, generating a reference voltage in response to the reference cell current, and comparing the voltage to the reference cell voltage.

23. The memory device of claim 18, wherein the first reference is a first current source for generating a current equal to a cell current of a memory cell that stores a level of charge between the second and third states.

24. The method of claim 15, wherein the first reference is provided by applying a first gate voltage to a first reference cell and the second reference is provided by applying a second gate voltage to the first reference cell, the first reference cell having a floating gate for storing charge.

25. In a memory device including at least one memory cell having a cell charge level that indicates one of four possible states, each state corresponding to a predetermined range of charge levels, a method for determining a state of the memory cell, the method comprising the steps of:

sensing the cell charge level of the memory cell;

comparing the cell charge level of the memory cell to a first reference;

selecting a second reference if the cell charge level of the memory cell is less than the first reference;

comparing the cell charge level of the memory cell to the second reference;

indicating that the memory cell is in a first state if the cell charge level is less than the second reference;

indicating that the memory cell is in a second state if the cell charge level is greater than the second reference; and

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selecting a third reference if the cell charge level of the memory cell is greater than the first reference;

comparing the cell charge level of the memory cell to the third reference;

indicating that the memory cell is in a third state if the cell charge level is less than the second reference; and

indicating that the memory cell is in a fourth state if the cell charge level is greater than the second reference; and

26. The memory device of claim 25, wherein the memory cell is a nonvolatile memory cell having a floating gate for storing charge.

27. The memory device of claim 26, wherein the first reference is a first reference memory cell and the second reference is a second reference memory cell, the first and second references memory cells having floating gates for storing charge.

28. The memory device of claim 27, wherein the first reference memory cell has a first cell charge level corresponding to a level of charge between the second and third states.

29. The memory device of claim 28, wherein the second reference memory cell has a second cell charge level corresponding to a level of charge between the first and second states.

30. The memory device of claim 29, wherein the third reference memory cell has a third cell charge level corresponding to a level of charge between the third and fourth states.

31. The memory device of claim 30, wherein the step of sensing the cell charge level of the memory cell comprises the step of generating a cell current for the memory cell.

32. The memory device of claim 31, wherein the step of comparing the cell charge level of the memory cell to the first reference comprises the steps of generating a reference cell current for the first reference memory cell, and comparing the cell current to the reference cell current.

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33. The memory device of claim 30, wherein the step of sensing the cell charge level of the memory cell comprises the steps of generating a cell current for the memory cell, and generating a voltage in response to the cell current.

34. The memory device of claim 30, wherein the step of comparing the cell charge level of the memory cell to the first reference comprises the steps of generating a reference cell current for the first reference memory cell, generating a reference voltage in response to the reference cell current, and comparing the voltage to the reference cell voltage.

35. The memory device of claim 25, wherein the first reference is a first current source for generating a current equal to a cell current of a memory cell that stores a level of charge between the second and third states.

36. In a memory device including at least one memory cell having a threshold voltage level that indicates one of n possible states, wherein n is greater than 2, each state corresponding to a predetermined range of threshold voltage levels, a method for determining a state of the memory cell, the method comprising the steps of:

providing m references, where m is equal to at least n-1, each of the m references corresponding to a threshold voltage level between two states;

sensing the threshold voltage level of the memory cell;

comparing the threshold voltage level of the memory cell to a first reference;

outputting a first result of comparing the threshold voltage level of the memory cell to the first reference;

comparing the threshold voltage level of the memory cell to a selected one of a second reference and a third reference in response to the first result; and

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outputting a second result of comparing the threshold voltage level of the memory cell to the selected one of the second reference and the third reference.

37. The method of claim 36, wherein the step of comparing the threshold voltage level of the memory cell to the selected one of the second reference and the third reference includes the further steps of:

if the threshold voltage level of the memory cell is less than the first reference as indicated by the first result, comparing the threshold voltage level of the memory cell to the second voltage reference; and

if the threshold voltage level of the memory cell is greater than the first reference as indicated by the first result, comparing the threshold voltage level of the memory cell to the third reference.

38. The method of claim 37, wherein the first reference corresponds to a threshold voltage level between a n/2 state and a (n/2 + 1) state.

39. The method of claim 38, wherein the second reference corresponds to a threshold voltage level between a (n/4) state and a (n/4 +1) state.

40. The method of claim 39, wherein the third reference corresponds to a threshold voltage level between a (3n/4) state and a (3n/4 + 1) state.

41. The method of claim 37, wherein the first and second results are each expressed using a single binary bit.

42. The method of claim 37, wherein ($\log_2$ n) is equal to an integer.

43. The method of claim 37, wherein n is equal to four.

44. The method of claim 37, wherein n is equal to eight.

45. In a memory device including at least one memory cell having a threshold voltage level that indicates one of n possible states, where n is greater than 2, each state corresponding to a predetermined range of threshold voltage levels, a sensing circuit for determining a state of the memory cell, the sensing circuit comprising:

a first reference corresponding to a first threshold voltage level;

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a first comparator coupled to the memory cell and to the first reference, the first comparator for comparing the threshold voltage level of the memory cell to the first reference, and for outputting a first result;

a second reference corresponding to a second threshold voltage level;

a third reference corresponding to a third threshold voltage level;

a second comparator coupled to the memory cell and a selected one of the second reference and the third reference, the second comparator for comparing the threshold voltage level of the memory cell to the selected one of the second reference and the third reference, and for outputting a second result; and

a selector circuit coupled for receiving the first result, the selector circuit for selectively coupling the one of the second reference and the third reference to the second comparator in response to the first result.

46. The sensing circuit of claim 45, wherein the selector circuit couples the second reference to the second comparator if the threshold voltage level of the memory cell is less than the first reference.

47. The sensing circuit of claim 46, wherein the selector circuit couples the third reference to the second comparator if the threshold voltage level of the memory cell is greater than the first reference.

48. The sensing circuit of claim 47, wherein the first threshold voltage level is between a n/2 state and a (n/2 + 1) state.

49. The sensing circuit of claim 48, wherein the third threshold voltage level is between a 3n/4 state and a (3n/4 + 1) state.

50. The sensing circuit of claim 49, wherein the second threshold voltage level is between a n/4 state and a (n/4 + 1) state.

51. The sensing circuit of claim 50, wherein n is equal to four.

52. The sensing circuit of claim 50, wherein n is equal to eight.

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53. The sensing circuit of claim 45, wherein the sensing circuit further comprises a first reference cell having a select gate and a floating gate for storing charge, the first reference cell for providing the first reference in response to a first gate voltage, for providing the second reference in response to a second gate voltage, and for providing the third reference in response to a third gate voltage, the first, second, and third gate voltages being applied to the select gate of the first reference cell.

54. In a memory device including at least one memory cell having a threshold voltage level that indicates one of n possible states, where n is greater than 2, each state corresponding to a predetermined range of voltage levels, a sensing circuit for determining a state of the memory cell, the sensing circuit comprising:

a number m references, where m is equal to n-1, each of the m references corresponding to a threshold voltage level between two states;

a comparator coupled to the memory cell and a selected one of the m references, the second comparator for comparing the threshold voltage level of the memory cell to a first reference, for outputting a first result, for comparing the cell voltage level to a one of a second and third reference, and for outputting a second result; and

a selector circuit coupled for receiving the first result, the selector circuit for initially coupling the first reference to the comparator, and for selectively coupling the one of the second reference and the third reference to the comparator in response to the first result.

55. The sensing circuit of claim 54, wherein the selector circuit couples the second reference to the second comparator if the threshold voltage level of the memory cell is less than the first reference.

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56. The sensing circuit of claim 55, wherein the selector circuit couples the third reference to the second comparator if the threshold voltage level of the memory cell is greater than the first reference.

57. The sensing circuit of claim 56, wherein the first voltage level is between a n/2 state and a (n/2 + 1) state.

58. The sensing circuit of claim 57, wherein the third voltage level is between a 3n/4 state and a (3n/4 + 1) state.

59. The sensing circuit of claim 58, wherein the second voltage level is between a n/4 state and a (n/4 + 1) state.

60. The sensing circuit of claim 54, wherein n is equal to four.

61. The sensing circuit of claim 54, wherein n is equal to eight.

62. The sensing circuit of claim 54, wherein the sensing circuit further comprises a first reference cell having a select gate and a floating gate for storing charge, the first reference cell for providing the first reference in response to a first gate voltage, for providing the second reference in response to a second gate voltage, and for providing the third reference in response to a third gate voltage, the first, second, and third gate voltages being applied to the select gate of the first reference cell.

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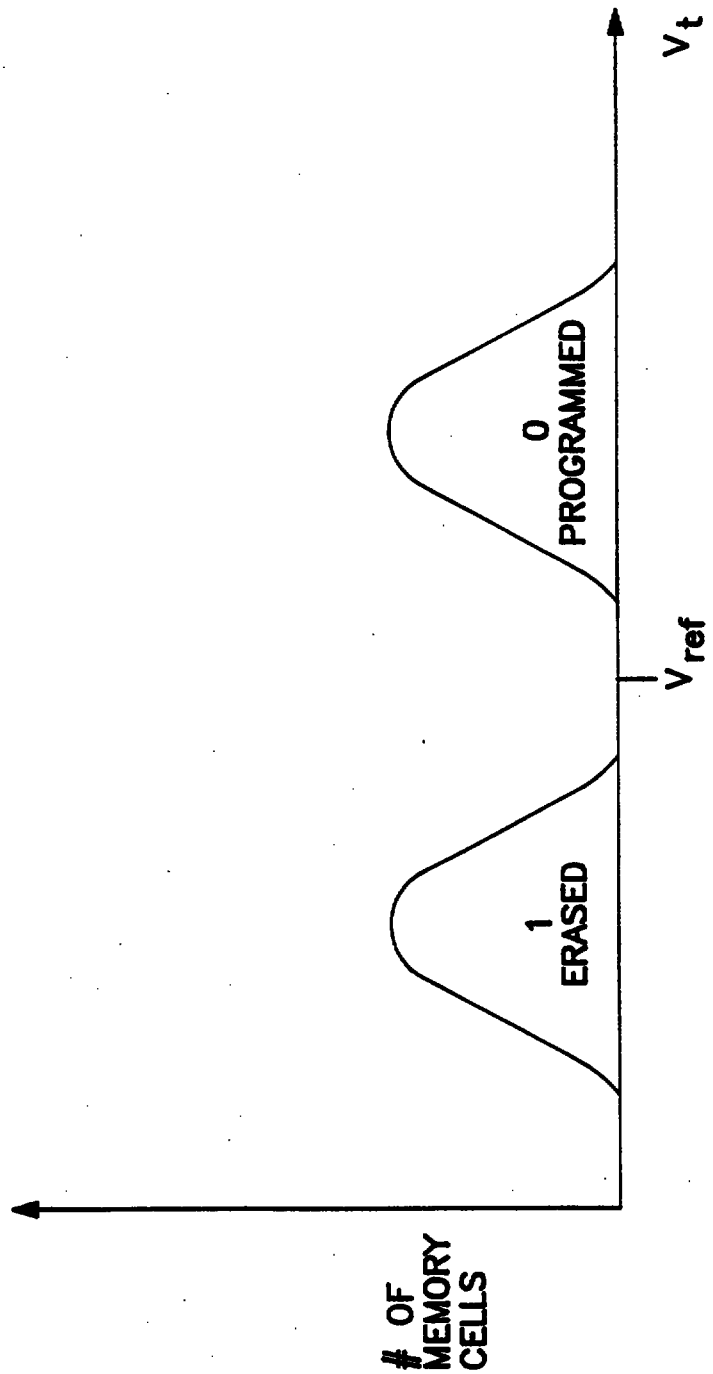
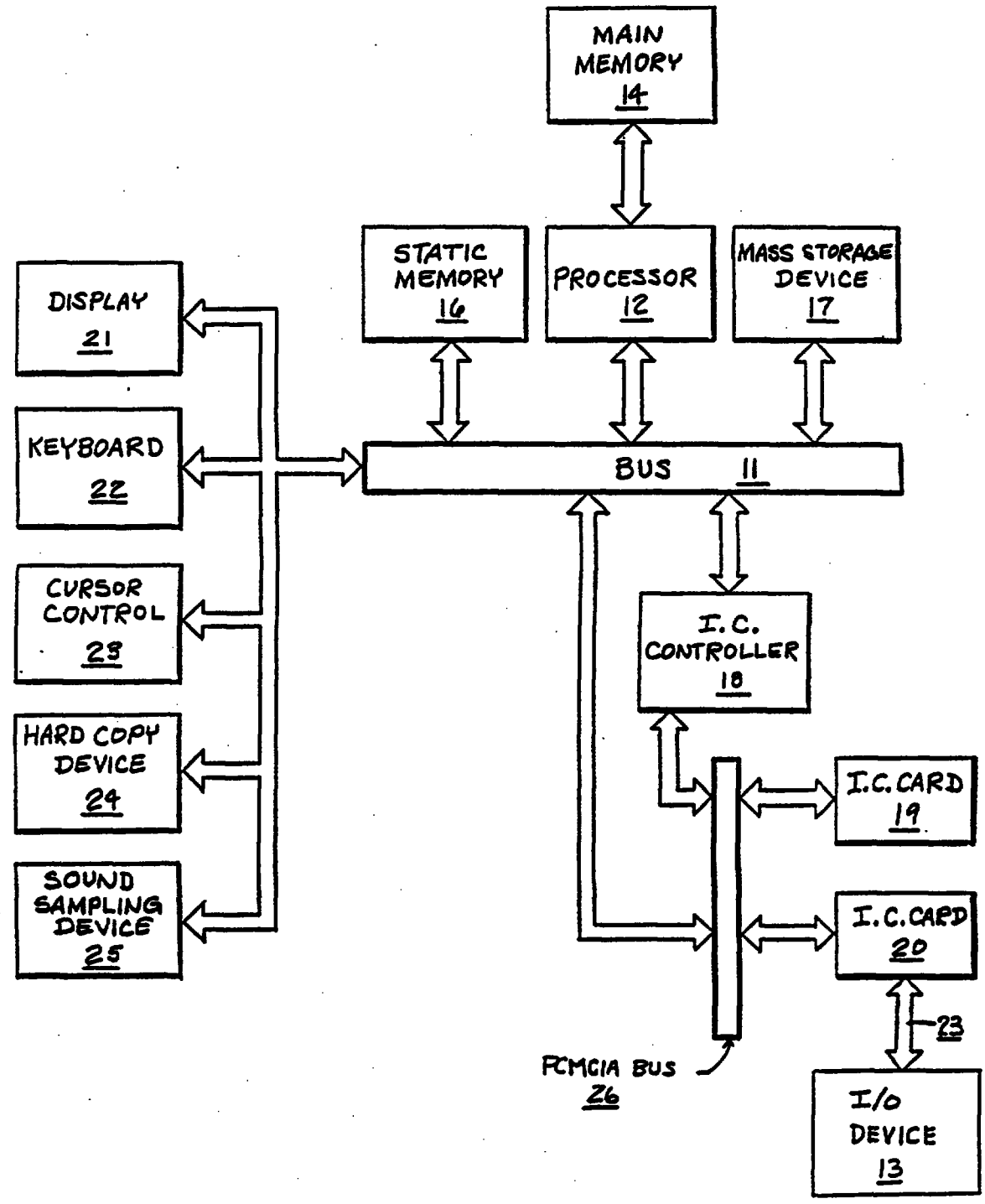



FIG. 1
PRIOR ART

FIG. 2


MAIN MEMORY 14
STATIC MEMORY 16
PROCESSOR 12
MASS STORAGE DEVICE 17
DISPLAY 21
KEYBOARD 22
CURSOR CONTROL 23
HARD COPY DEVICE 24
SOUND SAMPLING DEVICE 25
BUS 11
I.C. CONTROLLER 18
I.C. CARD 19
I.C. CARD 20
23
I/O DEVICE 13
PCMCIA BUS 26

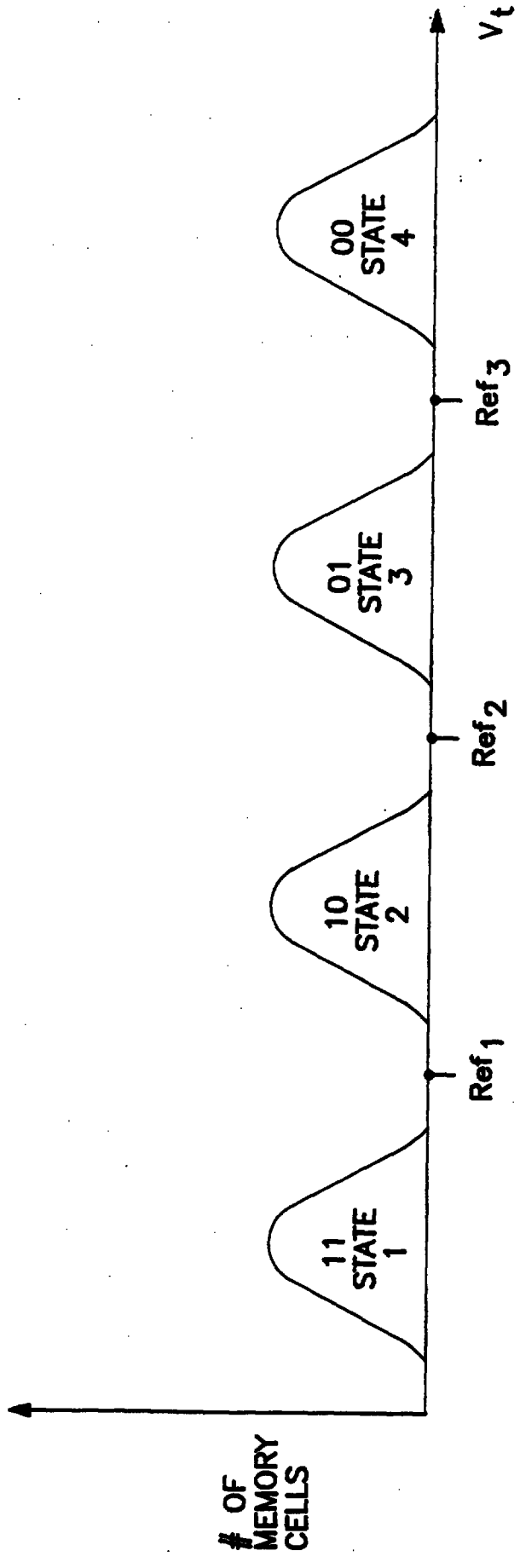

$V_t$
00
STATE
4
01
STATE
3
10
STATE
2
11
STATE
1
$Ref_3$
$Ref_2$
$Ref_1$
# OF
MEMORY
CELLS

FIG. 3

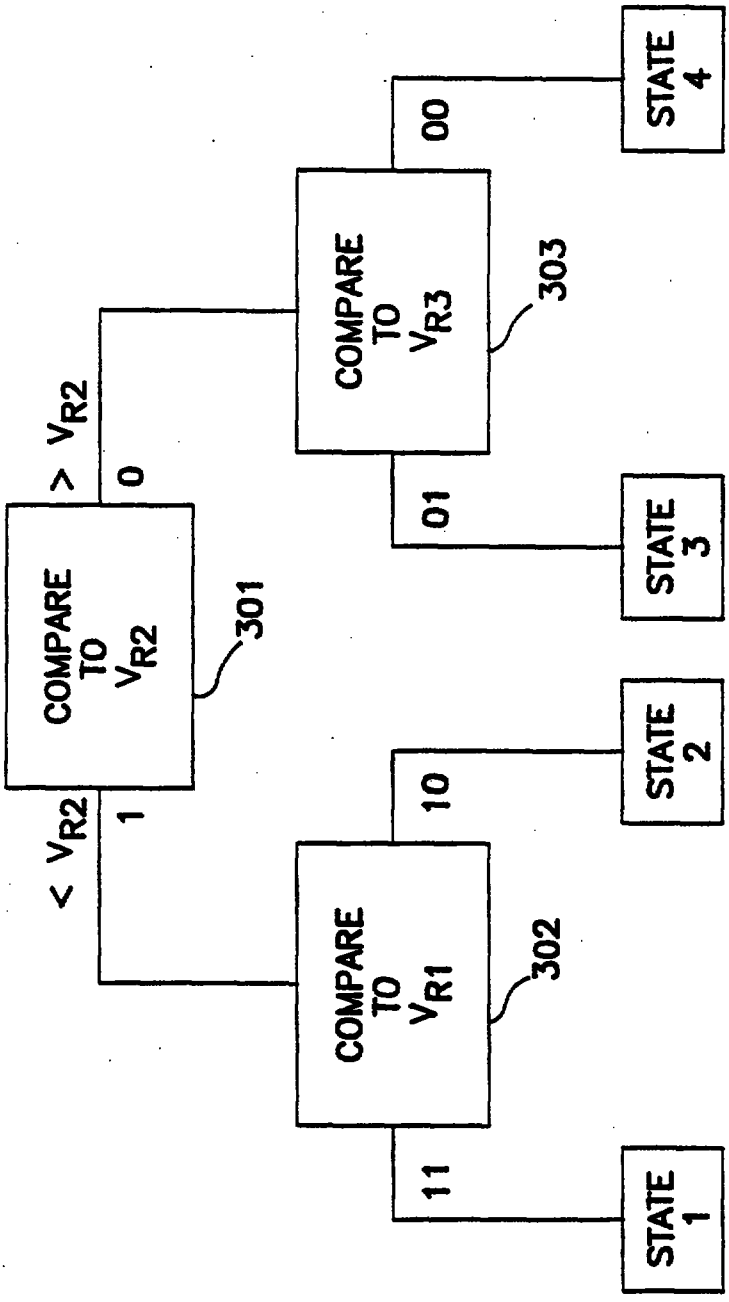

COMPARE TO $V_{R2}$
301
> $V_{R2}$
0
< $V_{R2}$
1
COMPARE TO $V_{R3}$
303
COMPARE TO $V_{R1}$
302
00
01
10
11
STATE 4
STATE 3
STATE 2
STATE 1

FIG. 4A

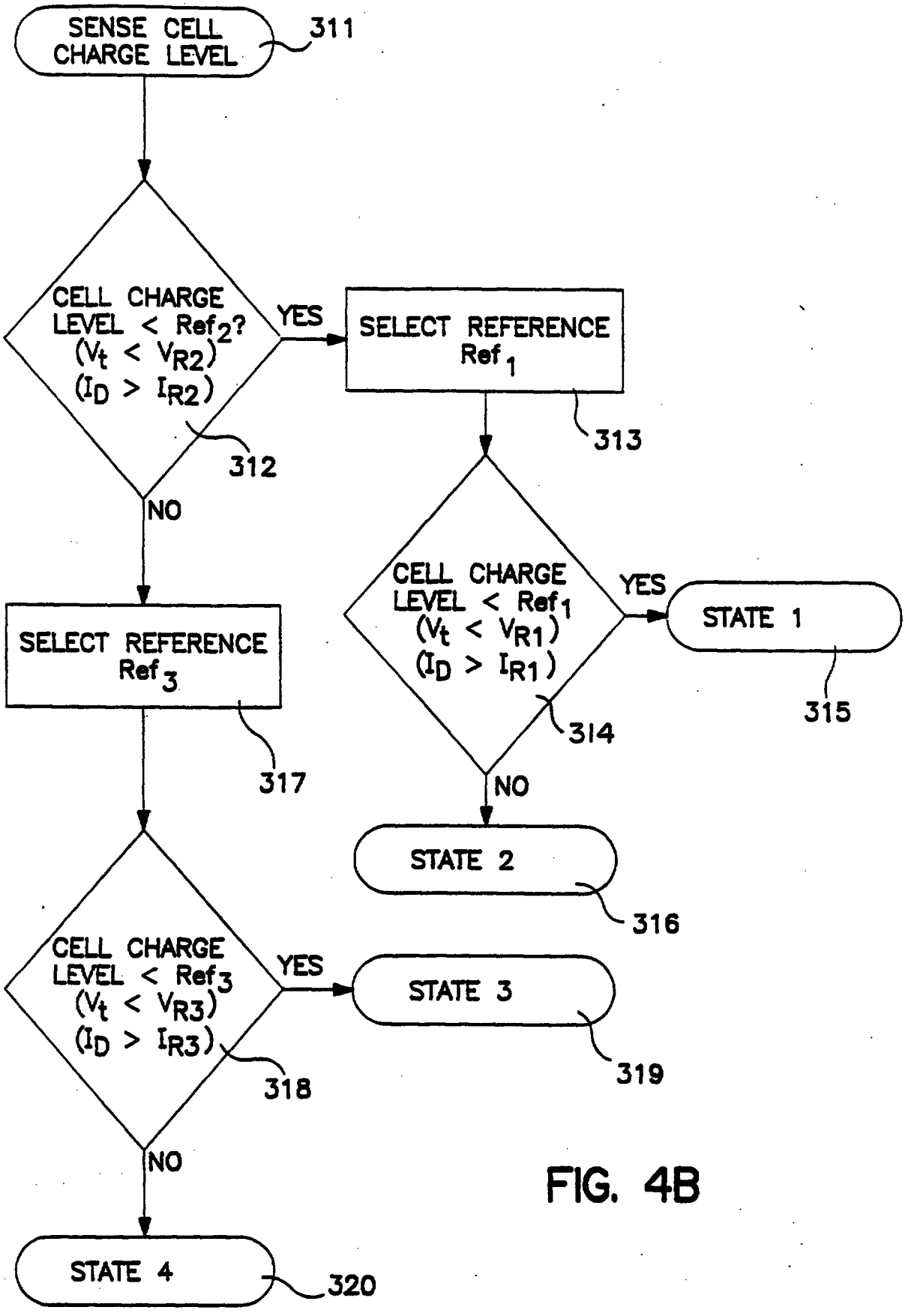

SENSE CELL CHARGE LEVEL
311
CELL CHARGE LEVEL < Ref2? (Vt < VR2) (ID > IR2)
312
YES
SELECT REFERENCE Ref1
313
NO
CELL CHARGE LEVEL < Ref1 (Vt < VR1) (ID > IR1)
314
YES
STATE 1
315
NO
STATE 2
316
SELECT REFERENCE Ref3
317
CELL CHARGE LEVEL < Ref3 (Vt < VR3) (ID > IR3)
318
YES
STATE 3
319
NO
STATE 4
320

FIG. 4B

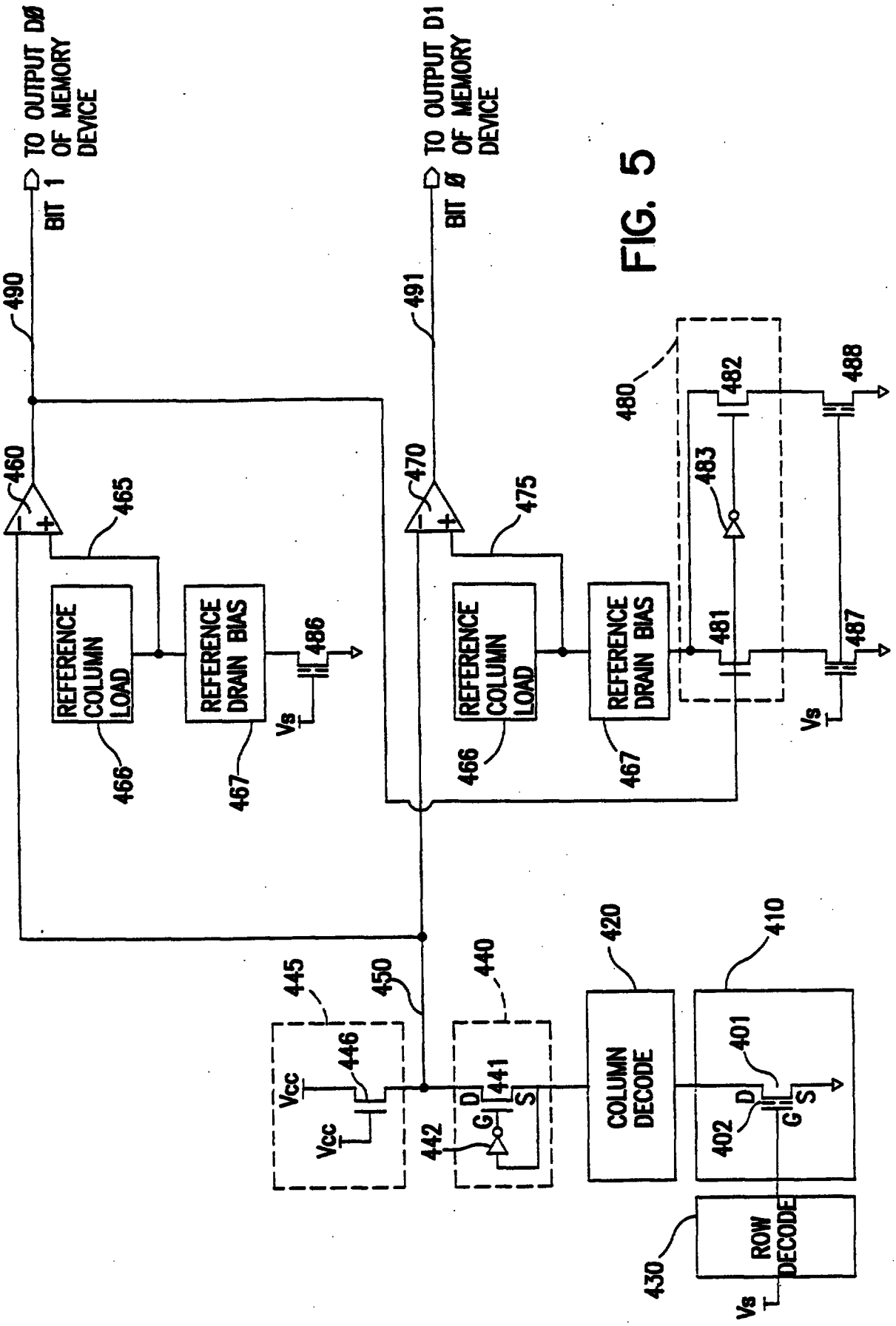

TO OUTPUT DØ OF MEMORY DEVICE
BIT 1
TO OUTPUT D1 OF MEMORY DEVICE
BIT Ø
490
491
460
470
465
475
REFERENCE COLUMN LOAD
REFERENCE DRAIN BIAS
466
467
486
Vs
480
482
483
488
481
487
445
446
Vcc
450
440
441
442
420
COLUMN DECODE
410
401
402
430
ROW DECODE

FIG. 5

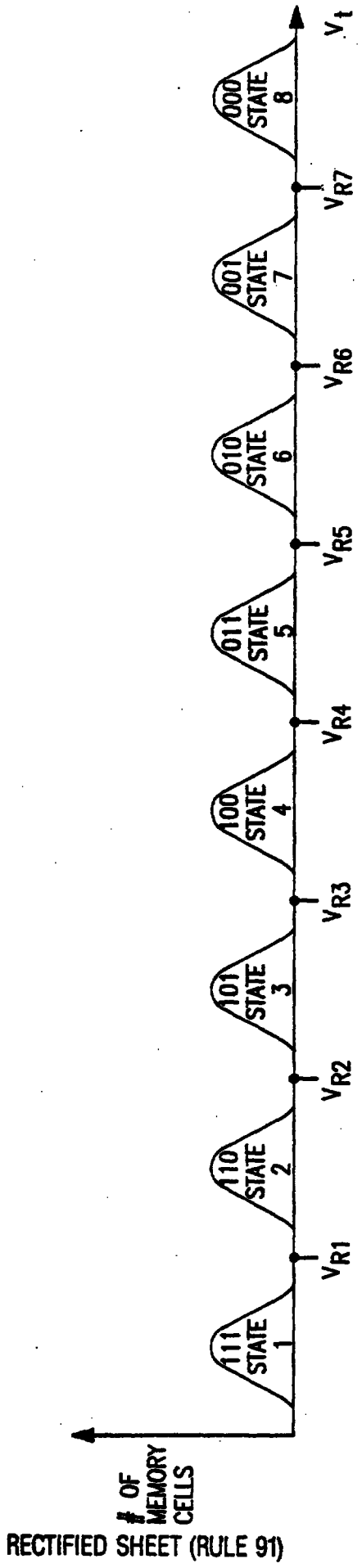

111 STATE 1
110 STATE 2
101 STATE 3
100 STATE 4
011 STATE 5
010 STATE 6
001 STATE 7
000 STATE 8
$V_{R1}$
$V_{R2}$
$V_{R3}$
$V_{R4}$
$V_{R5}$
$V_{R6}$
$V_{R7}$
$V_t$
# OF MEMORY CELLS

FIG. 6

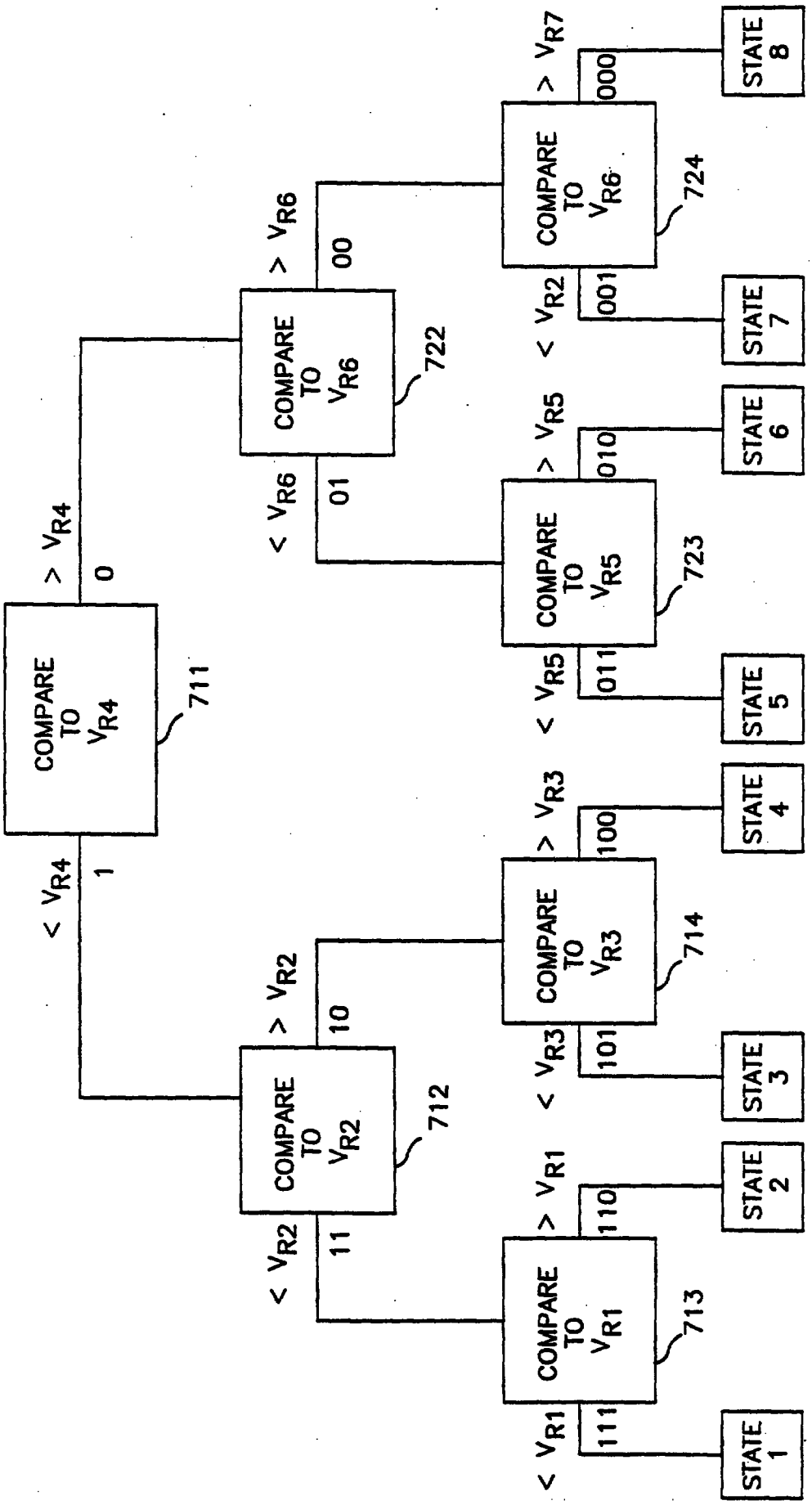

COMPARE TO $V_{R4}$
711
> $V_{R4}$
0
< $V_{R4}$
1
COMPARE TO $V_{R2}$
712
> $V_{R2}$
10
< $V_{R2}$
11
COMPARE TO $V_{R6}$
722
> $V_{R6}$
00
< $V_{R6}$
01
COMPARE TO $V_{R1}$
713
> $V_{R1}$
110
< $V_{R1}$
111
COMPARE TO $V_{R3}$
714
> $V_{R3}$
100
< $V_{R3}$
101
COMPARE TO $V_{R5}$
723
> $V_{R5}$
010
< $V_{R5}$
011
COMPARE TO $V_{R6}$
724
> $V_{R7}$
000
< $V_{R2}$
001
STATE 1
STATE 2
STATE 3
STATE 4
STATE 5
STATE 6
STATE 7
STATE 8

FIG. 7

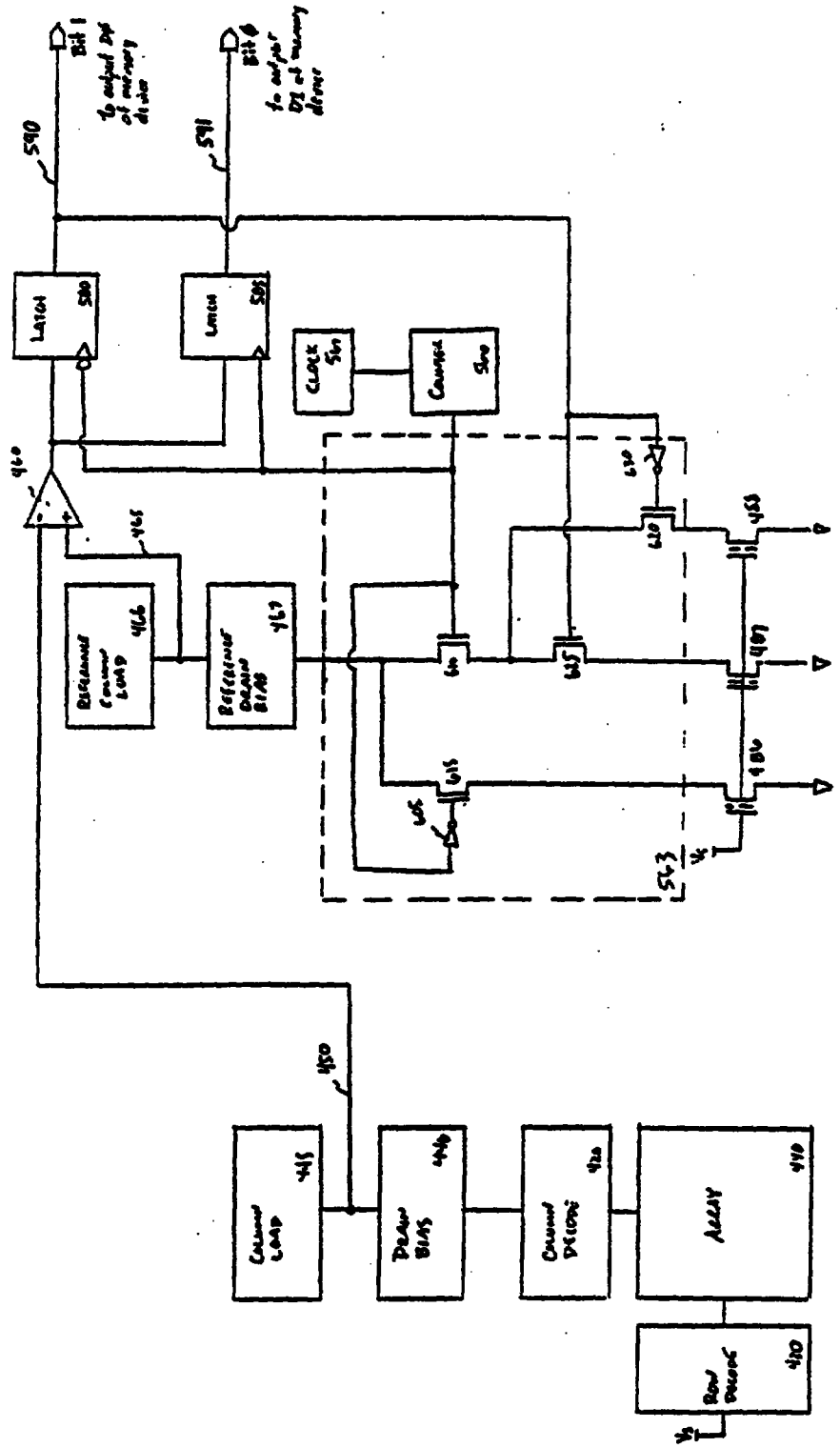

590
591
Latch
Latch
Clock Gen
Counter
Reference Column Load
Reference Column Bias
Column Load
Column Bias
Column Decode
Array
Row Decode

Figure 8

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**Claims**

1. In a flash memory device including at least one flash electrically-erasable programmable read-only memory (EEPROM) cell having n bits indicative of $2^n$ states, each state corresponding to a predetermined range of cell charge levels, a method for determining a state of the flash EEPROM cell, the method comprising the steps of:

a) sensing a cell charge level of the flash EEPROM cell;

b) comparing using a first comparator the cell charge level of the flash EEPROM cell and a reference cell charge level of a selected first reference cell;

c) outputting from the first comparator a result of step b) indicative of a first one of the n bits in the flash EEPROM cell;

d) supplying the result of step b) to an input of a selector circuit, the selector circuit selecting one of a second reference cell and a third reference cell, wherein selection between the second and third reference cells is done in response to the result of step b), the second reference cell being selected if the cell charge level of the flash EEPROM cell is less than the reference cell charge level of the selected first reference cell, and the third reference cell being selected if the cell charge level of the flash EEPROM cell is greater than the reference cell charge level of the selected first reference cell;

e) comparing using a second comparator the cell charge level of the flash EEPROM cell to the selected one of a reference cell charge level of the second reference cell and a reference cell charge level of the third reference cell; and

f) outputting from the second comparator a result of step e) indicative of a second one of the n bits of the flash EEPROM cell wherein the

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first comparator continues to output the result of step b) while steps d), e), and f) are performed such that the first comparator outputs the first one of the n bits and the second comparator outputs the second one of the n bits simultaneously to indicate the state of the flash EEPROM cell.

2. The method as described in Claim 63 further comprising the steps of:

g) in response to a result of step f), selecting one of a fourth reference cell and a fifth reference cell, the fourth reference cell being selected if the cell charge level of the flash EEPROM cell is a first value and the fifth reference cell being selected if the cell charge level of the flash EEPROM cell is a second value;

h) comparing the cell charge level of the flash EEPROM cell and a reference cell charge level of the selected one of the fourth and fifth reference cells; and

i) outputting a result of step h) indicative of an a third one of the n bits in the flash EEPROM cell wherein the first and second comparators continue to output the results of steps b) and f), respectively, while steps g), h), and i) are performed, such that the first comparator outputs the first one of the n bits and the second comparator outputs the second one of the n bits simultaneously with the third one of the n bits to indicate the state of the flash EEPROM cell.

3. In a flash memory device including at least one flash electrically-erasable programmable read-only memory (EEPROM) cell having n bits indicative of $2^n$ states, each state corresponding to a predetermined range of cell charge levels, a method for determining a state of the flash EEPROM cell, the method comprising the steps of:

a) sensing a cell charge level of the flash EEPROM cell;

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b) comparing using a comparator the cell charge level of the flash EEPROM cell and a reference cell charge level of a selected first reference cell in a decode circuit;

c) outputting from the comparator a result of step b) indicative of a first one of the n bits in the flash EEPROM cell;

d) supplying the result of step b) to an input of the decode circuit, the decode circuit selecting one of a second reference cell and a third reference cell in response to the result of step b), the second reference cell being selected if the cell charge level of the flash EEPROM cell is less than the reference cell charge level of the selected first reference cell, and the third reference cell being selected if the cell charge level of the flash EEPROM cell is greater than the reference cell charge level of the selected first reference cell;

e) comparing using the comparator the cell charge level of the flash EEPROM cell to the selected one of a reference cell charge level of the second reference cell and a reference cell charge level of the third reference cell; and

f) outputting from the comparator a result of step g) indicative of a second one of the n bits of the flash EEPROM cell wherein the result of step b) and the result of step e) indicate the state of the flash EEPROM cell.

4. A flash memory device including at least one flash electrically-erasable programmable read-only memory (EEPROM) cell that stores n bits that indicate one of $2^n$ states, each state corresponding to a predetermined range of cell charge levels, the flash memory device comprising:

a) a first comparator that performs a first comparison of a cell charge level of the flash EEPROM cell and a first reference cell charge level

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of a first reference cell, wherein a result of the first comparison is output from the first comparator to indicate a value of the n bit of the flash EEPROM cell;

b) a selector circuit having an input for receiving the result of the first comparison, the selector circuit selecting one of a second reference cell and a third reference cell in response to the result of the first comparison, the second reference cell being selected if the charge level of the flash EEPROM cell is less than the first reference cell charge level, the third reference cell being selected if the charge level of the flash EEPROM cell is greater than the first reference cell charge level; and

c) a second comparator that performs a second comparison of the cell charge level of the flash EEPROM cell and the selected one of a second reference cell charge level of the second reference cell and a third reference cell charge level of the third reference cell, wherein a result of the second comparison is output from the second comparator to indicate the (n-1) bit of the flash EEPROM cell, wherein the first comparator continues to output the result of the first comparison while steps b) and c) are performed such that the first comparator outputs the n bit and the second comparator outputs the (n-1) bit simultaneously to indicate the state of the flash EEPROM cell.

5. A flash memory device comprising:

a flash electrically-erasable programmable read-only memory (EEPROM) cell having n bits indicative of $2^n$ states, each state corresponding to a predetermined range of cell charge levels;

a comparator coupled to the flash EEPROM cell; and

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a decode circuit coupled to the comparator and including n-1 reference cell charge levels, wherein the comparator outputs a first signal in response to a first comparison of a cell charge level of the flash EEPROM cell with a first one of the n-1 reference cell charge levels, wherein the first signal is indicative of an n bit in the flash EEPROM cell, wherein the decode circuit selects one of a second one and a third one of the n-1 reference cell charge levels in response to the first signal, wherein the comparator outputs a second signal in response to a second comparison of the cell charge level of the flash EEPROM cell to the selected one of the second and third reference cell charge levels, and wherein the second signal is indicative of an n-1 bit of the flash EEPROM cell.

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