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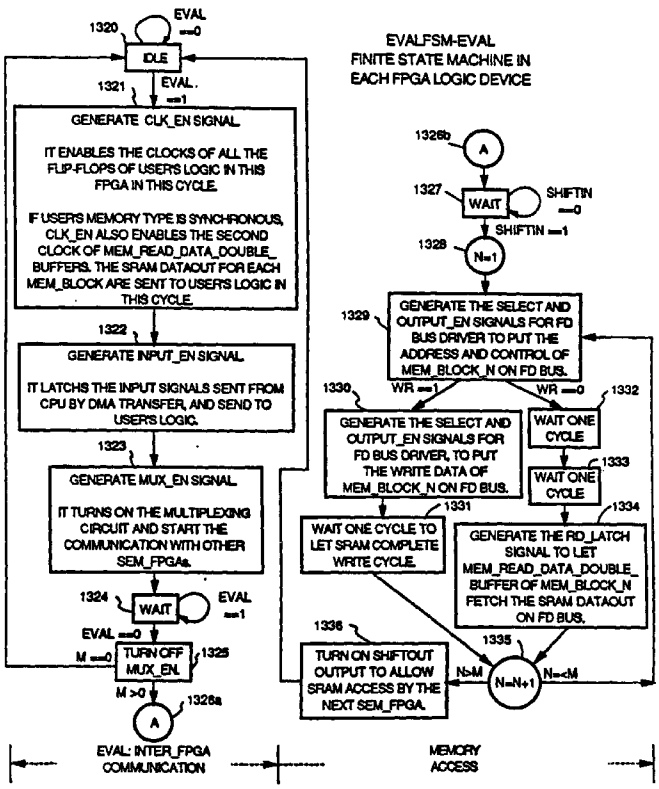
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(54) Title: TIMING-INSENSITIVE GLITCH-FREE LOGIC SYSTEM AND METHOD



(57) Abstract: A timing insensitive glitch-free (TIGF) logic device which can take the form of any latch or edge triggered flip-flop. In one embodiment, a trigger signal is provided to update the TIGF logic device. The trigger signal is provided during a short trigger period that occurs at adjacent times from the evaluation period (figure 59). In latch form, the TIGF latch includes a flip-flop that holds the current state of the TIGF latch until a trigger signal is received (figure 59). A multiplexer is also provided to receive the new input value and the old stored value. The enable signal functions as the selector signal for the multiplexer. In flip-flop form, the TIGF flip-flop includes a first flip-flop that holds the new input value, a second flip-flop that holds the current stored value, and a clock edge detector. Hold time violations are avoided because one dedicated flip-flop stores the new input value which effectively blocks input changes during evaluation.

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