

SPECIFICATION

Receiver for compatible AM stereo signals

5 Description

The present invention relates to the field of AM stereo receivers and more particularly to a receiver having an improved tuning arrangement.

A number of systems are known which provide AM stereo transmission and reception. One of these is compatible in that the envelope of the transmitted signal contains only the sum or monophonic information $(L + R)$ and all of the stereo information is transmitted by phase modulation of the carrier. In this known system, the stereo receiver demodulates the compatible signal in a symmetrical fashion; i.e., provides signals in quadrature which are then demodulated in synchronous detectors to provide sum and difference signals and, ultimately, L and R. A receiver utilizing synchronous detectors in both sum and difference channels may be difficult to tune properly, as the beats during the tuning-in period would have to be blocked out of the audio channels, and other provision made for tuning.

According to the present invention there is provided a receiver for receiving a carrier wave which is amplitude modulated with signal information proportional to the sum of first and second intelligence signals, and which is phase modulated with a signal proportional to an angle $\varnothing$ having the form $\varnothing = \arctan [C_1 (A - B)/C_2 + A + B]$ where C_1 and C_2 are constants, and A and B are said first and second intelligence signals respectively, the receiver comprising an input circuit for receiving said signal and deriving therefrom an intermediate frequency signal, an envelope detector circuit coupled to the input circuit for detecting the amplitude modulation on the intermediate frequency signal, a synchronous detector circuit coupled to the input circuit for providing an output proportional to $(A - B)\cos \varnothing$, a corrector circuit coupled to the input circuit and the synchronous detector circuit for providing an output proportional to $A - B$ and a matrix for processing the $A - B$ and $A + B$ signals to provide separate A and B outputs.

In a receiver constructed in accordance with one embodiment of the present invention, the incoming broadcast signal will be processed in conventional fashion in RF and IF stages, then the sum signal will be demodulated in an envelope detector and coupled to a matrix. The output of the IF stage is also processed in a synchronous detector to derive a signal having the form $(L - R)\cos \varnothing$ where $\varnothing = \arctan (L - R)/(1 + L + R)$. A corrector signal proportional to $\cos \varnothing$ is derived from the received signal and the output of the synchronous detector is divided by the corrector signal to produce the $L - R$ difference signal. The corrector signal is also processed to provide a control signal for locking out the difference channel during tuning and until the phase locked loop is locked in. Both the sum and difference signals are then processed in the matrix to provide L and R outputs.

The invention will now be described by way of example only with particular reference to the accompanying drawing wherein the sole figure is a block diagram of a diagram of a receiver embodying the present invention.

The receiver illustrated is designed to receive a compatible AM stereo signal from a transmitter. The broadcast signal of a transmitter is compatible with present monophonic receivers in that the carrier is amplitude modulated with a monophonic signal only $(1 + L + R)$, all stereo information being carried by phase modulation. In brief, the carrier is modulated in quadrature with the sum $(L + R)$ and difference $(L - R)$ signals, limited to remove amplitude variation and leaving only phase variation, then amplitude modulated with $1 + L + R$ in the high level modulator. The output or broadcast signal is then $(1 + L + R)\cos[\omega t + \arctan (L - R)/(1 + L + R)]$. It is to be noted that "L" and "R" are used herein in an exemplary fashion only.

In the receiver, an antenna 10 receives a compatible AM stereo signal of the form given hereinabove, and this signal is processed in the usual fashion in RF stage 11 and IF stage 12. The monophonic or sum signal $L + R$ is obtained by coupling the output of the IF stage to an envelope detector 13. The $L + R$ signal is then coupled to a matrix 14. An AGC detector 15 may be coupled from the output of the envelope detector 13 back to the IF stage 12 for controlling the gain in the IF stage, as is known in the art. The output of the IF stage 12 is also coupled to a synchronous detector 16 and to a limiter 17. The limiter 17 is coupled to a phase detector 18 which, with a lowpass filter 19 and a voltage controlled oscillator 20, comprises a phase locked loop (PLL) 22, an output of which $(\sin \omega t)$ is coupled to the synchronous detector 16. An output of the limiter 17, bearing only the transmitted phase information, is coupled to a cosine phase detector 23, as is an output $(\cos \omega t)$ of the phase locked loop 22. The cosine phase detector 23 is a multiplier of a type such as the Motorola MC 1595 four quadrant multiplier. The instantaneous phase difference between the two carrier frequencies (unmodulated and transmitted) is detected in the cosine phase detector 23 and provides the correction information necessary to restore the original stereo signals. The desired correction information is a signal proportional to the cosine of $\varnothing$ or $\cos \arctan [(L - R)/(1 + L + R)]$ or $(1 + L + R)/\sqrt{(1 + L + R)^2 + (L - R)^2}$. When the desired correction information is coupled to a divider 25 which also receives the output of the synchronous detector 16, the output of the divider becomes $L - R$, the desired stereo difference signal.

Until the receiver is properly tuned, however, the PLL 22 output is not a function of ωt , but is a frequency which approaches ωt as a broadcast signal is tuned in. The difference frequency would then appear in the correction signal at the output of the cosine phase detector 23 and cause an unacceptable output in the difference channel. Therefore, the cosine phase detector 23 output is also coupled to a lowpass filter 27 (2-10 Hz) where the average DC level of the output can be used to control a mono/stereo mode switch 28. The

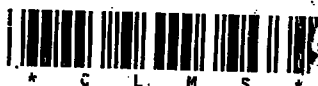
switch 28 is a voltage-controlled switch and is set to remain in the "monophonic" position until the PLL locks in on $\omega c t$, then switch to the "stereophonic" position.

In monophonic mode, only $L + R$ is coupled to the matrix, and the receiver is tuned in using this monophonic audio output only. When the receiver is tuned in, and the PLL is locked on $\omega c t$, the DC level of the cosine phase detector 23 output, as filtered through the filter 27, is sufficiently high to switch the mono/stereo switch 28 to the stereophonic mode. This allows the $L - R$ signal to be coupled to the matrix 14 which provides separated L and R at its output terminals.

In terms of signal, the output of the IF stage 12 will be proportional to $(1 + L + R) \cos(\omega c t + \phi)$ where $\phi = \arctan[(L - R)/(1 + L + R)]$. The output of the envelope detector 13 will be proportional to $L + R$. The output of the limiter 17 will be proportional to $\cos(\omega c t + \phi)$ and the outputs of the phase locked loop will be proportional to $\sin \omega c t$ and, after phase shifting, $\cos \omega c t$. The output of the synchronous detector 16 is the product of $(1 + L + R) \cos(\omega c t + \phi)$ and $\sin \omega c t$. Disregarding the double frequency term $2\omega c t$, and remembering that ϕ is $\arctan(L - R)/(1 + L + R)$, it is apparent that the product is proportional to $(L - R) \cos \phi$. The output of the cosine phase detector 23 will be proportional to $\cos \phi$ and the output of the divider 25 will thus be proportional to $(L - R) \cos \phi / \cos \phi$ or $(L - R)$. With inputs of $(L + R)$ and $(L - R)$, the matrix 14 will provide L and R outputs.

CLAIMS

1. A receiver for receiving a carrier wave which is amplitude modulated with signal information proportional to the sum of first and second intelligence signals, and which is phase modulated with a signal proportional to an angle ϕ having the form $\phi = \arctan[C_1(A - B)/C_2 + A + B]$ where C_1 and C_2 are constants, and A and B are the first and second intelligence signals respectively, the receiver comprising
 - an input circuit for receiving said signal and deriving therefrom an intermediate frequency signal,
 - an envelope detector circuit coupled to the input circuit for detecting the amplitude modulation on the intermediate frequency signal,
 - a synchronous detector circuit coupled to the input circuit for providing an output proportional to $(A - B) \cos \phi$,
 - a corrector circuit coupled to the input circuit and the synchronous detector circuit for providing an output proportional to $A - B$ and
 - a matrix for processing the $A - B$ and $A + B$ signals to provide separate A and B outputs.
2. A receiver as claimed in claim 1 wherein the input circuit includes an RF stage and an IF stage.
3. A receiver as claimed in claim 1 wherein the corrector circuit includes a limiter circuit, a circuit for providing a signal related to the phase of the unmodulated intermediate frequency signal, a cosine phase detector, coupled to the limiter circuit and the signal providing circuit for providing a signal proportional to $\cos \phi$, and a circuit for dividing the output signal of the synchronous detector by the output signal of the cosine phase detector.
4. A receiver substantially as hereinbefore described and as shown in the sole figure of the accompanying drawing.



switch 28 is a voltage-controlled switch and is set to remain in the "monophonic" position until the PLL locks in on ω_{ct} , then switch to the "stereophonic" position.

In monophonic mode, only $L + R$ is coupled to the matrix, and the receiver is tuned in using this monophonic audio output only. When the receiver is tuned in, and the PLL is locked on ω_{ct} , the DC level of the cosine phase detector 23 output, as filtered through the filter 27, is sufficiently high to switch the mono/stereo switch 28 to the stereophonic mode. This allows the $L - R$ signal to be coupled to the matrix 14 which provides separated L and R at its output terminals. 5

In terms of signal, the output of the IF stage 12 will be proportional to $(1 + L + R) \cos(\omega_{ct} + \emptyset)$ where $\emptyset = \arctan [(L - R)/(1 + L + R)]$. The output of the envelope detector 13 will be proportional to $L + R$. The output of the limiter 17 will be proportional to $\cos(\omega_{ct} + \emptyset)$ and the outputs of the phase locked loop will be proportional to $\sin \omega_{ct}$ and, after phase shifting, $\cos \omega_{ct}$. The output of the synchronous detector 16 is the product of $(1 + L + R) \cos(\omega_{ct} + \emptyset)$ and $\sin \omega_{ct}$. Disregarding the double frequency term $2\omega_{ct}$, and remembering that $\emptyset$ is $\arctan(L - R)/(1 + L + R)$, it is apparent that the product is proportional to $(L - R) \cos \emptyset$. The output of the cosine phase detector 23 will be proportional to $\cos \emptyset$ and the output of the divider 25 will thus be proportional to $(L - R) \cos \emptyset / \cos \emptyset$ or $(L - R)$. With inputs of $(L + R)$ and $(L - R)$, the matrix 14 will provide L and R outputs. 10 15

CLAIMS

1. A receiver for receiving a carrier wave which is amplitude modulated with signal information proportional to the sum of first and second intelligence signals, and which is phase modulated with a signal proportional to an angle $\emptyset$ having the form $\emptyset = \arctan [C_1(A - B)/C_2 + A + B]$ where C_1 and C_2 are constants, and A and B are the first and second intelligence signals respectively, the receiver comprising
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 - a corrector circuit coupled to the input circuit and the synchronous detector circuit for providing an output proportional to $A - B$ and
 - a matrix for processing the $A - B$ and $A + B$ signals to provide separate A and B outputs.
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3. A receiver as claimed in claim 1 wherein the corrector circuit includes a limiter circuit, a circuit for providing a signal related to the phase of the unmodulated intermediate frequency signal, a cosine phase detector, coupled to the limiter circuit and the signal providing circuit for providing a signal proportional to $\cos \emptyset$, and a circuit for dividing the output signal of the synchronous detector by the output signal of the cosine phase detector.
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