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THERMALLY ANNEALED WAFERS HAVING IMPROVED INTERNAL GETTERING

BACKGROUND OF THE INVENTION

The present invention generally relates to the preparation of semiconductor material substrates, especially silicon wafers, which are used in the manufacture of electronic components. More particularly, the present invention relates to a process for the thermal treatment of silicon wafers to dissolve agglomerated vacancy defects and improve internal gettering capabilities, enabling such wafers to form ideal, non-uniform depth distributions of oxygen precipitates during the heat treatment cycles of essentially any arbitrary electronic device manufacturing process.

Single crystal silicon, which is the starting material for most processes for the fabrication of semiconductor electronic components, is commonly prepared with the so-called Czochralski process wherein a single seed crystal is immersed into molten silicon and then grown by slow extraction. As molten silicon is contained in a quartz crucible, it is contaminated with various impurities, among which is mainly oxygen. At the temperature of the silicon molten mass, oxygen comes into the crystal lattice until it reaches a concentration determined by the solubility of oxygen in silicon at the temperature of the molten mass and by the actual segregation coefficient of oxygen in solidified silicon. Such concentrations are greater than the solubility of oxygen in solid silicon at the temperatures typical

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employed in fabrication processes for electronic devices. As the crystal grows from the molten mass and cools, therefore, the solubility of oxygen in it decreases rapidly, whereby in the resulting slices or wafers oxygen is present in supersaturated concentrations.

In addition to oxygen, intrinsic point defects, such as silicon lattice vacancies, may be present in the crystal as it forms. Like oxygen, the solubility of vacancies in the solid silicon is in part temperature dependent. As the silicon crystal cools, at some point the crystal may become critically supersaturated with vacancies, resulting in the formation of agglomerated vacancy defects. Agglomerated vacancy defects are recognized to be the origin of such observable crystal defects as D-defects, Flow Pattern Defects (FPDs), Gate Oxide Integrity (GOI) Defects, Crystal Originated Particle (COP) Defects, and crystal originated Light Point Defects (LPDs), as well as certain classes of bulk defects observed by infrared light scattering techniques such as Scanning Infrared Microscopy and Laser Scanning Tomography. Agglomerated vacancy defects are recognized to be a hindrance to the performance of electronic devices manufactured from wafers containing them.

The thermal treatment cycles typically employed in the fabrication of electronic devices can cause the precipitation of oxygen in silicon wafers which are supersaturated in oxygen. Like the agglomeration of vacancy defects, the precipitation of oxygen may also act to hinder device performance, depending upon the location within the wafer at which precipitation occurs. For example, oxygen precipitates located in the active device

region of the wafer can impair the operation of the device. In contrast, oxygen precipitates located in the bulk of the wafer are advantageous because they are capable of trapping undesired metal impurities that may come into contact with the wafer. The use of oxygen precipitates located in the bulk of the wafer to trap metals is commonly referred to as internal or intrinsic gettering ("IG").

A number of approaches have been suggested as to how agglomerated defects may be prevented from forming, or eliminated once formed. For example, the dissolution or annihilation of agglomerated intrinsic point defects may generally be achieved using high temperature heat treatments of the silicon in wafer form. (See, e.g., Fusegawa et al., European Patent Application 503,816 A1 and S. Nadahara et al., "Hydrogen Annealed Silicon Wafer," Solid State Phenomena, vols. 57-58, pp. 19-26 (1997).) However, while these approaches may have the desirable effect of dissolving agglomerated defects in the near surface region of the wafer, they may also result in the dissolution of oxygen precipitates in the bulk of the wafer, causing internal gettering capabilities to be lost.

Accordingly, a need continues to exist for a process wherein agglomerated intrinsic point defects may be dissolved or annihilated from a silicon wafer, and yet still afford a wafer possessing the beneficial characteristics of internal gettering.

SUMMARY OF THE INVENTION

Among the objects of the invention, therefore, is the provision of a single crystal silicon wafer which, during the heat treatment cycles of essentially any electronic device manufacturing process, will form an ideal, non-uniform depth distribution of oxygen precipitates; the provision of such a wafer which will optimally and reproducibly form a denuded zone of sufficient depth and a sufficient density of oxygen precipitates in the wafer bulk; the provision of such a wafer in which the formation of the denuded zone and the formation of the oxygen precipitates in the wafer bulk is not dependant upon differences in oxygen concentration in these regions of the wafer; the provision of such a wafer in which the thickness of the resulting denuded zone is essentially independent of the details of the IC manufacturing process sequence; the provision of such a wafer in which the formation of the denuded zone and the formation of the oxygen precipitates in the wafer bulk is not influenced by the thermal history and the oxygen concentration of the Czochralski-grown, single crystal silicon ingot from which the silicon wafer is sliced; the provision of such a process in which the formation of the denuded zone does not depend upon the out-diffusion of oxygen; and, the provision of such a process in which the concentration of agglomerated vacancy defects is substantially reduced in a surface layer of the wafer.

Briefly, therefore, the present invention is directed to a single crystal silicon wafer having two major, generally parallel surfaces, one of which is the front surface of the wafer and the other of which is the back surface of the wafer, a central plane between the front and back surfaces, a circumferential edge joining the front and back surfaces, a stratum extending from the front surface to a distance, D_s, as measured from the front surface and toward the central plane, a surface layer which at least in part is coextensive with the stratum and which

comprises the region of the wafer between the front surface and a distance, D_1, of at least about 10 micrometers, as measured from the front surface and toward the central plane, and a bulk layer which comprises the region of the wafer between the central plane and the surface layer, the wafer being characterized in that

the wafer stratum is substantially free of agglomerated vacancy defects;

the bulk layer contains agglomerated vacancy defects; and,

the wafer has a non-uniform distribution of crystal lattice vacancies with the concentration of vacancies in the bulk layer being greater than the concentration of vacancies in the surface layer and with the vacancies having a concentration profile in which the peak density of the vacancies is at or near the central plane, the concentration generally decreasing from the position of peak density in the direction of the front surface of the wafer.

The present invention is further directed to a process for heat-treating a single crystal silicon wafer to dissolve agglomerated vacancy defects and to influence the precipitation behavior of oxygen in the wafer in a subsequent thermal processing step, the silicon wafer having two major, generally parallel surfaces, one of which is the front surface of the wafer and the other of which is the back surface of the wafer, a central plane

between the front and back surfaces, a circumferential edge joining the front and back surfaces, a stratum extending from the front surface to a distance, D_s, as measured from the front surface and toward the central plane, a surface layer which, at least in part is coextensive with the stratum and which comprises the region of the wafer between the front surface and a distance, D, measured from the front surface and toward the central plane, and a bulk layer which comprises the region of the wafer between the central plane and the surface layer. The process comprises thermally annealing the wafer in an atmosphere to dissolve pre-existing agglomerated vacancy defects in the stratum, heat-treating the annealed wafer to form crystal lattice vacancies in the surface and bulk layers, and then controlling the cooling rate of the heat-treated wafer to produce a wafer having a vacancy concentration profile in which the peak density is at or near the central plane with the concentration generally decreasing in the direction of the front surface of the wafer, the difference in the concentration of vacancies in the surface and bulk layers being such that a thermal treatment of the wafer at a temperature in excess of 750 °C is capable of forming a denuded zone in the surface layer and oxygen clusters or precipitates in the bulk layer with the concentration of the oxygen clusters or precipitates in the bulk layer being primarily dependant upon the concentration of vacancies.

The present invention is further directed to a process for heat-treating a single crystal silicon wafer to dissolve agglomerated vacancy defects and to influence

the precipitation behavior of oxygen in the wafer in a subsequent thermal processing step, the silicon wafer having a front surface, a back surface, a central plane between the front and back surfaces, a stratum extending from the front surface to a distance, D_s, as measured from the front surface and toward the central plane, a surface layer which at least in part is coextensive with the stratum and which comprises the region of the wafer between the front surface and a distance, D, measured from the front surface and toward the central plane, and a bulk layer which comprises the region of the wafer between the central plane and surface layer. The process comprises heat-treating the wafer in an atmosphere to form crystal lattice vacancies in the surface and bulk layers, and then controlling the cooling rate of the heat-treated wafer to produce a wafer having a vacancy concentration profile in which the peak density is at or near the central plane with the concentration generally decreasing in the direction of the front surface of the wafer and the difference in the concentration of vacancies in the surface and bulk layers being such that a thermal treatment of the wafer at a temperature in excess of 750 °C is capable of forming a denuded zone in the surface layer and oxygen clusters or precipitates in the bulk layer with the concentration of the oxygen clusters or precipitates in the bulk layer being primarily dependant upon the concentration of vacancies. Oxygen precipitate nucleation centers present in the cooled wafer are stabilized by heating the cooled wafer to a temperature of about 650 to about 850 °C for about 1 hour to about 4 hours, and then the stabilized wafer is

thermally annealed in an atmosphere to dissolve agglomerated vacancy defects present within a region extending from the front surface to a depth of at least about 5 microns.

Other objects and features of this invention will be in part apparent and in part pointed out hereinafter.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic depiction of the ideal precipitating wafer process of the present invention.

Fig. 2 is a photograph of a cross-section of a wafer (sample 4-7) which was processed as described in Example 1.

Fig. 3 is a photograph of a cross-section of a wafer (sample 4-8) which was subjected to the series of steps described in Example 1.

Fig. 4 is a photograph of a cross-section of a wafer (sample 3-14) which was subjected to the series of steps described in Example 1.

Fig. 5 is a graph of the log of platinum concentration (atoms/cm^3) versus depth from the surface of a wafer (sample 4-7) which was subjected to the series of steps set forth in Example 1.

Fig. 6 is a photograph of a cross-section of a wafer (sample 3-4) which was subjected to the series of steps set forth in Example 2.

Fig. 7 is a photograph of a cross-section of a wafer (sample 3-5) which was subjected to the series of steps set forth in Example 2.

Fig. 8 is a photograph of a cross-section of a wafer (sample 3-6) which was subjected to the series of steps set forth in Example 2.

Fig. 9 is a photograph of a cross-section of a wafer (sample 1-8) which was subjected to the series of steps set forth in Example 3.

FIG. 10 is logarithmic graph of the number density of bulk microdefects (BMD) versus the partial pressure of oxygen present in the atmosphere during rapid thermal annealing of single crystal silicon wafers in accordance with the present invention, as described in Example 4.

FIG. 11 is a photograph taken under magnification of a cross-section of a wafer (white background) which has been thermally annealed, in accordance with the present process, in a nitriding atmosphere in the absence of an enhanced oxide layer, following an NEC-1 treatment.

FIG. 12 is a photograph, taken under greater magnification than in Fig. 11, of a portion of the wafer cross-section shown in FIG. 11, showing in detail the essential absence of a denuded zone.

FIG. 13 is a photograph taken under magnification of a cross-section of a wafer (white background) which has been thermally annealed, in accordance with the present invention, in a nitriding atmosphere in the absence of an enhanced oxide layer and which was subsequently subjected to a thermal oxidation treatment.

FIG. 14 is a photograph, taken under greater magnification than in Fig. 13, of a portion of the wafer cross-section shown in FIG. 13, showing in detail the presence of a denuded zone.

FIG. 15 is a photograph taken under magnification of a cross-section of a wafer (white background) which has been thermally annealed, in accordance with the present invention, in a nitriding atmosphere in the absence of an enhanced oxide layer and which was subsequently subjected to a thermal oxidation treatment on only one side of the wafer.

FIG. 16 is a photograph, taken under greater magnification than in Fig. 15, of a portion of the wafer cross-section shown in FIG. 15, showing in detail the essential absence of a denuded zone on the shielded side of the wafer.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The process of the present invention affords the means by which to obtain a single crystal silicon wafer having a reduced concentration of agglomerated vacancy defects, as compared to the initial concentration of such defects, in a surface layer of the wafer. Additionally, the present process yields a wafer which is "ideally precipitating"; that is, a wafer which, during essentially any electronic device manufacturing process, will form a denuded zone of sufficient depth and a wafer bulk containing a sufficient density of oxygen precipitates for IG purposes. The process of the present invention acts to annihilate existing agglomerated vacancy defects in this surface layer, while creating a "template" in the silicon which determines or "prints" the manner in which oxygen will precipitate during an electronic device manufacturing process

In accordance with a first embodiment of the process of the present invention, a single crystal silicon wafer is initially subjected a thermal anneal, the temperature and duration of the anneal, as well as the atmosphere in which the wafer is annealed, are such that agglomerated vacancy defects are effectively annihilated or dissolved within a surface layer or stratum of the wafer. Generally, the conditions for this thermal anneal are those commonly used in the art for dissolving such defects. (See, e.g., Fusegawa et al., European Patent Application 503,816 A1; S. Nadahara et al., "Hydrogen Annealed Silicon Wafer," Solid State Phenomena, vols. 57-58, pp. 19-26 (1997); and, D. Graf et al., "High-Temperature Annealed Silicon Wafers," Electrochemical Society Proceedings, vol. 97-22, pp. 18-25 (1997).) For example, the wafer may be thermally annealed in an argon or hydrogen atmosphere, or a mixture thereof, in order to dissolve agglomerated vacancy defects present in a stratum extending from a surface and toward the center of the wafer.

Generally, the wafer is heated to a temperature for a duration sufficient to dissolve agglomerated vacancy defects present in a stratum extending from the surface to depths, as measured from the surface and toward the center of the wafer, of a few micrometers (i.e., at least about 1, 2, 3, 5, or even 10 micrometers), tens of micrometers (i.e., about 20, 40, 80 or more), hundreds of micrometers (i.e., about 100, 300, 500 microns or more), up to about the center of the wafer. The precise conditions will vary, depending upon the desired depth to which agglomerated vacancy defects are to be dissolved or

reduced in size. For example, the wafer may be heated to a temperature ranging from about 1100°C to about 1300°C for about 1 hour to about 4 hours, or about 1200°C to about 1250 °C for about 2 to about 3 hours.

In this regard, it is to be noted that in addition to the temperature, duration, atmosphere and ramping conditions (i.e., the rate at which the target anneal temperature is reached) of the thermal anneal, the size of the agglomerated defects to be dissolved is a factor in the efficiency of the anneal at removing such defects. Accordingly, the conditions necessary to achieve the desired result may be determined empirically by varying the treatment temperature, time and atmosphere composition for a number of samples. Therefore, the conditions may be other than that herein described without departing from the scope of the present invention.

Subjecting a wafer to this defect dissolving treatment results in the formation of a stratum near the surface of the wafer having a concentration of agglomerated vacancy defects which is reduced, as compared to the concentration of such defects in the starting material. Preferably, however, this surface layer will be substantially free of agglomerated vacancy defects. In this regard, it is to be noted that as used herein the phrase "substantially free of agglomerated vacancy defects" shall mean a concentration of agglomerated defects within the stratum that is less than the detection limit of these defects, which is currently about 10^4 defects/cm^3.

The conditions employed in the agglomerated defect dissolution treatment also results in the dissolution of oxygen precipitate nucleation centers present in the wafer, provided the wafer has not previously been subjected to a stabilizing heat treatment. In order to reestablish these centers, and thus enable the wafer to have an increased density of oxygen precipitates for IG purposes, the wafer is next subjected to a sequence of steps in which a vacancy concentration profile is formed. This portion of the present process effectively acts to determine or "print" the manner in which oxygen will ultimately precipitate within the wafer during an electronic device manufacturing process. Referring now to Fig. 1, wafer 1, having a front surface 3, a back surface 5, and an imaginary central plane 7 between the front and back surfaces, is heat-treated in an oxygen-containing atmosphere in step S_1 of this portion of the present process, in order to grow a superficial oxide layer 9 which envelopes the wafer. In general, the oxide layer will have a thickness which is greater than the native oxide layer which forms upon silicon (about 15 Ångstroms); preferably, the oxide layer has a thickness of at least about 20 Ångstroms and, in some embodiments, at least about 25 Ångstroms or even at least about 30 Ångstroms. Experimental evidence obtained to-date, however, suggests that oxide layers having a thickness greater than about 30 Ångstroms, while not interfering with the desired effect, provide little or no additional benefit.

It is to be noted that the terms "front" and "back" in this context are used to distinguish the two major,

generally planar surfaces of the wafer; the front surface of the wafer, as that term is used herein, is not necessarily the surface onto which an electronic device will subsequently be fabricated nor is the back surface of the wafer as that term is used herein necessarily the major surface of the wafer which is opposite the surface onto which the electronic device is fabricated. In addition, because silicon wafers typically have some total thickness variation (TTV), warp and bow, the midpoint between every point on the front surface and every point on the back surface may not precisely fall within a plane; as a practical matter, however, the TTV, warp and bow are typically so slight that to a close approximation the midpoints can be said to fall within an imaginary central plane which is approximately equidistant between the front and back surfaces.

In step S_2 of the precipitation portion of the present process, the wafer 1 is subjected to a heat-treatment step in which the wafer is heated to an elevated temperature to form and thereby increase the number density of crystal lattice vacancies 13 in the wafer. Preferably, this heat-treatment step is carried out in a rapid thermal annealer in which the wafers are rapidly heated to a target temperature and annealed at that temperature for a relatively short period of time. In general, the wafer is subjected to a temperature in excess of about 1150 °C, preferably at least about 1175 °C, more preferably at least about 1200 °C, and most preferably between about 1200 °C and about 1275 °C.

In a first embodiment of the precipitation portion of the present process, the rapid thermal annealing step

is carried out in the presence of a nitriding atmosphere; that is, the anneal is carried out in an atmosphere containing nitrogen gas (N_2) or a nitrogen-containing compound gas, such as ammonia, which is capable of nitriding an exposed silicon surface. The atmosphere may thus consist entirely of nitrogen or nitrogen compound gas, or it may additionally comprise a non-nitriding gas such as argon. An increase in vacancy concentration throughout the wafer is achieved nearly, if not immediately, upon achieving the annealing temperature. The wafer will generally be maintained at this temperature for at least one second, typically for at least several seconds (e.g., at least 3), preferably for several tens of seconds (e.g., 20, 30, 40, or 50 seconds) and, depending upon the desired characteristics of the wafer, for a period which may range up to about 60 seconds (which is near the limit for commercially available rapid thermal annealers). The resulting wafer will have a relatively uniform vacancy concentration (number density) profile in the wafer.

Based upon experimental evidence obtained to-date, the atmosphere in which the rapid thermal annealing step is carried out preferably has no more than a relatively small partial pressure of oxygen, water vapor and other oxidizing gases; that is, the atmosphere has a total absence of oxidizing gases or a partial pressure of such gases which is insufficient to inject sufficient quantities of silicon self-interstitial atoms which suppress the build-up of vacancy concentrations. While the lower limit of oxidizing gas concentration has not been precisely determined, it has been demonstrated that

for partial pressures of oxygen of 0.01 atmospheres (atm.), or 10,000 parts per million atomic (ppma), no increase in vacancy concentration and no effect is observed. Thus, it is preferred that the atmosphere have a partial pressure of oxygen and other oxidizing gases of less than 0.01 atm. (10,000 ppma); more preferably the partial pressure of these gases in the atmosphere is no more than about 0.005 atm. (5,000 ppma), more preferably no more than about 0.002 atm. (2,000 ppma), and most preferably no more than about 0.001 atm. (1,000 ppma).

In addition to causing the formation of crystal lattice vacancies, the rapid thermal annealing step causes the dissolution of any unstabilized oxygen precipitate nucleation centers which are present in the silicon starting material. These nucleation centers may be formed, for example, during the growth of the single crystal silicon ingot from which the wafer was sliced, or as a consequence of some other event in the previous thermal history of the wafer or of the ingot from which the wafer is sliced. Thus, the presence or absence of these nucleation centers in the starting material is not critical, provided these centers are capable of being dissolved during the rapid thermal annealing step.

The rapid thermal anneal may be carried out in any of a number of commercially available rapid thermal annealing ("RTA") furnaces in which wafers are individually heated by banks of high power lamps. RTA furnaces are capable of rapidly heating a silicon wafer, e.g., they are capable of heating a wafer from room temperature to 1200 °C in a few seconds. One such

commercially available RTA furnace is the model 610 furnace available from AG Associates (Mountain View, CA).

Intrinsic point defects (vacancies and silicon self-interstitials) are capable of diffusing through single crystal silicon with the rate of diffusion being temperature dependant. The concentration profile of intrinsic point defects, therefore, is a function of the diffusivity of the intrinsic point defects and the recombination rate as a function of temperature. For example, the intrinsic point defects are relatively mobile at temperatures in the vicinity of the temperature at which the wafer is annealed in the rapid thermal annealing step, whereas they are essentially immobile for any commercially practical time period at temperatures of as much as 700 °C. Experimental evidence obtained to-date suggests that the effective diffusion rate of vacancies slows considerably at temperatures less than about 700 °C and perhaps as great as 800 °C, 900 °C, or even 1,000 °C, the vacancies can be considered to be immobile for any commercially practical time period.

Upon completion of step S_2, the wafer is rapidly cooled in step S_3 through the range of temperatures at which crystal lattice vacancies are relatively mobile in the single crystal silicon. As the temperature of the wafer is decreased through this range of temperatures, the vacancies diffuse to the oxide layer 9 and are annihilated, thus leading to a change in the vacancy concentration profile with the extent of change depending upon the length of time the wafer is maintained at a temperature within this range. If the wafer were held at this temperature within this range for an infinite period

of time, the vacancy concentration would once again become substantially uniform throughout wafer bulk 11 with the concentration being an equilibrium value which is substantially less than the concentration of crystal lattice vacancies immediately upon completion of the heat treatment step. By rapidly cooling the wafer, however, a non-uniform distribution of crystal lattice vacancies can be achieved with the maximum vacancy concentration being at or near central plane 7 and the vacancy concentration decreasing in the direction of the front surface 3 and back surface 5 of the wafer. In general, the average cooling rate within this range of temperatures is at least about 5 °C per second and preferably at least about 20 °C per second. Depending upon the desired depth of the denuded zone, the average cooling rate may preferably be at least about 50 °C per second, still more preferably at least about 100 °C per second, with cooling rates in the range of about 100 °C to about 200 °C per second being presently preferred for some applications. Once the wafer is cooled to a temperature outside the range of temperatures at which crystal lattice vacancies are relatively mobile in the single crystal silicon, the cooling rate does not appear to significantly influence the precipitating characteristics of the wafer and thus, does not appear to be narrowly critical. Conveniently, the cooling step may be carried out in the same atmosphere in which the heating step is carried out.

In step S_4 of the precipitation portion of the present process, the wafer is subjected to an oxygen precipitation heat-treatment. For example, the wafer may be annealed at a temperature of 800 °C for four hours and

then at a temperature of 1000 °C for sixteen hours. Alternatively and preferably, the wafer is loaded into a furnace which is at a temperature of about 800 °C as the first step of an electronic device manufacturing process. When loaded into a furnace at this temperature, the previously rapidly thermal annealed wafer will have separate zones which behave differently with respect to oxygen precipitation. In the high vacancy regions (the wafer bulk), oxygen clusters rapidly as the wafer enters the furnace. By the time the loading temperature is reached, the clustering process is finished and a distribution of clusters is reached which depends only upon the initial concentration of vacancies. In the low vacancy regions (near the wafer surfaces), the wafer behaves like a normal wafer which lacks pre-existing oxygen precipitate nucleation centers; that is, oxygen clustering is not observed. As the temperature is increased above 800 °C or if the temperature remains constant, the clusters in the vacancy rich zone grow into precipitates and are thereby consumed, whereas in the vacancy lean zone nothing happens. By dividing the wafer into various zones of vacancy concentration, a template is effectively created through which is written an oxygen precipitate pattern which is fixed the moment the wafer is loaded into the furnace.

As illustrated in Fig. 1, the resulting depth distribution of oxygen precipitates in the wafer is characterized by clear regions of oxygen precipitate-free material (denuded zones) 15 and 15' extending from the front surface 3 and back surface 5 to a depth t, t', respectively. Between the oxygen precipitate-free

regions, 15 and 15', there is a region 17 which contains a substantially uniform density of oxygen precipitates.

The concentration of oxygen precipitates in region 17 is primarily a function of the heating step and secondarily a function of the cooling rate. In general, the concentration of oxygen precipitates increases with increasing temperature and increasing annealing times in the heating step, with precipitate densities in the range of about 1×10^7 to about 5×10^{10} precipitates/cm^3 being routinely obtained.

The depth t, t' from the front and back surfaces, respectively, of oxygen precipitate-free material (denuded zones) 15 and 15' is primarily a function of the cooling rate through the temperature range at which crystal lattice vacancies are relatively mobile in silicon. In general, the depth t, t' increases with decreasing cooling rates, with denuded zone depths of at least about 10, 20, 30, 40, 50, 70 or even 100 micrometers being attainable. Significantly, the depth of the denuded zone is essentially independent of the details of the electronic device manufacturing process and, in addition, does not depend upon the out-diffusion of oxygen as is conventionally practiced.

While the rapid thermal treatments may result in the out-diffusion of a small amount of oxygen from the surface of the front and back surfaces of the wafer, the amount of out-diffusion is significantly less than what is observed in conventional processes for the formation of denuded zones. As a result, an "ideal precipitating wafer" is formed having a substantially uniform interstitial oxygen concentration as a function of

distance from the silicon surface. For example, prior to the oxygen precipitation heat-treatment (S_4), the wafer will have a substantially uniform concentration of interstitial oxygen from the center of the wafer to regions of the wafer which are within about 15 microns of the silicon surface, more preferably from the center of the silicon to regions of the wafer which are within about 10 microns of the silicon surface, even more preferably from the center of the silicon to regions of the wafer which are within about 5 microns of the silicon surface, and most preferably from the center of the silicon to regions of the wafer which are within about 3 microns of the silicon surface. In this context, a substantially uniform oxygen concentration shall mean a variance in the oxygen concentration of no more than about 50%, preferably no more than about 20%, and most preferably no more than about 10%.

Typically, oxygen precipitation heat-treatments do not result in a substantial amount of oxygen outdiffusion from the heat-treated wafer. As a result, the concentration of interstitial oxygen in the denuded zone at distances more than several microns from the wafer surface will not significantly change as a consequence of the precipitation heat-treatment. For example, if the denuded zone of the wafer consists of the region of the wafer between the surface of the silicon and a distance, D_1 (which is at least about 10 micrometers) as measured from the front surface and toward the central plane, the oxygen concentration at a position within the denuded zone which is at a distance from the silicon surface equal to one-half of D_1 will typically be at least about

75% of the peak concentration of the interstitial oxygen concentration anywhere in the denuded zone. For some oxygen precipitation heat-treatments, the interstitial oxygen concentration at this position will be even greater, i.e., at least 80%, 85%, 90% or even 95% of the maximum oxygen concentration anywhere in the denuded zone.

In a second embodiment of the precipitation portion of the present process, a non-nitriding atmosphere is used instead of the nitriding atmosphere used in the heating (rapid thermal annealing) and cooling steps of the first embodiment. Suitable non-nitriding atmospheres include argon, helium, neon, carbon dioxide, and other such non-oxidizing, non-nitriding elemental and compound gases, or mixtures of such gases. The non-nitriding atmosphere, like the nitriding atmosphere, may contain a relatively small partial pressure of oxygen, i.e., a partial pressure less than 0.01 atm. (10,000 ppma), more preferably less than 0.005 atm. (5,000 ppma), more preferably less than 0.002 atm. (2,000 ppma), and most preferably less than 0.001 atm. (1,000 ppma).

In a third embodiment of the precipitation portion of the present process, step S_1 (the thermal oxidation step) is omitted and the starting wafer has no more than a native oxide layer. When such a wafer is annealed in a nitrogen atmosphere, however, the effect differs from that which is observed when a wafer having an oxide layer which is greater in thickness than a native oxide layer ("enhanced oxide layer") is annealed in nitrogen. When the wafer containing an enhanced oxide layer is annealed in a nitrogen atmosphere, a substantially uniform

increase in the vacancy concentration is achieved throughout the wafer nearly, if not immediately, upon reaching the annealing temperature; furthermore, the vacancy concentration does not appear to significantly increase as a function of annealing time at a given annealing temperature. If the wafer lacks anything more than a native oxide layer and if the front and back surfaces of the wafer are annealed in nitrogen, however, the resulting wafer will have a vacancy concentration (number density) profile which is generally "U-shaped" for a cross-section of the wafer; that is, a maximum concentration will occur at or within several micrometers of the front and back surfaces and a relatively constant and lesser concentration will occur throughout the wafer bulk with the minimum concentration in the wafer bulk initially being approximately equal to the concentration which is obtained in wafers having an enhanced oxide layer. Furthermore, an increase in annealing time will result in an increase in vacancy concentration in wafers lacking anything more than a native oxide layer.

Experimental evidence further suggests that this difference in behavior for wafers having no more than a native oxide layer and wafers having an enhanced oxide layer can be avoided by including molecular oxygen or another oxidizing gas in the atmosphere. Stated another way, when wafers having no more than a native oxide layer are annealed in a nitrogen atmosphere containing a small partial pressure of oxygen, the wafer behaves the same as a wafer having an enhanced oxide layer. Without being bound to any theory, it appears that a superficial oxide layer, which is greater in thickness than a native oxide

layer, serves as a shield which inhibits nitridization of the silicon. This enhanced oxide layer may thus be present on the starting wafer or it may be formed in situ by growing this layer during the annealing step.

In accordance with this third embodiment of the precipitation portion of the present process, therefore, the atmosphere during the rapid thermal annealing step preferably contains a partial pressure of at least about 0.0001 atm. (100 ppma), more preferably a partial pressure of at least about 0.0002 atm. (200 ppma). For the reasons previously discussed, however, the partial pressure of oxygen preferably does not exceed 0.01 atm. (10,000 ppma), and is more preferably less than 0.005 atm. (5,000 ppma), still more preferably less than 0.002 atm. (2,000 ppma), and most preferably less than 0.001 atm. (1,000 ppma).

However, it is to be noted that as an alternative to utilizing an atmosphere having a partial pressure of oxygen, the silicon wafer may simply be subjected to a thermal anneal, or rapid thermal anneal, treatment under an oxygen atmosphere after annealing under a nitrogen atmosphere or a neutral atmosphere, in accordance with step S_2, is complete. The oxygen annealing step may be performed after the wafer has been allowed to cool or, alternatively, may be performed at temperature (i.e., while the wafer is still hot after the initial thermal anneal step has been completed). Furthermore, this oxygen anneal step may optionally be performed for any of the above-described embodiments as a means by which to further tailor or profile the vacancy concentration

within the silicon wafer and, as such, the resulting oxygen precipitate pattern in the wafer.

Without being held to any particular theory, it is believed that oxygen annealing results in the oxidation of the silicon surface and, as a result, acts to create an inward flux of silicon self-interstitials. This inward flux of self-interstitials has the effect of gradually altering the vacancy concentration profile by causing recombinations to occur, beginning at the surface and then moving inward. A region of low vacancy concentration may therefore be created which, following an oxygen precipitation heat treatment, results in a denuded zone having a depth optimized for the particular end use of the device which is to be fabricated from the silicon wafer.

For silicon wafers having the peak concentration of vacancies within the bulk 17 of the silicon wafer, the depths t and t' of regions 15 and 15', respectively, may be selectively increased by controlling the rate at which oxidation of the surfaces occurs. The rate of oxidation is in turn dependent upon a number of factors, such as the atmospheric conditions, temperature and duration of this oxidation step. For example, the rate of oxidation will increase as the concentration of oxygen in the atmosphere increases, with the rate being greatest when pyrogenic steam is employed.

It is to be noted that the precise conditions for the oxidative treatment may be empirically determined by adjusting the temperature and duration of the anneal, and the atmospheric conditions (i.e., the composition of the atmosphere, as well as the oxygen partial pressure) in

order to optimize the depths t and/or t'. However, if something other than pure oxygen or pyrogenic steam is employed in the present process, preferable the partial pressure of oxygen in the atmosphere will be at least about 0.0001 (100 ppma), more preferably at least about 0.0002 (200 ppma), still more preferably at least about 0.0004 (400 ppma), and still more preferably at least about 0.0008 (800 ppma). In this regard it is to be noted that the limitations placed upon the oxygen content, or partial pressure, for the thermal anneal step S_2 are not applicable for this optional step of the precipitation process. Furthermore, if the peak concentration of vacancies for region 17 is to be substantially retained, the temperature of this oxidative treatment is preferably in excess of about 1150°C. More preferably, the temperature is at least about equal to the temperature employed during the thermal treatment of step S_2. Without being held to any particular theory, it is believed that if the temperature is less than that employed during the thermal treatment, the peak concentration of vacancies in region 17 may actually decrease because of the direct recombination of vacancies and self-interstitials.

Once the oxidative treatment has been completed, the wafer may be rapidly cooled, as in step S_3 above, through the range of temperatures at which crystal lattice vacancies are relatively mobile in the single crystal silicon. By rapidly cooling the wafer, the vacancy concentration profile is effectively "frozen" within the silicon matrix, thus establishing a non-uniform distribution of crystal lattice vacancies. It is

therefore desirable to cool at an average rate within this range of temperatures of at least about 5 °C per second, in order to avoid the vacancy concentration profile which has been established from being lost or erased. Preferably, however, the cooling rate is at least about 20 °C per second. It is to be noted that as the cooling rate is changed, the resulting profile may be further modified. Accordingly, depending upon the desired profile to be obtained, the average cooling rate may be at least about 50 °C per second, about 100 °C per second, or up to about 200 °C per second or more.

Once the wafer is cooled to a temperature outside the range of temperatures at which crystal lattice vacancies are relatively mobile in the single crystal silicon, the cooling rate does not appear to significantly influence the precipitating characteristics of the wafer and thus, does not appear to be narrowly critical. Conveniently, the cooling step may be carried out in the same atmosphere in which the heating step is carried out.

The separate oxidative treatment is an acceptable alternative to controlling the vacancy concentration profile by means of adjusting the rate of cooling, as described in detail above. Accordingly, when this oxidative treatment is employed the cooling rate of step S_4 may be greater than that herein described. In addition, it is to be noted that this oxidative treatment is preferred when the desired depths of t or t' are in excess of tens of micrometers, several tens of micrometers, or more.

It is to be further noted that the flexibility offered by the oxidative treatment enables this approach to be successfully performed on a wafer having a vacancy concentration (number density) profile which is generally "U-shaped." More specifically, as noted above, if a wafer having only a native oxide layer on the wafer surface is subjected to the thermal anneal step S_2, the resulting wafer will possess a vacancy profile which is generally "U-shaped." By subjecting such a wafer to this oxidative anneal treatment, the vacancy concentration profile may be altered, the exposure conditions being selectively determined in order to yield a desired vacancy profile which comports with present invention.

In other embodiments of the precipitation process, the front and back surfaces of the wafer may be exposed to different atmospheres, each of which may contain one or more nitriding or non-nitriding gases. For example, the back surface of the wafer may be exposed to a nitriding atmosphere as the front surface is exposed to a non-nitriding atmosphere. Alternatively, multiple wafers (e.g., 2, 3 or more wafers) may be simultaneously annealed while being stacked in face-to-face arrangement; when annealed in this manner, the faces which are in face-to-face contact are mechanically shielded from the atmosphere during the annealing. Alternatively, and depending upon the atmosphere employed during the rapid thermal annealing step and the desired oxygen precipitation profile of the wafer, the oxide layer may be formed only upon the side of the wafer at which the denuded zone is desired, e.g., front surface 3 of the wafer (see Fig. 1).

It is to be noted that, alternatively, the precipitation process may be performed on the silicon wafer prior to thermally annealing the wafer to dissolve agglomerated vacancy defects. However, if such an approach is employed, it is preferred that the wafer be subjected to a stabilizing heat treatment prior to being subjected to the defect dissolving treatment. For example, the wafer may be heated to a temperature within the range of about 400 to about 850°C for a period sufficient to impart the stability necessary to withstand the temperature of the defect dissolving treatment. In this regard, it is to be noted that greater stabilization is imparted as the duration of the heat treatment increases. Accordingly, durations of 20, 40, 60 or more minutes, up to 2, 3 or 4 hours or more, may be necessary depending upon the conditions of the defect dissolving treatment to be used. For example, a typical set of conditions employed for stabilization include heating the wafer to a temperature between about 650 and about 850 °C for about 1 to about 4 hours.

If a heat treatment sufficient to stability oxygen precipitate nucleation centers is employed, then oxygen precipitates may optionally be formed directly during the defect dissolution treatment; that is, the oxygen precipitation step S_4 may be replaced by the defect dissolving treatment. Alternatively, if desired the oxygen precipitation heat treatment, such as that referred to above for step S_4, may be completed prior to initiating the defect dissolving step.

The starting material for the process of the present invention is a single crystal silicon wafer which has

been sliced from a single crystal ingot grown in accordance with conventional Czochralski crystal growing methods. Such methods, as well as standard silicon slicing, lapping, etching, and polishing techniques are disclosed, for example, in F. Shimura, Semiconductor Silicon Crystal Technology, Academic Press, 1989, and Silicon Chemical Etching, (J. Grabmaier ed.) Springer-Verlag, New York, 1982 (incorporated herein by reference). The silicon wafer may be a polished or, alternatively, it may be lapped and etched but not polished. In addition, the wafer may have vacancy or self-interstitial point defects as the predominant intrinsic point defect. For example, the wafer may be vacancy dominated from center to edge, self-interstitial dominated from center to edge, or it may contain a central core of vacancy of dominated material surrounded by an axially symmetric ring of self-interstitial dominated material.

Czochralski-grown silicon typically has an oxygen concentration within the range of about 5×10^{17} to about 9×10^{17} atoms/cm^3 (ASTM standard F-121-83). Because the oxygen precipitation behavior of the wafer becomes essentially decoupled from the oxygen concentration in the present process, the starting wafer may have an oxygen concentration falling anywhere within or even outside the range attainable by the Czochralski process.

Depending upon the cooling rate of the single crystal silicon ingot from the temperature of the melting point of silicon (about 1410 °C) through the range of about 750 °C to about 350 °C, oxygen precipitate nucleation centers may form in the single crystal silicon

ingot from which the wafer is sliced. The presence or absence of these nucleation centers in the starting material is not critical to the present invention provided, however, these centers are capable of being dissolved by heat-treating the silicon at temperatures not in excess of about 1300 °C. Certain heat-treatments, such as annealing the silicon at a temperature of about 800 °C for about four hours, can stabilize these centers such that they are incapable of being dissolved at temperatures not in excess of about 1150 °C. The detection limit for oxygen precipitates is currently about 5 x 10^6 precipitates/cm^3. The presence (or density) of oxygen precipitation nucleation centers cannot be directly measured using presently available techniques. Various techniques may be used, however, to indirectly detect their presence. As previously discussed, preexisting oxygen precipitate nucleation centers in the silicon can be stabilized and precipitates can be grown at these sites by subjecting the silicon to an oxygen precipitation heat treatment. Thus, the presence of these nucleation centers can indirectly be measured after an oxygen precipitation heat treatment, e.g., annealing the wafer at a temperature of 800° C for four hours and then at a temperature of 1000° C for sixteen hours.

Substitutional carbon, when present as an impurity in single crystal silicon, has the ability to catalyze the formation of oxygen precipitate nucleation centers. For this and other reasons, therefore, it is preferred that the single crystal silicon starting material have a low concentration of carbon. That is, the single crystal silicon should have a concentration of carbon which is

less than about 5 x 10^{16} atoms/cm^3, preferably which is less than 1 x 10^{16} atoms/cm^3, and more preferably less than 5 x 10^{15} atoms/cm^3.

If an epitaxial layer is to be deposited upon a wafer prepared in accordance with the present invention, the present process may be carried out either before or after epitaxial deposition. If carried out before, it may be desirable to stabilize the oxygen precipitate nucleation centers in the wafer after the process of the present invention and before the epitaxial deposition. If carried out after, it may be desirable to carry out the process of the present invention in the epitaxial reactor immediately after the epitaxial deposition, provided the cooling rates required by the process of the present invention can be achieved.

The measurement of crystal lattice vacancies in single crystal silicon can be carried out by platinum diffusion analysis. In general, platinum is deposited on the samples and diffused in a horizontal surface with the diffusion time and temperature preferably being selected such that the Frank-Turnbull mechanism dominates the platinum diffusion, but which is sufficient to reach the steady-state of vacancy decoration by platinum atoms. For wafers having vacancy concentrations which are typical for the present invention, a diffusion time and temperature of 730 °C for 20 minutes may be used, although more accurate tracking appears to be attainable at a lesser temperature, e.g., about 680 °C. In addition, to minimize a possible influence by silicidation processes, the platinum deposition method preferably results in a surface concentration of less

than one monolayer. Platinum diffusion techniques are described elsewhere, for example, by Jacob et al., J. Appl. Phys., vol. 82, p. 182 (1997); Zimmermann and Ryssel, "The Modeling of Platinum Diffusion In Silicon Under Non-Equilibrium Conditions," J. Electrochemical Society, vol. 139, p. 256 (1992); Zimmermann, Goesele, Seilenthal and Eichiner, "Vacancy Concentration Wafer Mapping In Silicon," Journal of Crystal Growth, vol. 129, p. 582 (1993); Zimmermann and Falster, "Investigation Of The Nucleation of Oxygen Precipitates in Czochralski Silicon At An Early Stage," Appl. Phys. Lett., vol. 60, p. 3250 (1992); and Zimmermann and Ryssel, Appl. Phys. A, vol. 55, p. 121 (1992).

Examples 1 through 5 illustrate the precipitation portion of the present invention. These Examples should therefore not be interpreted in a limiting sense.

EXAMPLE 1

Silicon single crystals were pulled by the Czochralski method, sliced and polished to form silicon wafers. These wafers were then subjected to a surface oxidation step (S_1), rapid thermal annealing step in nitrogen or argon (S_2), rapidly cooled (S_3), and subjected to an oxygen stabilization and growth step (S_4) under the conditions set forth in Table I. The initial oxygen concentration of the wafers (O_i) before steps S_1 - S_4, the oxygen precipitate density in the bulk of the wafers after step S_4 (OPD), and the depth of the denuded zone after step S_4 (DZ) are also reported in Table I.

TABLE I

Sample	4-7	4-8	3-14
S_1	15 min at 1,000°C in N_2 + ~1% O_2	15 min at 1,000°C in N_2 + ~1% O_2	none
S_2	35 seconds at 1250°C in N_2	35 seconds at 1250°C in Ar	35 seconds at 1250°C in N_2
S_3	100°C/sec	100°C/sec	100°C/sec
S_4	4 hr at 800°C + 16 hr at 1,000°C in N_2	4 hr at 800°C + 16 hr at 1,000°C in N_2	4 hr at 800°C + 16 hr at 1,000°C in N_2
O_i (atoms/cm^3)	$7x10^{17}$	6.67×10^{17}	$7.2x10^{17}$
OPD (atoms/cm^3)	$1x10^{10}$	$4.4x10^{9}$	$1.69x10^{10}$
DZ (depth in μm)	70	95	0

Figures 2, 3, and 4 show cross-sections of the resulting wafers (these figures are enlargements of photographs taken at a magnification of 200X); sample 4-7 is shown in Fig. 2, sample 4-8 is shown in Fig. 3, and sample 3-14 is shown in Fig. 4.

In addition, the concentration of crystal lattice vacancies in the sample 4-7 was mapped using a platinum diffusion technique. A plot of platinum concentration

versus depth from the surface of the wafer (a depth of 0 micrometers corresponding to the front side of the wafer) appears in Fig. 5.

EXAMPLE 2

To demonstrate that the precipitation portion of the process of the present invention is relatively independent of oxygen concentration for Czochralski-grown silicon wafers, three wafers having different oxygen concentrations were subjected to the same series of steps described in Example 1. The conditions for each of these steps, the initial oxygen concentration of the wafers (O_i) before steps S_1 - S_4, the oxygen precipitate density (OPD) in the bulk of the wafers after step S_4, and the depth of the denuded zone (DZ) after step S_4 as measured from the surface of the wafer are reported in Table II. Figures 6, 7, and 8 show cross-sections of the resulting wafers (these figures are enlargements of photographs taken at a magnification of 200X); sample 3-4 is shown in Fig. 6, sample 3-5 is shown in Fig. 7, and sample 3-6 is shown in Fig. 8.

TABLE II

Sample	3-4	3-5	3-6
S_1	15 min at 1,000°C in N_2 + ~1% O_2	15 min at 1,000°C in N_2 + ~1% O_2	15 min at 1,000°C in N_2 + ~1% O_2
S_2	35 seconds at 1250°C in N_2	35 seconds at 1250°C in N_2	35 seconds at 1250°C in N_2
S_3	125°C/sec	125°C/sec	125°C/sec
S_4	4 hr at 800°C + 16 hr at 1,000°C in N_2	4 hr at 800°C + 16 hr at 1,000°C in N_2	4 hr at 800°C + 16 hr at 1,000°C in N_2
O_i (atoms/cm^3)	$6x10^{17}$	$7x10^{17}$	$8x10^{17}$
OPD (atoms/cm^3)	$4x10^{10}$	$1x10^{10}$	$6x10^{10}$
DZ (depth in μm)	~40	~40	~40

EXAMPLE 3

To demonstrate that the precipitation portion of the process of the present invention was relatively independent of the conditions used for the oxygen precipitate stabilization and growth step (S_4), a wafer (sample 1-8) having the same initial oxygen concentration was subjected to the same series of steps described in

Example 2 for sample 3-4 except that a proprietary, commercial 16 Mb DRAM process was used as the oxygen precipitate stabilization and growth step (S_4). Figure 9 shows a cross-section of the resulting wafer (this figure is an enlargement of a photograph taken at a magnification of 200X). After step S_4, samples 1-8 and 3-4 had comparable bulk oxygen precipitate densities ($7x10^{10}/cm^3$ for sample 1-8 versus $4x10^{10}/cm^3$ for sample 3-4) and comparable denuded zone depths (approximately 40 micrometers).

Example 4

This example illustrates the trend that may be observed in the density of bulk microdefects (BMD), i.e., the density of oxygen precipitants, and the depth of the denuded zone (DZ) resulting from an increase in the concentration of oxygen in the atmosphere during the heat-treatment step of the precipitation process. Three different sets of wafers were subjected to rapid thermal annealing under varying process conditions. The wafers in Set A were annealed at 1200°C for 30 seconds under a nitrogen atmosphere; the wafers in Set B were annealed under the same conditions for 20 seconds; and, the wafers in Set C were annealed at 1200°C for 30 seconds under an argon atmosphere. A pre-oxidation step was not performed on any of the wafers in the three sets in this Example.

As indicated by Table III, below, the oxygen partial pressure was increased for each wafer within a given Set. Once annealing was completed, the BMD density and DZ depth for each wafer was determined by means standard in the art. The results are present in Table III, below.

Table III

Wafer Set	Oxygen Partial Pressure	BMD Density (defects/cm^{-3})	DZ Depth (microns)
A	250 ppma	$6.14x10^9$	70
A	500 ppma	$6.24x10^9$	80
A	1000 ppma	$2.97x10^9$	80
A	2000 ppma	$7.02x10^8$	100
A	5000 ppma	$2.99x10^7$	ND
A	$1x10^6$ ppma	$6.03x10^6$	ND
B	500 ppma	$2.59X10^9$	80
B	1000 ppma	$1.72X10^9$	100
B	2000 ppma	$9.15X10^8$	100
B	5000 ppma	$2.65X10^7$	ND
B	$1x10^6$ ppma	$2.17X10^6$	ND
C	250 ppma	$2.65x10^9$	90
C	500 ppma	$4.03x10^9$	70
C	1000 ppma	$1.72x10^9$	140
C	5000 ppma	$1.69x10^8$	120

ND = not determined.

The above data shows that as the partial pressure of oxygen in the atmosphere increases, the number density of bulk microdefects decreases. In addition, when the oxygen partial pressure reaches 10,000 ppma, the number density of bulk microdefects is indistinguishable from the number density of bulk microdefects which is observed in wafers which have been subjected to an oxygen

precipitation heat-treatment without a prior rapid thermal annealing in accordance with the precipitation portion of the present invention.

EXAMPLE 5

Oxidative Thermal Anneal Treatment

For purposes of illustrating the oxidative thermal anneal treatment of the precipitation portion of the present invention, silicon wafers, obtained from single crystal silicon ingots grown in accordance with the Czochralski method, having only a native oxide layer were subjected to a rapid thermal annealing step (S_2). In each case, the wafers were annealed in a rapid thermal annealer under an ammonia-containing atmosphere at about 1180°C for about 3 minute, and then rapidly cooled (S_3). Referring now to FIGS. 11 and 12, it may be observed that, following an oxygen stabilization and growth step (S_4) and an NEC-1 treatment, such process conditions yield a silicon wafer having essentially no denuded zone and a bulk oxygen precipitate density (OPD) which is greater than about 1×10^{10} atoms/cm^3.

In contrast to the wafer of FIGS. 11 and 12, a denuded zone may be formed if, after cooling (S_3) is complete and prior to step S_4, the wafer is subjected to an oxidative thermal anneal step. Referring now to FIGS. 13 and 14, after cooling was complete the surface of a wafer etched slightly in order to remove any nitride layer present. The wafer was then heated to about 1180°C for about 3 minutes under an oxygen-containing ambient, having an oxygen concentration in this Example of about

100%, in a rapid thermal annealer. It may be observed that, following an oxygen stabilization and growth step (S_4) and an NEC-1 treatment, such process conditions yield a silicon wafer having a denuded zone depth of about 60 μm and a bulk oxygen precipitate density (OPD) which is greater than about 1 x 10^{10} atoms/cm^3.

Referring now to FIGS. 15 and 16, it may be observed that the oxidative thermal anneal step may be performed on only one side of the silicon wafer. Single-sided treatment is achieved by shielding the side of the wafer which is not to be treated. The wafer shown in FIGS. 15 and 16 was treated in the same manner as the wafer shown in FIGS. 13 and 14, with the exception that one side of the wafer was shielded by first forming a silicon nitride coating using a low temperature, chemical vapor phase deposition (CVD) process. It may be observed that, following an oxygen stabilization and growth step (S_4) and an NEC-1 treatment, the resulting wafer has a denuded zone depth of about 60 μm on the side which was not shielded (front-side), while the shielded side (back-side) of the wafer essentially had no denuded zone. The bulk oxygen precipitate density (OPD) of the wafer was greater than about 1 x 10^{10} atoms/cm^3.

It is to be noted that surface etching of the wafer to remove any nitride layer present is not necessary in order to achieve the results of the precipitation portion of the present process. Rather, the surface etch is optional and, accordingly, is not to be viewed in a limiting sense.

It is to be further noted that, in view of Example 5, that a denuded zone may be effectively formed by

thermally annealing the wafer in the presence of an oxidizing atmosphere. Additionally, a denuded zone formed by other embodiments of the precipitation portion of the present invention may be further modified by this thermal oxidation treatment. For example, the depth of the denuded zones of samples 4-7 and 4-8 (Example 1) may be increased by subjecting the samples to this thermal oxidation treatment prior to the oxygen precipitation heat treatment of step S_4. Likewise, for sample 3-14 (Example 1), a denuded zone may be formed by subjecting the wafer to this thermal oxidation treatment.

In view of the above, it will be seen that the several objects of the invention are achieved. As various changes could be made in the above compositions and processes without departing from the scope of the invention, it is intended that all matter contained in the above description be interpreted as illustrative and not in a limiting sense.

We claim:

1. A single crystal silicon wafer having two major, generally parallel surfaces, one of which is the front surface of the wafer and the other of which is the back surface of the wafer, a central plane between the front and back surfaces, a circumferential edge joining the front and back surfaces, a stratum extending from the front surface to a distance, D_0, as measured from the front surface and toward the central plane, a surface layer which at least in part is coextensive with the stratum and which comprises the region of the wafer between the front surface and a distance, D_1, of at least about 10 micrometers, as measured from the front surface and toward the central plane, and a bulk layer which comprises the region of the wafer between the central plane and the surface layer, the wafer being characterized in that

the wafer stratum is substantially free of agglomerated vacancy defects;

the bulk layer contains agglomerated vacancy defects; and,

the wafer has a non-uniform distribution of crystal lattice vacancies with the concentration of vacancies in the bulk layer being greater than the concentration of vacancies in the surface layer and with the vacancies having a concentration profile in which the peak density of the vacancies is at or near the central plane, the concentration generally decreasing from the position of peak density in the direction of the front surface of the wafer.

2. The wafer of claim 1 wherein D_1 is at least about 20 micrometers.

3. The wafer of claim 1 wherein D_1 is at least about 50 micrometers.

4. The wafer of claim 1, 2 or 3 wherein D_4 is at least about 5 micrometers.

5. The wafer of claim 1, 2 or 3 wherein D_8 is at least about 10 micrometers.

6. The wafer of claim 1, 2 or 3 wherein D_8 is at least about 20 micrometers.

7. The wafer of claim 1, 2 or 3 wherein the concentration of interstitial oxygen at distances greater than 3 microns from the wafer surface is at least about 50% of the concentration of interstitial oxygen in the bulk layer.

8. The wafer of claim 1, 2 or 3 wherein the concentration of interstitial oxygen at distances greater than 10 microns from the wafer surface is at least about 80% of the concentration of interstitial oxygen in the bulk layer.

9. The wafer of claim 1, 2 or 3 further characterized in that the wafer has an epitaxial layer on the front surface of the wafer.

10. The wafer of claim 1, 2 or 3 further characterized in that the front surface is polished.

11. The wafer of claim 1, 2 or 3 further characterized in that the wafer has a carbon concentration of about 1×10^{16} atoms/cm^3.

12. The wafer of claim 1, 2 or 3 further characterized in that the wafer has a carbon concentration of about 5×10^{15} atoms/cm^3.

13. The wafer of claim 1, 2 or 3 further characterized in that the wafer has an absence of oxygen precipitate nucleation centers which are incapable of being dissolved by heat-treating the wafer at a temperature not in excess of about 1300 °C.

14. A process for heat-treating a single crystal silicon wafer to dissolve agglomerated vacancy defects and to influence the precipitation behavior of oxygen in the wafer in a subsequent thermal processing step, the silicon wafer having two major, generally parallel surfaces, one of which is the front surface of the wafer and the other of which is the back surface of the wafer, a central plane between the front and back surfaces, a circumferential edge joining the front and back surfaces, a stratum extending from the front surface to a distance, D_s, measured from the front surface and toward the central plane, a surface layer which, at least in part is coextensive with the stratum and which comprises the region of the wafer between the front surface and a

distance, D, measured from the front surface and toward the central plane, and a bulk layer which comprises the region of the wafer between the central plane and the surface layer, the process comprising:

thermally annealing the wafer in an atmosphere to dissolve pre-existing agglomerated vacancy defects in the stratum;

heat-treating the annealed wafer to form crystal lattice vacancies in the surface and bulk layers; and,

controlling the cooling rate of the heat-treated wafer to produce a wafer having a vacancy concentration profile in which the peak density is at or near the central plane with the concentration generally decreasing in the direction of the front surface of the wafer, the difference in the concentration of vacancies in the surface and bulk layers being such that a thermal treatment of the wafer at a temperature in excess of 750 °C is capable of forming a denuded zone in the surface layer and oxygen clusters or precipitates in the bulk layer with the concentration of the oxygen clusters or precipitates in the bulk layer being primarily dependant upon the concentration of vacancies.

15. The process of claim 14 wherein the wafer is thermally annealed in an atmosphere of hydrogen, argon or a mixture thereof.

16. The process of claim 14 wherein the wafer is thermally annealed at a temperature between about 1100 °C and about 1300 °C for about 1 to about 4 hours.

17. The process of claim 14 wherein heat-treating the annealed wafer comprises:

(a) subjecting said wafer to a first heat-treatment in an oxidizing atmosphere to form a superficial silicon dioxide layer of a thickness of at least about 20 angstroms; and,

(b) subjecting the product of (a) to a second heat-treatment at a temperature of at least about 1150°C.

18. The process of claim 17 wherein the atmosphere for said second heat-treatment is non-nitriding.

19. The process of claim 18 wherein the atmosphere for said second heat-treatment is primarily argon, helium or a mixture thereof.

20. The process of claim 17 wherein the atmosphere for said second heat-treatment is nitriding.

21. The process of claim 17 wherein the second heat-treatment comprises heating the wafer to a temperature in excess of about 1175 °C in an oxygen containing atmosphere for a period of less than 60 seconds with the partial pressure of oxygen being less than about 5,000 ppma.

22. The process of claim 17 wherein the second heat-treatment comprises heating the wafer to a temperature in excess of about 1200 °C in an oxygen containing atmosphere for a period of less than 60

seconds with the partial pressure of oxygen being less than about 5,000 ppma.

23. The process of any one of claims 14 through 22 wherein said cooling rate is at least about 50 °C per second through the temperature range at which crystal lattice vacancies are relatively mobile in silicon.

24. The process of any one of claims 14 through 22 wherein said cooling rate is at least about 100 °C per second through the temperature range at which crystal lattice vacancies are relatively mobile in silicon.

25. The process of any one of claims 14 through 22 wherein the wafer is thermally annealed to dissolve pre-existing agglomerated vacancy defects in the stratum to a depth of about 10 micrometers.

26. The process of any one of claims 14 through 22 wherein the wafer is thermally annealed to dissolve pre-existing agglomerated vacancy defects in the stratum to a depth of about 20 micrometers.

27. The process of claim 14 wherein heat-treating the annealed wafer comprises:

(a) subjecting said wafer to a first heat-treatment at a temperature of at least about 1150°C in a nitriding atmosphere; and,

(b) subjecting the product of (a) to a second heat-treatment at a temperature of at least about 1150°C in an

oxidizing atmosphere having a partial pressure of oxygen of at least about 100 ppma.

28. The process of claim 14 wherein the annealed wafer is heat-treated in a nitriding atmosphere having a partial pressure of oxygen ranging from at least about 100 ppma to less than about 5,000 ppma.

29. A process for heat-treating a single crystal silicon wafer to dissolve agglomerated vacancy defects and to influence the precipitation behavior of oxygen in the wafer in a subsequent thermal processing step, the silicon wafer having a front surface, a back surface, a central plane between the front and back surfaces, a stratum extending from the front surface to a distance, D_s, measured from the front surface and toward the central plane, a surface layer which, at least in part, is coextensive with the stratum and which comprises the region of the wafer between the front surface and a distance, D, measured from the front surface and toward the central plane, and a bulk layer which comprises the region of the wafer between the central plane and surface layer, the process comprising the steps of:

heat-treating the wafer in an atmosphere to form crystal lattice vacancies in the surface and bulk layers;

controlling the cooling rate of the heat-treated wafer to produce a wafer having a vacancy concentration profile in which the peak density is at or near the central plane with the concentration generally decreasing in the direction of the front surface of the wafer and the difference in the concentration of vacancies in the

surface and bulk layers being such that a thermal treatment of the wafer at a temperature in excess of 750 °C is capable of forming a denuded zone in the surface layer and oxygen clusters or precipitates in the bulk layer with the concentration of the oxygen clusters or precipitates in the bulk layer being primarily dependant upon the concentration of vacancies;

stabilizing oxygen precipitate nucleation centers present in the cooled wafer by heating the cooled wafer to a temperature of about 650 to about 850 °C for about 1 hour to about 4 hours; and,

thermally annealing the stabilized wafer in an atmosphere to dissolve agglomerated vacancy defects present within a region extending from the front surface to a depth of at least about 5 microns.

30. The process of claim 29 wherein the stabilized wafer is thermally annealed in an atmosphere of hydrogen, argon or a mixture thereof.

31. The process of claim 29 wherein the stabilized wafer is thermally annealed at a temperature between about 1100 °C and about 1300 °C for about 1 to about 4 hours.

32. The process of claim 29 wherein heat-treating the wafer comprises:

(a) subjecting the wafer to a first heat-treatment in an oxidizing atmosphere to form a superficial silicon dioxide layer of a thickness of at least about 20 angstroms; and,

(b) subjecting the product of (a) to a second heat-treatment at a temperature of at least about 1150°C.

33. The process of claim 32 wherein the atmosphere for said second heat-treatment is non-nitriding.

34. The process of claim 33 wherein the atmosphere for said second heat-treatment is primarily argon, helium or a mixture thereof.

35. The process of claim 32 wherein the atmosphere for said second heat-treatment is nitriding.

36. The process of claim 32 wherein the wafer is subjected to a second heat-treatment at a temperature in excess of about 1175 °C in an oxygen containing atmosphere for a period of less than 60 seconds with the partial pressure of oxygen being less than about 5,000 ppma.

37. The process of claim 32 wherein the wafer is subjected to a second heat-treatment at a temperature in excess of about 1200 °C in an oxygen containing atmosphere for a period of less than 60 seconds with the partial pressure of oxygen being less than about 5,000 ppma.

38. The process of any one of claims 29 through 37 wherein the stabilized wafer is thermally annealed to dissolve agglomerated vacancy defects within a region

extending from the front surface to a depth of at least about 10 microns.

39. The process of any one of claims 29 through 37 wherein the stabilized wafer is thermally annealed to dissolve agglomerated vacancy defects within a region extending from the front surface to a depth of at least about 20 microns.

40. The process of any one of claims 29 through 39 wherein said cooling rate is at least about 50 °C per second through the temperature range at which crystal lattice vacancies are relatively mobile in silicon.

41. The process of any one of claims 29 through 39 wherein said cooling rate is at least about 100 °C per second through the temperature range at which crystal lattice vacancies are relatively mobile in silicon.

42. The process of claim 29 wherein heat-treating the wafer comprises:

(a) subjecting the wafer to a first heat-treatment at a temperature of at least about 1150°C in a nitriding atmosphere; and,

(b) subjecting the product of (a) to a second heat-treatment at a temperature of at least about 1150°C in an oxidizing atmosphere having a partial pressure of oxygen of at least about 100 ppma.

43. The process of claim 29 wherein the wafer is heat-treated in a nitriding atmosphere having a partial

pressure of oxygen ranging from at least about 100 ppma to less than about 5,000 ppma.