CLAIMS

~~What is claimed is:~~

1. A method of wireless communication, comprising:

generating an information block comprising control information for a scheduled entity;

~~selecting~~generating a ~~total number~~single set of ~~combined~~ cyclic redundancy check (CRC) bits ~~based on at least a list size utilized in~~corresponding to a total number of combined CRC bits equal to a sum of a first number of integrity check bits and a second number of CRC-aided successive-cancellation list (SCL) ~~decoding at the scheduled entity~~bits;

generating CRC information for the information block, the CRC information comprising the total number of the combined CRC bits;

encoding the information block, including the CRC information, utilizing polar coding to generate a polar code block; and

transmitting the polar code block to the scheduled entity over a wireless air interface.

2. The method of claim 1, ~~wherein selecting the number of CRC bits~~ further ~~comprises~~comprising:

selecting the ~~total number of the combined CRC bits to be equal to a sum of a first number of integrity check bits and a~~ second number of the CRC-aided SCL bits~~, wherein the second number of the CRC-aided SCL bits is selected~~ based on ~~the~~a list size~~.~~ utilized in SCL decoding at the scheduled entity.

3. The method of claim 2, wherein selecting the number of combined CRC bits further comprises:

selecting the second number of the CRC-aided SCL bits to be equal to a binary logarithm of the list size.

4. The method of claim 3, wherein:

the second number of the CRC-aided SCL bits comprises three bits when the list size is equal to eight; and

the second number of the CRC-aided SCL bits comprises five bits when the list size is equal to thirty-two.

5. The method of claim 4, wherein the first number of the integrity check bits comprises sixteen bits.

6. The method of claim 1, wherein the information block comprises a plurality of original bit locations and the polar code block comprises a plurality of coded bit locations, wherein each of the plurality of coded bit locations corresponds to one of a plurality of sub-channels, and wherein generating the information block further comprises:

determining a reliability metric for each of the original bit locations to produce a plurality of reliability metrics;

sorting the plurality of sub-channels based on the plurality of reliability metrics in order from highest reliability metrics to lowest reliability metrics; and

allocating a portion of the plurality of sub-channels either comprising the highest reliability metrics or distributed among the plurality of sub-channels to the CRC information.

7. The method of claim 1, wherein generating the CRC information further comprises:

adding an additional number of zero bits to the control information to produce a first polynomial, wherein the additional number of the zero bits is equal to the total number of the combined CRC bits;

dividing the first polynomial by a generator polynomial to produce a remainder polynomial comprising the total number of the combined CRC bits;

scrambling the combined CRC bits with an identifier associated with the scheduled entity to produce the CRC information; and

appending the CRC information to the control information in the information block.

8. An apparatus configured for polar coding, the apparatus comprising:

a processor;

a memory communicatively coupled to the processor; and

a transceiver communicatively coupled to the processor,

wherein the processor is configured to:

generate an information block comprising control information for a scheduled entity;

~~select~~generate a ~~total number~~single set of ~~combined~~ cyclic redundancy check (CRC) bits ~~based on at least~~corresponding to a ~~list size utilized in~~ total number of combined CRC bits equal to a sum of a first number of integrity check bits and a second number of CRC-aided successive-cancellation list (SCL) ~~decoding at the scheduled entity~~bits;

generate CRC information for the information block, the CRC information comprising the total number of the combined CRC bits;

encode the information block, including the CRC information, utilizing polar coding to generate a polar code block; and

transmit the polar code block to the scheduled entity over a wireless air interface via the transceiver.

9. The apparatus of claim 8, wherein the processor is further configured to:

select the ~~total number of the combined CRC bits to be equal to a sum of a first number of integrity check bits and a~~ second number of the CRC-aided SCL bits~~, wherein the second number of the CRC-aided SCL bits is selected~~ based on ~~the~~a list size utilized in SCL decoding at the scheduled entity.

10. The apparatus of claim 9, wherein the processor is further configured to:

select the second number of the CRC-aided SCL bits to be equal to a binary logarithm of the list size.

11. The apparatus of claim 10, wherein:

the second number of the CRC-aided SCL bits comprises three bits when the list size is equal to eight; and

the second number of the CRC-aided SCL bits comprises five bits when the list size is equal to thirty-two.

12. The apparatus of claim 11, wherein the first number of the integrity check bits comprises sixteen bits.

13. The apparatus of claim 8, wherein the information block comprises a plurality of original bit locations and the polar code block comprises a plurality of coded bit locations, wherein each

of the plurality of coded bit locations corresponds to one of a plurality of sub-channels, and wherein the processor is further configured to:

determine a reliability metric for each of the original bit locations to produce a plurality of reliability metrics;

sort the plurality of sub-channels based on the plurality of reliability metrics in order from highest reliability metrics to lowest reliability metrics; and

allocate a portion of the plurality of sub-channels either comprising the highest reliability metrics or distributed among the plurality of sub-channels to the CRC information.

14. The apparatus of claim 8, wherein the processor is further configured to:

add an additional number of zero bits to the control information to produce a first polynomial, wherein the additional number of the zero bits is equal to the number of the combined CRC bits;

divide the first polynomial by a generator polynomial to produce a remainder polynomial comprising the number of the combined CRC bits;

scramble the combined CRC bits with an identifier associated with the scheduled entity to produce the CRC information; and

append the CRC information to the control information in the information block.

15. A method of wireless communication operable at a scheduled entity, comprising:

receiving a polar code block comprising control information for the scheduled entity and cyclic redundancy check (CRC) information comprising a single set of CRC bits corresponding to a total number of combined CRC bits ~~selected based on at least a list size utilized in~~equal to a sum of a first number of integrity check bits and a second number of CRC-aided successive-cancellation list (SCL) ~~decoding at the scheduled entity~~bits;

SCL decoding the polar code block utilizing ~~SCL decoding and~~ the CRC information to produce an information block comprising the control information and the CRC information; and

verifying an integrity of the control information utilizing the CRC information.

16. The method of claim 15, wherein the ~~total number of the combined CRC bits is equal to a sum of a first number of integrity check bits and a~~ second number of CRC-aided SCL bits~~,~~

~~wherein the second number of CRC-aided SCL bits is selected~~ is based on ~~the~~a list size utilized in the SCL decoding.

17. The method of claim 16, wherein the second number of CRC-aided SCL bits is equal to a binary logarithm of the list size.

18. The method of claim 17, wherein:

the second number of the CRC-aided SCL bits comprises three bits when the list size is equal to eight; and

the second number of the CRC-aided SCL bits comprises five bits when the list size is equal to thirty-two.

19. The method of claim 18, wherein the first number of the integrity check bits comprises sixteen bits.

20. The method of claim 15, wherein the information block comprises a plurality of original bit locations and the polar code block comprises a plurality of coded bit locations, wherein each of the coded bit locations corresponds to one of a plurality of sub-channels, and wherein receiving the polar code block further comprises:

receiving the CRC information within a portion of the plurality of sub-channels either comprising highest reliability metrics or distributed among the plurality of sub-channels.

21. The method of claim 15, wherein verifying the integrity of the control information utilizing the CRC information further comprises:

descrambling the CRC information utilizing an identifier associated with the scheduled entity to produce the combined CRC bits;

dividing the information block comprising the control information and the combined CRC bits by a generator polynomial to produce a remainder; and

if the remainder is equal to zero, verifying the control information is correctly received.

22. The method of claim 15, wherein decoding the polar code block utilizing SCL decoding and the CRC information further comprises:

decoding the polar code block to produce a plurality of information block candidates, wherein a number of the plurality of information block candidates is equal to the list size; and

utilizing the CRC information to select one of the plurality of information block candidates as the information block.

23. An apparatus configured for polar decoding, the apparatus comprising:

a processor;

a memory communicatively coupled to the processor; and

a transceiver communicatively coupled to the processor,

wherein the processor is configured to:

receive, via the transceiver, a polar code block comprising control information for the scheduled entity and cyclic redundancy check (CRC) information comprising a single set of CRC bits corresponding to a total number of combined CRC bits ~~selected based on at least a list size utilized in~~equal to a sum of a first number of integrity check bits and a second number of CRC-aided successive-cancellation list (SCL) ~~decoding at the apparatus~~bits;

~~decode~~SCL decoding the polar code block utilizing ~~SCL decoding and~~ the CRC information to produce an information block comprising the control information and the CRC information; and

verify an integrity of the control information utilizing the CRC information.

24. The apparatus of claim 23, wherein the ~~total number of the combined CRC bits is equal to a sum of a first number of integrity check bits and a~~ second number of CRC-aided SCL bits~~, wherein the second number of CRC-aided SCL bits is selected~~ is based on ~~the~~a list size utilized in the SCL decoding.

25. The apparatus of claim 24, wherein the second number of CRC-aided SCL bits is equal to a binary logarithm of the list size.

26. The apparatus of claim 25, wherein:

the second number of the CRC-aided SCL bits comprises three bits when the list size is equal to eight; and

the second number of the CRC-aided SCL bits comprises five bits when the list size is equal to thirty-two.

27. The apparatus of claim 26, wherein the first number of the integrity check bits comprises sixteen bits.

28. The apparatus of claim 23, wherein the information block comprises a plurality of original bit locations and the polar code block comprises a plurality of coded bit locations, wherein each of the coded bit locations corresponds to one of a plurality of sub-channels, and wherein the processor is further configured to:

receive the CRC information within a portion of the plurality of sub-channels either comprising highest reliability metrics or distributed among the plurality of sub-channels.

29. The apparatus of claim 23, wherein the processor is further configured to:

descramble the CRC information utilizing an identifier associated with the apparatus to produce the combined CRC bits;

divide the information block comprising the control information and the combined CRC bits by a generator polynomial to produce a remainder; and

if the remainder is equal to zero, verify the control information is correctly received.

30. The apparatus of claim 23, wherein the processor is further configured to:

decode the polar code block to produce a plurality of information block candidates, wherein a number of the plurality of information block candidates is equal to the list size; and

utilize the CRC information to select one of the plurality of information block candidates as the information block.

31. An apparatus configured for polar coding, comprising:

means for generating an information block comprising control information for a scheduled entity;

means for generating a single set of cyclic redundancy check (CRC) bits corresponding to a total number of combined CRC bits equal to a sum of a first number of integrity check bits and a second number of CRC-aided successive-cancellation list (SCL) bits;

means for generating CRC information for the information block, the CRC information comprising the total number of the combined CRC bits;

means for encoding the information block, including the CRC information, utilizing polar coding to generate a polar code block; and

means for transmitting the polar code block to the scheduled entity over a wireless air interface.

32. An article of manufacture, comprising:

a non-transitory computer-readable medium having stored therein instructions executable by one or more processors of an apparatus to:

generate an information block comprising control information for a scheduled entity;

generate a single set of cyclic redundancy check (CRC) bits corresponding to a total number of combined CRC bits equal to a sum of a first number of integrity check bits and a second number of CRC-aided successive-cancellation list (SCL) bits;

generate CRC information for the information block, the CRC information comprising the total number of the combined CRC bits;

encode the information block, including the CRC information, utilizing polar coding to generate a polar code block; and

transmit the polar code block to the scheduled entity over a wireless air interface.

33. An apparatus configured for polar decoding, comprising:

means for receiving a polar code block comprising control information for the scheduled entity and cyclic redundancy check (CRC) information comprising a single set of CRC bits corresponding to a total number of combined CRC bits equal to a sum of a first number of integrity check bits and a second number of CRC-aided successive-cancellation list (SCL) bits;

means for SCL decoding the polar code block utilizing the CRC information to produce an information block comprising the control information and the CRC information; and

means for verifying an integrity of the control information utilizing the CRC information.

34. An article of manufacture, comprising:

a non-transitory computer-readable medium having stored therein instructions executable by one or more processors of an apparatus to:

receive a polar code block comprising control information for the scheduled entity and cyclic redundancy check (CRC) information comprising a single set of CRC bits

corresponding to a total number of combined CRC bits equal to a sum of a first number of integrity check bits and a second number of CRC-aided successive-cancellation list (SCL) bits;

SCL decode the polar code block utilizing the CRC information to produce an information block comprising the control information and the CRC information; and

verify an integrity of the control information utilizing the CRC information.