Method for Fabricating a Semiconductor on Insulator Substrate with Reduced SECCO Defect Density

The invention relates to a method for fabricating a semiconductor on insulator (SeOI) substrate, in particular a silicon on insulator (SOI) substrate, comprising the steps of providing a source substrate, providing a predetermined splitting area inside the source substrate, attaching, preferably by bonding, the source substrate to a handle substrate, detaching a remainder of the source substrate from the source handle compound at the predetermined splitting area to thereby transfer a device layer of the source substrate onto the handle substrate, and thinning of the device layer.

Such semiconductor on insulator substrates, like the mentioned silicon on insulator substrate, represent a certain amount of different defects, e.g. crystalline defects, point defects, metallic contamination, etc. One particular type of defect is a so-called SECCO defect. In the past, these defects were not considered to be critical as the number was low enough for the typical SOI applications, e.g. logic circuits. However, with new applications coming up for SOI technology, e.g. memory devices, SeOI substrates need to be provided with a SECCO defect level of less than 100 per cm^2, whereas, up to now, this value was about a factor five higher.

Figure 1 illustrates the standard process of determining SECCO defects in SOI structures and which has been described in L.F.Giles, A.Nejim, P.L.F.Hemment, Vacuum 43, 297 (1992) or by the same authors in Materials Chemistry and Physics 35 (1993) 129-133.

The concentration of SECCO defects can be determined by displaying them by virtue of a solution of SECCO type, the composition of which is known from the above mentioned documents.

Starting from a SOI substrate 1 comprising a device layer 3 with a thickness of e.g. 2000 Å and a silicon oxide layer 5 with a thickness of e.g. 4000 Å on a silicon wafer 7, a standard technique for displaying defects by virtue of a solution of SECCO type comprises:

A stage A which consists in immersing the substrate 1 for several seconds, for example 10 to 25 seconds in a solution of SECCO type in order to etch 1000 – 2000 Å of silicon from the device layer 3 and more rapidly to selectively etch this device layer 3 at the crystal defects 9 in the material until holes 11 corresponding to the sites of the defects 9 open onto the silicon oxide layer 5.

The duration of stage A depends on the thickness to be removed and has to be such that all SECCO defects can be identified. As a rule of thumb, at least half of the thickness of the device layer is removed, but for thicker layers this might be much more, for example such that 500 or 300 Angstroms are left, even for device layers with a thickness between 1000 and 2000 Angstroms. On the other hand, for very thin device layers (800 Angstroms or less than 500 Angstroms), it might be sufficient to remove less than half of the thickness because the SECCO defects are revealed before, i.e. the SECCO defects penetrate the device layer even before half of the thickness is etched away.

A stage B, which consists in immersing the substrate 1 in a hydrofluoric acid solution in order to etch the holes 11 produced in the preceding stage, by widening them in the dielectric layer 5.

Following this treatment, the holes 11 which remain are sufficiently large so that they can be counted under a microscope. It appears that, at a certain remaining device layer 3 thickness, the defect density stabilizes and reaches an upper limit value indicating that, starting from this thickness, all defects in the original layer are visualized. In the case of standard semiconductor on insulator substrates, stabilization is achieved around 500Å or at the latest around 300Å of remaining device layer 3 thickness. Indeed, it appears that the device layer 3 in the zone of SECCO defects etches approximately two times as fast as the normal device layer in zones without SECCO defects.

US 2005/0208322 discloses a method for fabricating a semiconductor on insulator substrate dealing with removal of defects. The proposed process is a SmartCut™ type process which comprises additional steps the transfer of a semiconductor device layer from a source substrate onto a handle substrate to reduce the number of defects. These additional steps comprise a sacrificial oxidation stage transforming a part of the device layer into an oxide, which is removed, followed by a polishing stage. With this steps, defects in the surface

regions can be removed. However, the polishing stage introduces additional defects which are then removed by a second sacrificial oxidation stage oxidizing a surface part of the semiconductor device layer and removing the oxidized portions. With this method, SECCO defects in a range of about 500 defects per cm^2 can be achieved. However, this method has the disadvantage that an additional process step is necessary and, furthermore, it is not possible to achieve defect levels of 100 defects per cm^2 or less.

Other SOI manufacturing processes have been proposed which do not include the polishing step. US 2005/0026426 proposes a thermal treatment to minimize high frequency roughness so that chemical mechanical polishing is not needed. This type of process, in particular, includes a high temperature anneal of the silicon on insulator substrate with the device layer being protected by a layer of silicon oxide known as "stabilization oxidation anneal". However, this type of long and high temperature anneal can generate other types of defects such as slip lines. Furthermore, these kind of anneal steps require furnaces that can sustain high temperatures which are generally relatively expensive and difficult to control in terms of contamination.

It appears that these known processes still do not lead to SECCO defect densities of better than 100 per cm^2 and that, for device layers of less than 1000Å, the described methods do not lead to satisfying results. Starting therefrom, it is the purpose of this invention to provide a semiconductor on insulator wafer fabrication method with which a SECCO defect density of less than 100 defects per cm^2 is achievable and which can be applied to relatively thin device layers.

This object is achieved with the method accordingly to claim 1. Accordingly, the method comprises the steps of providing a source substrate, providing a predetermined splitting area inside the source substrate, attaching, preferably by bonding, the source substrate to a handle substrate to form a source handle compound, detaching a remainder of the source substrate from the source-handle compound at the predetermined splitting area to thereby transfer a device layer of the source substrate onto the handle substrate and thinning of the device layer. The method is characterised in that the predetermined splitting area is provided by implanting atomic species with a dose of less than 2.3×10^{16} atoms per cm^2 and thinning is carried out at a temperature of less than 925°C, e.g. between 850°C and 925°C; preferentially between 850°C and 875°C.

It appears that, even though each one of the process parameters might have been previously known individually, it is the special combination of the process parameters which leads to a surprisingly high reduction in SECCO defects down to less than 100 defects per cm^2 or even less than 50 defects per cm^2, in particular for final device layer thicknesses of less than 1000 Å.

In the claimed temperature regime, a good balance between throughput and SECCO defect densities can be achieved. In case one is interested in reducing SECCO defect density even further, preferred temperature ranges are less than 900°C, more in particular less than 850°C.

Preferably, the method can comprise a thermal treatment step before and/or after the thinning. Even further preferred can be a rapid thermal anneal (RTA) step of a duration of at least 30 seconds, in particular between 30 seconds and 90 seconds, more in particular between 45 seconds and 75 seconds at a temperature of at least 1200°C, in particular at about 1250°C. Such a rapid thermal anneal step does not only lead to a reduction in surface roughness but it has furthermore been observed that synergistic effects with respect to SECCO defects are observed in combination with the above mentioned process parameters so that the number of SECCO defects can be even further reduced.

According to a variant, the thermal treatment step can be a furnace anneal of at least 10 minutes in a temperature range of 1000 - 1200°C. With such a thermal treatment step, not only the surface roughness can be reduced but, furthermore, the SECCO defect density can also be optimized.

Advantageously, the thermal treatment step can be carried out under non-oxidizing atmosphere, in particular under Argon. Under this atmosphere, a further optimization of surface roughness, as well as SECCO defects, has been observed.

According to an advantageous embodiment, the thermal treatment step can comprise two or more successive rapid thermal treatment steps. Better annealing results are obtained by carrying out multiple short RTA runs compared to one long run.

Advantageously, the predetermined splitting area can be achieved using helium and hydrogen ions with a dose of 1.4 x 10^{16} atoms/cm^2 or less , in particular in a range of 1.2 x 10^{16} atoms/cm^2 to 1.4 x 10^{16} atoms/cm^2, more in particular in a range of 1.3 x 10^{16} atoms/cm^2 to 1.4 x 10^{16} atoms/cm^2, or and 0.9 x 10^{16} atoms/cm^2 or less, in particular in a range of 0.7 x 10^{16} atoms/cm^2 to 0.9 x 10^{16} atoms/cm^2, more in particular in a range of 0.8 x 10^{16} atoms/cm^2 to 0.9 x 10^{16} atoms/cm^2, respectively. Under these process conditions, a further reduced SECCO defect density can be achieved. In particular, the combination of two different types of ions plays a role in reducing SECCO defects.

According to a preferred embodiment, implanting can be carried out at an energy of 49 keV or less concerning Helium. Reducing the energy of the ions, in particular of the helium ions, to 49 keV or less, has revealed a further reduction in the SECCO defect density.

Preferably, the thinning can comprise at least a first and a second thinning step. Splitting the thinning step into two or more distinct steps has shown better results concerning the amount of SECCO defects compared to having only one thinning step, in the case of thinning by thermal oxidation and des-oxidation. This result can be even further improved when a rapid thermal annealing (RTA) step is carried out between both thinning steps.

Preferably, a temperature treatment can be carried out after the first and second thinning steps, respectively. Again, not only the surface roughness value can be optimized but, at the same time, SECCO defects can be reduced by combining a thinning step with a temperature treatment step.

Preferably thinning can comprise oxidizing the device layer. Thinning in this context is thus achieved by consuming a part of the transferred device layer by oxidation. Later in the process, a removal step can be carried out to remove the oxidized region with a suitable process, e.g. etching.

Preferably the thickness reduction of the device layer can be larger for the second thinning step than for the first thinning step. By doing so, it appears that the SECCO defect density further diminishes, particularly when a rapid thermal annealing step is carried out between both thinning steps.

According to a variant, the thinning can be achieved by at least one of wet etch, dry etch and etching under HCl and H. While the wet etch is typically carried out at room temperature, the dry etch and etching under HCl and H are carried out at a temperature of less than 925°C, for example between 900°C and 925°C. Here the process can thus be carried out at rather low temperatures.

Preferably, the device layer can have a thickness of 1000Å or less after the thinning. As already described above, the prior art processes do not lead to sufficiently low SECCO defect densities for thin or thinned device layers of 1000Å, whereas the advantageous combination of different process parameters also leads to reduced SECCO defects in very thin device layers of 1000Å and less.

The object of the invention is also achieved with the silicon on insulator wafer, in particular, fabricated according to one of the methods described above.

The invention will be described in detail in conjunction with the enclosed Figures:

Figure 1 illustrates the known process of determining the SECCO defect, and

Figures 2A – 2H illustrate one embodiment of the inventive method for fabricating a semiconductor on insulator substrate with reduced SECCO defect density.

Figure 2A illustrates the source substrate 21, here a silicon wafer, e.g. a 300 mm silicon wafer, comprising a silicon base 23 and a silicon oxide layer 25 which is the natural silicon oxide but could also be a deposited or artificially grown silicon oxide layer or any other suitable dielectric layer.

According to the invention, atomic species, here a mixture of helium and hydrogen ions, are implanted with a dose not exceeding 2.3×10^{16} atoms/cm^2. According to an advantageous variant of the invention, the helium ions are implanted with a dose of 1.4×10^{16} atoms/cm^2 and the hydrogen ions with a dose of 0.9×10^{16} atoms/cm^2. The energy of the ions is, according to this embodiment, 49 keV for helium and 32 keV for hydrogen. This leads to about 2450Å depth of implantation. The implanting of the ions, indicated by a series of

arrows in Figure 2B, leads to the formation of a predetermined splitting area 27 inside the source substrate 21, here inside the silicon base 23 essentially parallel to the main surface of the source substrate 21.

Subsequently, illustrated in Figure 2C, the source substrate 21 is attached, preferably by bonding via the oxide layer 23, with a handle substrate 29, in this example also a 300 mm silicon wafer with or without dielectric layer, to form a source-handle compound. Instead of a silicon wafer, any other suitable handle substrate 29 could be used.

By providing thermal or mechanical energy, the predetermined splitting area 27 (Figure 2C) is further weakened which in turn leads to a complete detachment of a remainder 31 of the source substrate 21 and the transfer of a device layer 33, together with the dielectric layer 23, onto the handle substrate 19, as illustrated in Figure 2D. The transferred layers have a transferred thickness of about 2450Å, corresponding to an intermediate wafer product. After the thinning steps of the manufacturing process, the final device layer is thinner, for example 1000 or 800Å or less. This corresponds thus to the final wafer product.

The next process step consists in a sacrificial oxidation which, according to the invention, is carried out at a temperature of less than 925°C, in particular between 850°C and 925°C, more in particular between 850°C and 875°C. The aim of this step is to reduce the thickness of the device layer by transforming a part of the transferred silicon of device layer 33 into a silicon oxide 35. Thus, by doing so, the silicon part of transferred device layer 37 is thinner (see Figure 2E). Typically 800Å of the device layer 33 are transformed during this step. In case that throughput plays a secondary role, it is even possible to carry out the process at less than 900°C, in particular at less than 850°C.

Instead of or in addition to a sacrificial oxidation, it is also possible to carry out an etch step under HCl and H atmosphere to partially remove the device layer.

Subsequently, a rapid thermal anneal step is carried out which serves to reduce the roughness. According to this embodiment, the rapid thermal anneal is carried out at a temperature of at least 1200°C, in particular at about 1250°C for at least 30 seconds, preferably between 30 – 90 seconds, more in particular between 45 - 75 seconds.

As a next step, the oxide layer 35 is removed by a standard process, like etching using e.g. a HF solution. This leads to the situation as illustrated in Figure 2F wherein the structure comprises the base 29, the transferred oxide layer 23 and the thinned device layer 37.

Subsequently, a second oxidation step is carried out by oxidation which leads to a partial consumption of the already thinned device layer 37 which is turned into an oxide 39 so that the remaining thinned device layer 41 now has a thickness of 1000Å or less. Also, this oxidation step is carried out at less than 925°C.

Subsequently, again, a rapid anneal step is carried out at 1200°C, in particular at 1250°C for at least 30 seconds, in particular between 30 – 90 seconds, more in particular between 45 - 75 seconds, preferably under an Argon atmosphere and/or Helium atmosphere and/or Hydorgen atmosphere. Finally, an additional removal step is carried out to remove the oxide layer 39 to achieve the final structure comprising a thinned device layer 41 on a dielectric layer 23 and the base 29, as illustrated in Figure 2H.

The inventive method according to the described embodiment has the advantage that each process step is optimized such that synergistic effects occur which lead to an important reduction in SECCO defects, namely with a density being lower than 100 defects per cm^2 or even lower than 50 defects per cm^2. This optimization is achieved with a choice of a low ion implantation density and the choice of a low oxidation temperature when reducing the thickness of the transferred layer. In addition, the special process parameters of the rapid thermal anneal step also lead to a reduction of the SECCO defect density. Furthermore, the splitting of the thinning into two distinct steps further helps in keeping the SECCO defects low. The process parameter mix is furthermore such that device layers of less than 1000Å can be provided with the mentioned low SECCO defect density.

Without departing from the inventive concept, the invention according to the first embodiment can be carried out under the following variants. First of all, instead of only carrying out one RTA step after each oxidation, it is further beneficial to carry out at least two or more RTAs successively. According to another embodiment, the thermal treatment step can also be a furnace anneal of at least 10 minutes carried out in a temperature range of 1000 - 1200°C, in an Argon atmosphere. According to a further variant, the oxidation as a thinning step can be replaced by a wet etch, dry etch or an etching under HCl and H.

By carrying out this first embodiment or any of the variants alone or in combination, SECCO defect densities of less than 100 per cm^2, in particular less than 50 per cm^2 have been fabricated and the low amount of SECCO defects has even been observed for large diameter substrates, e.g. based on 300 mm wafers. It therefore becomes possible to use this kind of substrate also for memory devices.

Claims

1. Method for fabricating a semiconductor on insulator substrate, in particular a silicon on insulator substrate, comprising the steps of:

   - providing a source substrate, preferably a mono-crystalline source substrate
   - providing a predetermined splitting area inside the source substrate
   - attaching, preferably by bonding, the source substrate to a handle substrate to form a source-handle compound
   - detaching a remainder of the source substrate from the source-handle compound at the predetermined splitting area to thereby transfer a device layer of the source substrate onto the handle substrate
   - thinning of the device layer

   characterized in that

   the predetermined splitting area is provided by implanting atomic species with a dose of less than 2.3×10^{16} atoms/cm² and thinning is carried out at a temperature of less than 925°C, in particular between 850°C and 925°C, more in particular between 850 and 875°C, such that a SECCO defect density of less than 100 defects per cm^2, in particular less than 50 defects per cm^2, is achieved.

2. Method according to claim 1 further comprising a thermal treatment step before and/or after the thinning.

3. Method according to claim 2, wherein the thermal treatment step is a rapid thermal anneal (RTA) step of a duration of at least 30 seconds, preferably between 30 - 90 seconds, more in particular between 45 - 75 seconds.

4. Method according to claim 3, wherein the RTA is carried out at a temperature of at least 1200°C, in particular at about 1250°C.

5. Method according to claim 2, wherein the thermal treatment step is a furnace anneal of at least 10 minutes.

6. Method according to claim 5, wherein the temperature is in a range of 1000°C to 1200°C.

7. Method according to claim 2 to 6, wherein the thermal treatment step is carried out under a non oxidizing atmosphere, in particular under Ar and/or H.

8. Method according to one of claims 2 to 7, wherein the thermal treatment step comprises two or more successive rapid thermal treatment steps.

9. Method according to one of claims 1 to 8, wherein providing of the predetermined splitting area is achieved using He and or H ions with dose of 1.4×10^{16} atoms/cm² or less , in particular in a range of 1.2×10^{16} atoms/cm² to 1.4×10^{16} atoms/cm², more in particular in a range of 1.3×10^{16} atoms/cm² to 1.4×10^{16} atoms/cm², or and 0.9×10^{16} atoms/cm² or less, in particular in a range of 0.7×10^{16} atoms/cm² to 0.9×10^{16} atoms/cm², more in particular in a range of 0.8×10^{16} atoms/cm² to 0.9×10^{16} atoms/cm², respectively.

10. Method according to one of claims 1 to 9, wherein implanting is carried out at an energy of 49keV or less.

11. Method according to one of claims 1 to 10, wherein thinning comprises at least a first and a second thinning step.

12. Method according to claim 11, wherein a temperature treatment is carried out after the first and after the second thinning step respectively.

13. Method according to claim 11 or 12, wherein a rapid thermal anneal (RTA) step is carried out between a first and a second thinning step.

14. Method according to one of claims 11 to 13, wherein the thickness reduction of the device layer is larger for the second thinning step than for the first thinning step.

15. Method according to one of claims 1 to 4, wherein thinning comprises oxidation of the device layer.

16. Method according to one of claims 1 to 4, wherein thinning is achieved by at least one of wet etch, dry etch and etching under HCl and H.

17. Method according to one of claims 1 to 6, wherein the device layer has a thickness of less than 1000Å, in particular less than 800Å, after the thinning.

18. Method according to one of claims 1 to 7, wherein the source and the handle substrate are 300mm substrates.

19. Silicon on insulator wafer, in particular fabricated according to one of claims 1 to 8, comprising a device layer, an insulating layer and a handle substrate, characterized in that the device layer exhibits a SECCO defect density of less than 100 defects per cm^2, in particular less than 50 defects per cm^2.