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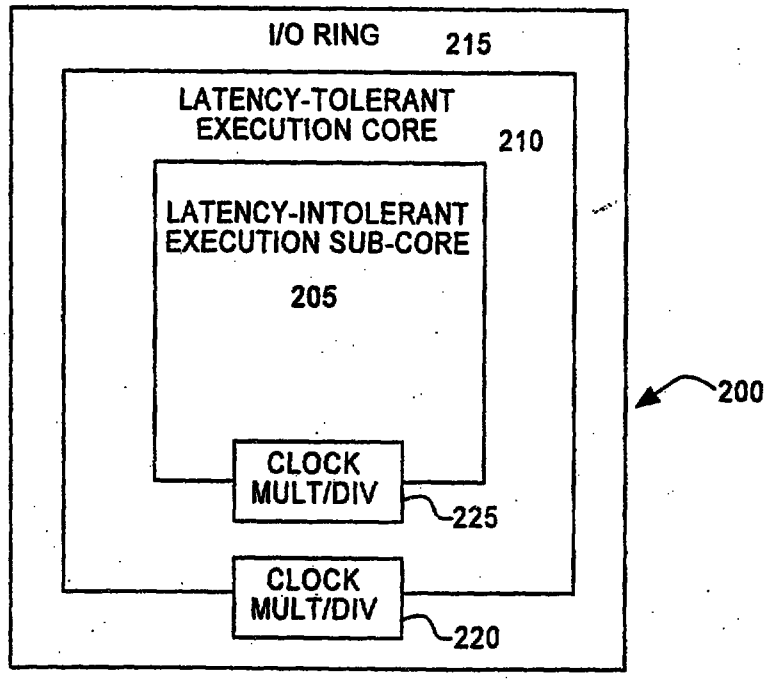
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(54) Title: PROCESSOR HAVING REPLAY ARCHITECTURE



(57) Abstract

A microprocessor having a replay architecture with an execution core for performing data speculation in executing an instruction, a delay unit for making a copy of the instruction and holding the copy for as long as the instruction takes to execute, and a checker for determining whether the data speculation was bogus. If the data speculation was bogus, the delay unit and its buffer send the copy of the instruction back to the execution core for re-execution. A multiplexor coupled to the input of the execution core selects for execution among original instructions from the instruction cache, replay instructions from the delay unit, and manufactured instructions from various other units such as the TLB or tag units, according to a priority scheme.

*(Referred to in PCT Gazette No. 34/1998, Section II)