CLAIMS

1. An integrated circuit, comprising:

a photodetection region; and

a drain region electrically coupled to the photodetection region; and

an at least partially opaque and at least partially insulative material disposed above or below at least a portion of the photodetection region and having a triangular-shaped opening configured to receive dopants therethrough,

wherein the photodetection region is configured to induce an intrinsic electric field in a direction from the photodetection region to the drain region.

2. The integrated circuit of claim 1, wherein the photodetection region comprises a dopant configuration that induces the intrinsic electric field.

3. The integrated circuit of claim 2, wherein the dopant configuration generates a potential gradient from the photodetection region to the drain region.

4. The integrated circuit of claim 3, wherein the dopant configuration is triangular-shaped.

5. The integrated circuit of any one of claims 1 to 4, further comprising:

a mask disposed above or below at least a portion of the photodetection region, the mask having a triangular-shaped opening configured to receive dopants therethrough.

65. The integrated circuit of any one of claims 51 to 4, further comprising:

a first charge storage region electrically coupled to the photodetection region,

wherein the photodetection region is configured to receive incident light in a first direction and to transfer charge carriers, generated therein in response to the incident light, to the first charge storage region in a second direction perpendicular to the first direction.

76. The integrated circuit of claim 65, wherein the photodetection region is configured to induce the intrinsic electric field in the second direction.

~~8~~7. The integrated circuit of claim ~~7~~6, wherein the opening comprises a first end and a second end spaced from the first end in the second direction, and the opening is wider, in a third direction perpendicular to each of the first and second directions, at the first end than at the second end.

~~9~~8. The integrated circuit of claim ~~8~~7, wherein the opening is at least 75% wider, in the third direction, at the first end than at the second end.

~~10~~9. The integrated circuit of claim ~~5~~1, and/or wherein the mask has a thickness of approximately 0.6 microns in a direction parallel to the first optical axis.

~~11~~10. The integrated circuit of any one of claims 1 to 9, wherein the drain region is coupled to the photodetection region by a charge transfer channel.

~~12~~11. The integrated circuit of claim ~~11~~10, further comprising:

a transfer gate electrically coupled to the charge transfer channel and configured to control a transfer of charge carriers from the photodetection region to the drain region.

~~13~~12. The integrated circuit of claim ~~12~~11, wherein the transfer gate is configured to receive a control signal and bias the charge transfer channel to transfer charge carriers using the control signal.

~~14~~13. The integrated circuit of claim ~~6~~5, further comprising a pixel comprising the photodetection region, the first charge storage region, and the drain region, wherein the pixel has an area smaller than or equal to 7.5 microns x 5 microns.

~~15~~14. A method of manufacturing the integrated circuit of any one of claims 1 to 13, the method comprising:

depositing an ~~mask~~ at least partially opaque and at least partially insulative material on at least a portion of the photodetection region; and

removing at least a portion of the ~~mask~~ at least partially opaque and at least partially insulative material to create an opening having a triangular shape.

~~16~~15. The method of claim ~~15~~14, further comprising doping the photodetection region through the opening.

16. The integrated circuit of any one of claims 1 to 13, or the method of claim 14 or 15, further comprising a mask, wherein the mask includes the at least partially opaque and at least partially insulative layer.

~~17. An integrated circuit, comprising:~~

~~a photodetection region;~~

~~a charge storage region electrically coupled to the photodetection region; and~~

~~a drain region electrically coupled to the photodetection region,~~

~~wherein the charge storage region and the drain region are positioned on a same side of the photodetection region.~~

~~18. The integrated circuit of claim 17, further comprising:~~

~~a first transfer gate configured to control a transfer of charge carriers from the photodetection region to the drain region; and~~

~~a second transfer gate configured to control a transfer of charge carriers from the photodetection region to the charge storage region.~~

~~19. The integrated circuit of claim 18, wherein:~~

~~the first transfer gate is configured to receive a first control signal and transfer charge carriers from the photodetection region to the drain region in response to the first control signal; and~~

~~the second transfer gate is configured to receive a second control signal and transfer charge carriers from the photodetection region to the charge storage region in response to the second control signal.~~

~~20. The integrated circuit of claim 19, wherein:~~

~~the first transfer gate is configured to control a transfer of excitation charge carriers, generated in response to excitation light received in the photodetection region, to the drain region; and~~

~~the second transfer gate is configured to control a transfer of fluorescent emission charge carriers, generated in response to fluorescent emission light received in the photodetection region following reception of the excitation light, to the charge storage region.~~

~~21~~17. An integrated circuit, comprising:

a first pixel comprising a first photodetection region configured to induce an electric field in a first direction; and

a second pixel comprising a second photodetection region configured to induce an electric field in a second direction substantially opposite the first direction,

wherein the first and second pixels are positioned one after another in one of the first and second directions.

~~22~~18. The integrated circuit of claim ~~21~~17, wherein:

the first pixel comprises a drain region and/or a charge storage region positioned after the first photodetection region in the first direction; and

the second pixel comprises a drain region and/or a charge storage region positioned after the second photodetection region in the second direction.

~~23~~19. The integrated circuit of claim ~~22~~18, further comprising:

a first row of pixels comprising the first pixel and each comprising a first photodetection region configured to induce an electric field in the first direction; and

a second row of pixels comprising the second pixel and each comprising a second photodetection region configured to induce an electric field in the second direction,

wherein the first row of pixels and the second row of pixels are positioned one after another in one of the first and second directions.

20. The integrated circuit of claim 18, wherein:

the first pixel comprises a first charge storage region positioned after the first photodetection region in the first direction; and

the second pixel comprises a second photodetection region positioned after the second photodetection region in the second direction.

21. A system, comprising:

the integrated circuit of any one of claims 5 to 13 and 16 to 20; and

a control circuit configured to provide control signals to transfer gates of the integrated circuit to accumulate charge carriers in the first charge storage region over a plurality of collection periods, each collection period corresponding to a pulse of excitation light.

~~24. An integrated circuit, comprising:~~

~~a photodetection region; and~~

~~at least one drain layer configured to receive incident photons and/or charge carriers via the photodetection region.~~

~~25. The integrated circuit of claim 24, wherein the at least one drain layer is positioned, in a first direction in which the photodetection region is configured to receive incident photons, after the photodetection region.~~

~~26. The integrated circuit of claim 25, wherein the at least one drain layer includes a collection layer configured to discard the charge carriers to a direct current (DC) power supply voltage when the collection layer is electrically coupled to the DC power supply voltage.~~

~~27. The integrated circuit of claim 26, wherein the collection layer comprises a same semiconductor doping type as the photodetection region.~~

~~28. The integrated circuit of claim 27, wherein the at least one drain layer further includes a protection layer disposed between the collection layer and the photodetection region, the protection layer and the collection layer having opposite conductivity types.~~

~~29. The integrated circuit of claim 25, further comprising at least one charge storage region coupled to the photodetection region by a charge transfer channel region.~~

~~30. The integrated circuit of claim 29, wherein at least a portion of the at least one drain layer is disposed after a first charge storage region of the at least one charge storage region in the first direction.~~

~~31. The integrated circuit of claim 30, wherein the at least a portion of the at least one drain layer includes at least a portion of the collection layer.~~

~~32. The integrated circuit of claim 31, wherein the at least one drain layer further comprises a first barrier region coupled to the protection layer and positioned after the first charge storage region in the first direction.~~

~~33. The integrated circuit of claim 32, wherein the first barrier region and the first charge storage region have opposite conductivity types.~~

~~34. The integrated circuit of claim 33, wherein the protection layer and the first barrier region are further coupled to a second barrier region disposed, at least in part, between the first charge storage region and the photodetection region.~~

~~35. An integrated circuit, comprising:~~

~~a plurality of pixels, each pixel of the plurality of pixels comprising a photodetection region and a charge storage region; and~~

~~a control circuit configured to control a transfer of charge carriers from the photodetection region to the charge storage region of each of the plurality of pixels.~~

~~36. The integrated circuit of claim 35, wherein each pixel of the plurality of pixels further comprises a first transfer gate configured to receive a control signal from the control circuit and control the transfer of charge carriers from the photodetection region to the charge storage region using the control signal.~~

~~37. The integrated circuit of claim 36, wherein the control signal is a sinusoidal control signal.~~

~~38. The integrated circuit of claim 37, wherein the control signal is a square wave control signal.~~

~~39. The integrated circuit of claim 36, wherein each pixel of the plurality of pixels comprises a plurality of transfer gates comprising the first transfer gate and configured to receive a~~

respective plurality of control signals from the control circuit, the plurality of control signals being out of phase from one another.

40. The integrated circuit of claim 39, wherein the plurality of control signals comprises two control signals that are 180 degrees out of phase from one another.

41. The integrated circuit of claim 39, wherein the plurality of control signals comprises three control signals that are 120 degrees out of phase from one another.

42. The integrated circuit of claim 39, wherein the plurality of control signals sums to a constant value at multiple points over time.

43. The integrated circuit of claim 39, wherein each pixel of the plurality of pixels further comprises a drain region, and the plurality of transfer gates further comprises a second transfer gate configured to control a transfer of charge carriers from the photodetection region to the drain region.

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44. An integrated circuit, comprising:

a photodetection region configured to receive incident light in a first direction; and

a surface positioned, in the first direction, before the photodetection region and configured to direct the incident photons towards the photodetection region.

45. The integrated circuit of claim 44, further comprising a charge storage region electrically coupled to the photodetection region and a transfer gate configured to control a transfer of charge carriers from the photodetection region to the charge storage region.

46. The integrated circuit of claim 44, further comprising at least one barrier elongated parallel to the first direction.

47. The integrated circuit of claim 46, wherein the at least one barrier comprises first and second barriers elongated parallel to the first direction and positioned on opposite sides of the photodetection region in a direction perpendicular to the first direction.

~~48. The integrated circuit of claim 44, wherein the surface comprises a plurality of openings.~~

~~49. The integrated circuit of claim 48, wherein the plurality of openings comprises triangular openings having bases disposed along the surface.~~

~~50. The integrated circuit of claim 49, wherein the plurality of openings comprises pyramidal openings.~~

~~51. The integrated circuit of claim 50, wherein the plurality of openings comprises a material having a refractive index greater than a refractive index of the surface.~~

~~52. The integrated circuit of claim 51, wherein the plurality of openings comprises a material having a dielectric constant greater than a dielectric constant of the surface.~~

~~53. A method of manufacturing the integrated circuit of claim 47, the method comprising removing at least a part of the surface to create the plurality of openings.~~

~~54. The method of claim 53, further comprising at least partially filling the plurality of openings with a material having a refractive index greater than a refractive index of the surface.~~