Claims

What is claimed is:

1. A memory comprising:

   a first switch transistor comprising a drain terminal, a source terminal and a gate terminal;

   a second switch transistor comprising a drain terminal, a source terminal and a gate terminal;

   a third switch transistor comprising a drain terminal coupled to the source terminal of the first switch transistor, a source terminal and a gate terminal;

   a fourth switch transistor comprising a drain terminal coupled to the source terminal of the second switch transistor, a source terminal and a gate terminal;

   a first resistive memory element comprising a first terminal coupled to the source terminal of the fourth switch transistor, and a second terminal coupled to the source terminal of the first switch transistor; and

   a second resistive memory element comprising a first terminal coupled to the source terminal of the third switch transistor, and a second terminal coupled to the source terminal of the second switch transistor.

2. The memory of claim 1, wherein when writing data to the memory, the first switch transistor and the second switch transistor are turned off, and the third switch transistor and the fourth switch transistor are turned on.

3. The memory of claim 1, wherein when reading data from the memory, the first switch transistor and the second switch transistor are turned on, and the third switch transistor and the fourth switch transistor are turned off.

4. The memory of claim 1, wherein:

   the drain terminal of the first switch transistor is coupled to a first bit line, and the gate terminal of the first switch transistor is coupled to a read word line;

   the drain terminal of the second switch transistor is coupled to a second bit line, and the gate terminal of the second switch transistor is coupled to the read word line;

   the gate terminal of the third switch transistor is coupled to a write word line, and the source terminal of the third switch transistor is coupled to a second source line; and

   the gate terminal of the fourth switch transistor is coupled to the write word line, and the source terminal of the fourth switch transistor is coupled to a first source line.

5. The memory of claim 4, wherein when writing a logic 0 to the memory, the first switch transistor and the second switch transistor are turned off, the third switch transistor and the fourth switch transistor are turned on, the first source line has a high voltage level, and the second source line has a low voltage level lower than the high voltage level.

6. The memory of claim 5, wherein when writing the logic 0 to the memory, the first resistive memory element is set to have a high resistance, and the second resistive memory element is set to have a low resistance lower than the high resistance.

7. The memory of claim 4, wherein when reading a logic 0 from the memory, the first switch transistor and the second switch transistor are turned on, the third switch transistor and the fourth switch transistor are turned off, the first source line has a high voltage level, and the second source line has the high voltage level.

8. The memory of claim 4, wherein when writing a logic 1 to the memory, the first switch transistor and the second switch transistor are turned off, the third switch transistor and the fourth switch transistor are turned on, the first source line has a low voltage level, and the second source line has a high voltage level higher than the low voltage level.

9. The memory of claim 8, wherein when writing the logic 1 to the memory, the first resistive memory element is set to have a low resistance, and the second resistive memory element is set to have a high resistance higher than the low resistance.

10. The memory of claim 4, wherein when reading a logic 1 from the memory, the first switch transistor and the second switch transistor are turned on, the third switch transistor and the fourth switch transistor are turned off, the first source line has a high voltage level, and the second source line has the high voltage level.

11. The memory of claim 4, wherein:
    the first resistive memory element comprises a top electrode coupled to the first terminal of the first resistive memory element, a bottom electrode coupled to the second terminal of the first resistive memory element, and a transition metal oxide layer formed between the top electrode of the first resistive memory element and the bottom

electrode of the first resistive memory element; and

the second resistive memory element comprises a top electrode coupled to the first terminal of the second resistive memory element, a bottom electrode coupled to the second terminal of the second resistive memory element, and a transition metal oxide layer formed between the top electrode of the second resistive memory element and the bottom electrode of the second resistive memory element.