ELIMINATION OF STI RECESS AND FACET GROWTH IN EMBEDDED SILICON-GERMANIUM (eSiGe) MODULE

ABSTRACT

A method (and semiconductor device) of fabricating a semiconductor device eliminates shallow trench isolation (STI) recess in embedded SiGe p-type field effect transistor (pFET) structures. This increases device performance by improving isolation and decreasing leakage current caused by SiGe facet growth and silicide encroachment at the STI. A mask is selectively formed over the STI and adjacent nFET regions to protect them during formation (e.g., reactive ion etching (RIE)) of the embedded source/drain (S/D) regions of the pFET. The mask also extends over the STI edge by a predetermined distance to cover a portion of the embedded S/D region disposed between the STI and gate structure. This helps protect or isolate the STI region during SiGe layer formation in the defined embedded S/D regions.

Fig.2