

Abstract

Capacitor in a semiconductor arrangement, and method for its production

The capacitor in a semiconductor arrangement, in particular a DRAM, has an electrode structure (10) containing a plurality of elements which are arranged at a distance from one another and are electrically connected by means of a connection structure (9), which is [sic] composed completely of p-conducting material with a doping $> 10^{20} \text{ cm}^{-3}$. The elements of the electrode structure are arranged one above the other or next to one another and may have a pot-shaped design. In the production methods, a layer sequence consisting alternately of a p⁻-doped and a p⁺-doped layer is produced and acquires an opening (8; 70) by means of anisotropic etching. A p⁺-type zone, which connects the layer sequence and forms the connection structure (9), is produced at least in one edge region of the opening. The p⁻-doped layers are subsequently etched selectively with respect to the p⁺-doped layers, a capacitor dielectric (11) is deposited and a counter-electrode (12) is produced.

Fig. 2