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METAL LAYERS FORMED AS A COMPOSITE OF SUB-LAYERS AND DEVICES INCLUDING SAME

Background of the Invention

This invention relates to the deposition of metal layers, such as the conductors in an integrated circuit.

In integrated circuits (ICs), metal layers are used to make electrical contact to device active areas (e.g., as electrodes to the gate, source and drain of FETs) and to interconnect devices to one another (e.g., as runners between devices on the same level of an IC or as vias between devices on different levels). In both cases, vias or windows with essentially vertical sidewalls are opened in an overlying dielectric layer to expose a portion of an underlying layer (e.g., the semiconductor active areas of devices or the commonly referred to "Metal-1" of the first level of metalization). A plug of metal from an overlying metal layer (e.g., "Metal-1" in the case of a device contacts or the commonly referred to "Metal-2" in the case of interconnects) extends through the via or window and makes an electrical connection between a metal layer and a semiconductor (device contact) or between two metal layers (interconnect). For simplicity, we will hereinafter refer to the electrical connection in both cases (metal to semiconductor, and metal to metal) as an *interconnect*.

Aluminum and aluminum alloys are the most common materials used for such metal layers. Typically, these Al-based layers are deposited as single layers by means of a single-step deposition such as sputtering. Al-based, single-layer metalization, however, suffers several major problems when used to form interconnects in vias or windows: (1) poor step coverage at a top edge of the window, (2) pinch-off or a lack of metal deposition along a sidewall of the window, and (3) overhang or excessive metal above a top edge of the window. Any one or more of these problems may adversely affect IC reliability. Thus, poor step coverage and overhang often produce voids (an absence of metal) in the windows which reduce the ability of the interconnect to carry current. Pinch-off, on the other hand, causes electron crowding, and hence undesirably high current densities, in the sidewall regions where metal is absent.

Lack of adequate step coverage in vertical or near vertical-walled openings or vias, especially those with aspect ratios greater than unity, is often addressed in the prior art by using tapered (i.e., sloped) sidewalls. However, this taper technology results in a larger pitch. Because a larger pitch means increased spacing between parallel metal conductors (e.g., runners), any significant taper is

likely to render this technology unsuitable for design rules of, say, 0.5μm, 0.3μm or less.

Other prior art approaches to filling high aspect ratio vias entail multiple step metalization processes. In one case, a thick metal layer is deposited at a cold temperature, and the remainder of the metal is deposited as the temperature is ramped up to allow for reflow of the metal layer. See U.S. Patent 4,970,176 granted to C. J. Tracy et al. on November 13, 1990. In another case, a very thin layer of small grain aluminum is deposited at a cold temperature, typically below 350°C. Deposition is stopped until the temperature is increased to the required deposition temperature, over 500°C, and then deposition of aluminum is resumed. See U.S. Patent 5,108,951 (col. 4, lines 1-9) granted to F. E. Chen et al. on April 28, 1992. The Chen et al. patent goes on to describe an alternative technique in which aluminum is deposited continuously while the wafer is being heated. That is, a small amount of aluminum is deposited at or below 350° C, and as the wafer gradually heats to the desired deposition temperature (400-500 ° C), aluminum deposition continues. Chen et al. reports that this technique gives a layer of aluminum which is deposited with very small grain sizes, tending to minimize grain size growth at later stages (col. 4, lines 10-21).

None of these multi-step metalization processes for filling high aspect ratio vias, however, recognizes the important relationship between interconnect performance and the need for a plug which has both a large grain size and a particular texture (i.e., grain orientation).

Thus, a need remains in the art for a metalization scheme that addresses the above problems in fabricating interconnects in essentially vertical-walled vias or windows. A particular need remains for such a metalization scheme which is suitable for high aspect ratio vias such as those present at sub-half-micron design rules.

Summary of the Invention

These problems are addressed in accordance with one aspect of the invention, a method of making integrated circuits in which an opening (e.g., via or window) is filled with an Al-based plug by depositing a texture control Ti layer under conditions which yield a predetermined orientation in subsequently deposited Al-based layers. Then a plurality of Al-based sublayers are deposited: first, a fine grained first sublayer with essentially a <111> orientation is deposited at a relatively cold temperature on the Ti layer; next, a second sublayer is deposited on the first sublayer while the temperature is ramped up from the cold temperature to a peak

deposition temperature, so that, during the ramp up, a Ti-aluminide layer is formed at the interface between the Ti layer and the first sublayer, and so that the grain size of the Al-based material increases; and next, a third sublayer is deposited at the peak temperature. During deposition of the third sublayer, the entire microstructure of the plug adjusts itself so that the plug comprises a single grain or at most three grains, and, in addition, the texture of the entire plug has essentially a <111> orientation.

Another aspect of the invention is an integrated circuit including a Ti-aluminide layer and an Al-based plug which fills an opening (e.g., a via or window). The texture of the Al-based plug has essentially a <111> orientation, and the plug itself comprises a single grain, or at most three grains.

Brief Description of the Drawings

The invention, together with its various features and advantages, can be readily understood from the following more detailed description taken in conjunction with accompanying drawing, in which:

FIG. 1 is a schematic rendering of the cross-section of a plug in a via which interconnects Metal-1 and Metal-2 layers in an IC;

FIGS. 2-6 show schematically the sequential steps in the fabrication of the plug of FIG. 1 in accordance with one embodiment of the invention; and

FIG. 7 depicts FIG. 6 with various sublayers shown as a single layer.

In the interests of clarity of illustration, the figures have not been drawn to scale.

Detailed Description

An integrated circuit (IC) typically comprises a semiconductor body (e.g., a silicon substrate or a silicon epitaxial layer on a substrate) in which the active regions of devices (e.g., FETs, bipolar transistors) or the passive regions of other devices (e.g., resistors, capacitors) are formed. Devices on different parts of a wafer are typically insulated from one another by insulative (e.g., oxide) regions, and selected devices are interconnected by means of conductive (e.g., metal) layers. Due to the complexity of the interconnection patterns, the metal layers are formed on more than one level (commonly two levels, but increasingly three or four levels).

Different levels of metal layers, as well as metal layers and semiconductor device areas, are electrically insulated from one another by one or more insulative (e.g., silicon oxide or silicon nitride) layers, except in those areas where electrical connections are desired. These insulative layers are sometimes referred to as interlayer dielectrics. In those areas, vias or windows are opened in the insulative layer(s) and then filled with metal plugs. FIG. 1 schematically illustrates a

portion of an IC 10 which includes a composite Metal-1 layer 12 on Si body 14. For example, body 14 may comprise a wafer or substrate with or without a Si epitaxial layer and typically with silicon oxide isolation regions separating devices and/or device regions as described above, but not shown. Thus, although the following description relates to interconnects between Metal-1 and Metal-2, the invention is also applicable to connections between Metal-1 and semiconductor device regions, or between Metal-2 and higher level metals.

Continuing with the description of the Metal-1 to Metal-2 interconnect, FIG. 1 shows that Metal-1 layer 12 is interconnected with composite Metal-2 layer 16 by means of metal plug 18. The Metal-1 and Metal-2 layers are separated from one another by insulative layer 20 in which an opening (e.g., a via or window) is formed to allow plug 18 to extend from Metal-2 to Metal-1. In accordance with one aspect of the invention, both the plug 18 and the Metal-2 layer 16 are formed by depositing a texture control Ti layer 24 under conditions which yield a predetermined orientation in subsequently deposited Al-based layers. More specifically, the texture control Ti layer 24 should be deposited under conditions which produce a close-packed Ti layer having essentially a basal plane (002) orientation. This basal plane of Ti has the same atomic configuration as the (111) plane of Al-based layers, which thereby induces Al-based layers to have essentially a <111> orientation when deposited on such a Ti layer.

After the Ti texture control layer 24 is deposited, a plurality of Al-based sublayers are sequentially deposited, each under different deposition conditions which result in grain boundary diffusion, recrystallization and grain growth. For example, the sublayers may be deposited at different deposition rates and under conditions which produce a plug 18 having essentially a <111> orientation and having a single grain or at most three grains. Although the ability to form a plug with as little as a single grain is determined by the inventive fabrication process, the maximum size of the grain(s) is determined by the dimensions of the plug (or of the via in which it is formed). In general, fewer grains means fewer grain boundaries which, in turn, means fewer defects and, hence, better electromigration characteristics and less stress-induced voiding. Thus, a single grain is optimum in this regard, but two or three grains still provide excellent performance.

FIGS. 2-6 illustrate the sequential steps in the fabrication of such an interconnect. In this example, the plug 18 and the laterally extending field portions are deposited initially as three sublayers. However, the invention is not limited in scope to three sublayers; more than three (e.g., four sublayers or more) are also

suitable.

In the following illustrative description, it will be assumed that all metal layers are deposited by sputtering, although the invention is not limited to this technique (e.g., evaporation may also be suitable). In addition, the process is conveniently carried out in a state-of-the art cluster tool or machine with individual deposition chambers. To improve deposition uniformity across a wafer, sputtering is preferably performed using planar targets.

In a first step, shown in FIG. 2, a well-known composite barrier layer 22 is deposited on the bottom and sidewalls of via 19 and on the top of oxide layer 20. The barrier layer illustratively comprises two layers (not shown): a refractory metal (e.g., Ti) formed on the surface of the via and a refractory metal nitride (e.g., TiN) formed on the refractory metal. Deposition of barrier layer 22 typically takes place at a substrate or wafer temperature in the range of about 25-400°C. Next, as shown in FIG. 3, a thin ($\leq$250Å) texture control Ti layer 24 is deposited on barrier layer 22, under conditions which produce a close-packed structure with essentially a basal plane (002) orientation. Thus, layer 24 is deposited at a substrate or wafer temperature in the range of about 25-400°C; preferably at a cold temperature of $\leq$100°C (50°C has been found to be suitable). During subsequent deposition of Al-based metals in via 19, a layer of Ti-aluminide is formed at the interface between layer 24 and the first deposited Al-based layer. The texture of the Al-based metals has essentially a <111> orientation, and the plug 18 ultimately formed comprises a single grain (or at most three). Layer 24 also improves mechanical and electrical reliability.

After deposition of layer 24, three Al-based metal sublayers 16.1, 16.2 and 16.3 are sequentially deposited as shown in FIGS. 4-6. However, if after deposition of layer 24 is complete, the substrate or wafer temperature is above about 100°C, then the substrate or wafer should be cooled before the deposition of the first sublayer 16.1.

The sublayers comprise Al-based metals such as Al-based alloys. Suitable alloys include Al-Cu, Al-Si-Cu, Al-Sc, Al-Ge, Al-Sc-X, Al-Ge-X (where X=Si and/or Cu), Al-Pd-Nb, Al-Pd-Mg, Al-Hf-Ti, etc. The composition of the AlCu or AlSiCu alloys may comprise about 0.05-5.0% Cu by weight and 0.05-5.0% Si by weight, and typically 0.5-2.0% Cu and 0.5-1.5% Si by weight.

The first sublayer 16.1, shown in FIG. 4, is relatively thin and serves as a nucleation layer for deposition of the second sublayer. Sublayer 16.1 has a relatively small average grain size (e.g., $\leq$2500Å , typically 1000-1700 Å) which is

achieved by deposition at a cold substrate or wafer temperature of about 50-100°C. Illustratively, deposition also takes place at a relatively high deposition rate and at high power (e.g., 9-11 kW and about 160 to 190 Å/sec.). The typical thickness of sublayer 16.1 is about 30-50% of the total thickness of the three sublayers.

At the end of its deposition, the second sublayer 16.2, shown in FIG. 5, has a much larger average grain size than sublayer 16.1; typically about 2-3 times larger, or illustratively about 2500 – 8000 Å, depending on the dimensions of the plug. Sublayer 16.2 is deposited while the substrate or wafer temperature is ramped up from the deposition temperature of sublayer 16.1 to a peak temperature in the range of about 400-500°C (typically 460-500°C). Illustratively, sublayer 16.2 is deposited at a much lower deposition rate (e.g., about 10 to 30 Å/sec.) and at a much lower power (e.g., 0.5-1.5 kW) than sublayer 16.1. During the deposition of sublayer 16.2, the previously-mentioned Ti-aluminide compound forms, typically at a temperature of about 300-350°C, at the interface between sublayer 16.1 and Ti layer 24. Depending on the relative thicknesses of the Ti layer 24 and the sublayer 16.1, the former may or may not be totally converted to Ti-aluminide. If not, a portion of Ti layer 24 remains in the plug when the IC is completed. In addition, during this step the deposited metal (M) flows into the vias (FIG. 5) typically to a thickness which is about 50-70% of the total thickness of the three sublayers (or of the Metal-2 layer 16).

At the end of its deposition, the third sublayer 16.3, shown in FIG. 6, has a relatively large average grain size (e.g., 2500-10,000Å), depending on the dimensions of the plug. This characteristic is achieved by deposition at the peak temperature of the ramp up used in the previous step (e.g., at 460-500°C). Illustratively, sublayer 16.3 is also deposited at the relatively high deposition rates used for first sublayer 16.1. Importantly, during this step, the microstructure of the plug 18 adjusts itself so that the plug comprises only a single large size grain or at most three large sized grains. Moreover, the texture of the plug has essentially a <111> orientation.

As mentioned previously, the maximum grain size is determined by the dimensions of the plug. For example, a plug which is 8000 Å high and 8000 Å wide may contain a single grain of 8000 Å size or two grains each of 8000x4000 Å size.

The ability of the invention to realize a plug which comprises a single <111>-oriented grain (or at the most three) enables the via to be filled, as shown in FIG. 7, without the attendant prior art problems of pinch off, overhang, voids, etc., as well as with improved electromigration properties and reduced stress-induced

voiding. Because of the presence of a single grain (or at most three) in the plug area, FIG. 7 does not depict the various sublayers of Metal-2 layer 16.

In addition, our TEM investigations have also uncovered the presence of small material islands (of the order of 10 Å in size) at the interface between sublayers 16.1 and 16.2, before the deposition of sublayer 16.3. The likely composition of the islands comprises a silicon oxide, an aluminum oxide or a solute-bearing precipitate of aluminum (e.g., $CuAl_2$). We have found that these islands may desirably inhibit interface diffusion, initially pin the grain boundaries of the Al-based layers (which allows for a <111> texture), and/or prevent void linkage due to stress-induced voiding. Thus, device lifetimes are increased.

It is to be understood that the above-described arrangements are merely illustrative of the many possible specific embodiments which can be devised to represent application of the principles of the invention. Numerous and varied other arrangements can be devised in accordance with these principles by those skilled in the art without departing from the spirit and scope of the invention. In particular, although the principles of the invention are described in terms of forming interconnects and filling openings, they are equally applicable to covering steps and forming metal layers in general.

In addition, the sublayer deposition steps may be undertaken in the same deposition chamber by keeping the wafer or substrate heater off during the deposition of the first sublayer, turning it on at the beginning of the deposition of the second sublayer and leaving it on until all sublayer depositions are complete. Forming the plug in this manner allows multiple chamber processing in the cluster machine or tool because two or more chambers can be used for parallel processing of the sublayer deposition, thereby increasing throughput. Furthermore, the second sublayer may be deposited at an initial temperature which is less than, equal to, or greater than the deposition temperature of the first sublayer.

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Claims:

1. An integrated circuit (10) comprising

first and second layers, and

an interconnect connecting said first and second layers to one another, characterized in that:

said interconnect comprises a Ti-aluminide layer and an Al-based layer (16) disposed on said aluminide layer, said Al-based layer (16) comprising at most three grains and having essentially a <111> orientation.

2. The integrated circuit (10) of claim 1 further including a Ti layer (24), said aluminide layer being disposed on said Ti layer (24).

3. The integrated circuit (10) of claim 2 wherein said Ti layer (24) has a close-packed structure with essentially a (002) basal plane orientation.

4. The integrated circuit (10) of claim 3 wherein said Ti layer (24) is disposed on a TiN layer disposed on a second Ti layer.

5. A method of fabricating an integrated circuit (10) which includes a composite metal layer(16), characterized in that said metal layer (16) is formed by the steps of:

depositing a texture control Ti layer at a first temperature so that said Ti layer (24) has essentially a (002) basal plane orientation and subsequently deposited Al-based layers (16.1, 16.2, 16.3) have essentially a <111> orientation,

depositing an Al-based first sublayer (16.1) at a second temperature on said Ti layer (24),

while increasing the temperature from a third temperature to a peak temperature greater than said second temperature, depositing an Al-based second sublayer (16.2) on said first sublayer (16.1) so that a Ti-aluminide layer forms at least at the interface between said Ti layer (24) and said first sublayer (16.1), and so that, at the end of its deposition, the average grain size of said second sublayer (16.2) is greater than that of said first sublayer (16.1), and

at said peak temperature depositing an Al-based third sublayer (16.3) on said second sublayer (16.2) so the microstructure of said sublayers (16.1, 16.2, 16.3) adjusts itself to produce at most three grains.

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6. The method of claim 5 wherein said Ti layer (24) is deposited on a TiN layer formed on a second Ti layer.

7. The method of claim 5 wherein said first temperature during deposition of said Ti layer (24) is in the range of approximately 25 – 100°C, said second temperature during deposition of said first sublayer (16.1) is in the range of approximately 50 – 100°C, said third temperature during the deposition of said second sublayer (16.2) is less than approximately 100°C, and said peak temperature during the deposition of said third sublayer (16.3) is in the range of approximately 400 – 500°C.

8. The method of claim 5 wherein said first sublayer (16.1) is deposited to have an average grain size of less than about 2500Å, said second sublayer (16.2) is deposited to have an average grain size in the range of about 2500-8000 Å, and said third sublayer (16.3) is deposited to have an average grain size in the range of about 2500 – 10,000Å.

9. The method of claim 5 wherein said aluminide layer is formed under conditions which consume the entirety of said texture control Ti layer (24).

10. The method of claim 5 wherein said aluminide layer is formed under conditions which consume only a portion of said texture control Ti layer (24).

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