

ABSTRACT

The present disclosure includes a memory device including a first vertical plug and a second vertical plug that are arranged to be adjacent to each other, a first select line contacting the first
5 vertical plug, a second select line over a same layer as the first select line and contacting the second vertical plug, and an isolation pattern overlapping with a portion of the first vertical plug and a portion of the second vertical plug and separating the first select line from the second select line.

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FIG. 6A