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Abstract

A video display system comprises: a video display (244); first and signal processors (356, 354) for cropping first and second video signals (Y_MN, YUV_AX) representative of first and second pictures; a circuit (312) for generating a side-by-side display format of the pictures on the video display; and, a panning control circuit (340, 320), responsive to panning command signals, for positioning said pictures in the side-by-side display format and for independently panning the pictures, as positioned. The panning control circuit generates independent fixed and variable delays for controlling line memories in the signal processors. Fixed delays control picture positions and variable delays control panning.

FIGURE 3

