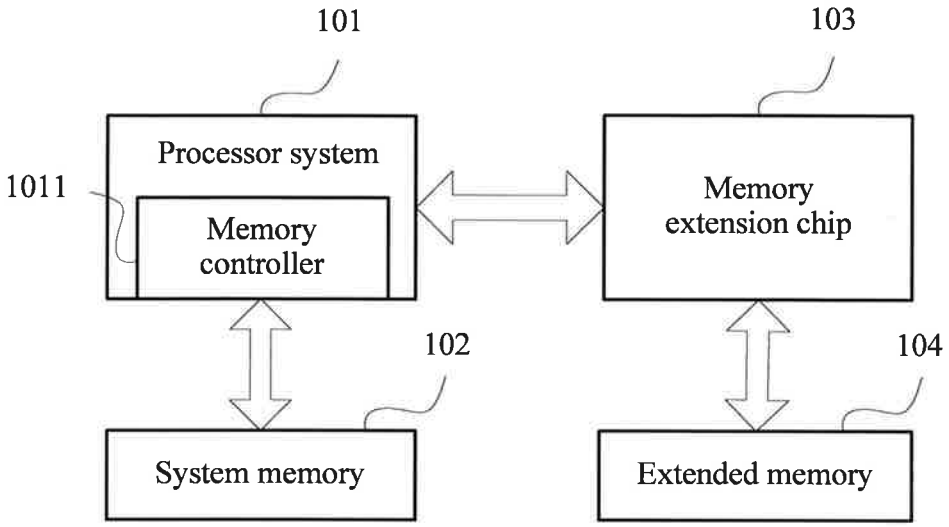

101
103
Processor system
1011
Memory controller
Memory extension chip
102
104
System memory
Extended memory

FIG. 1

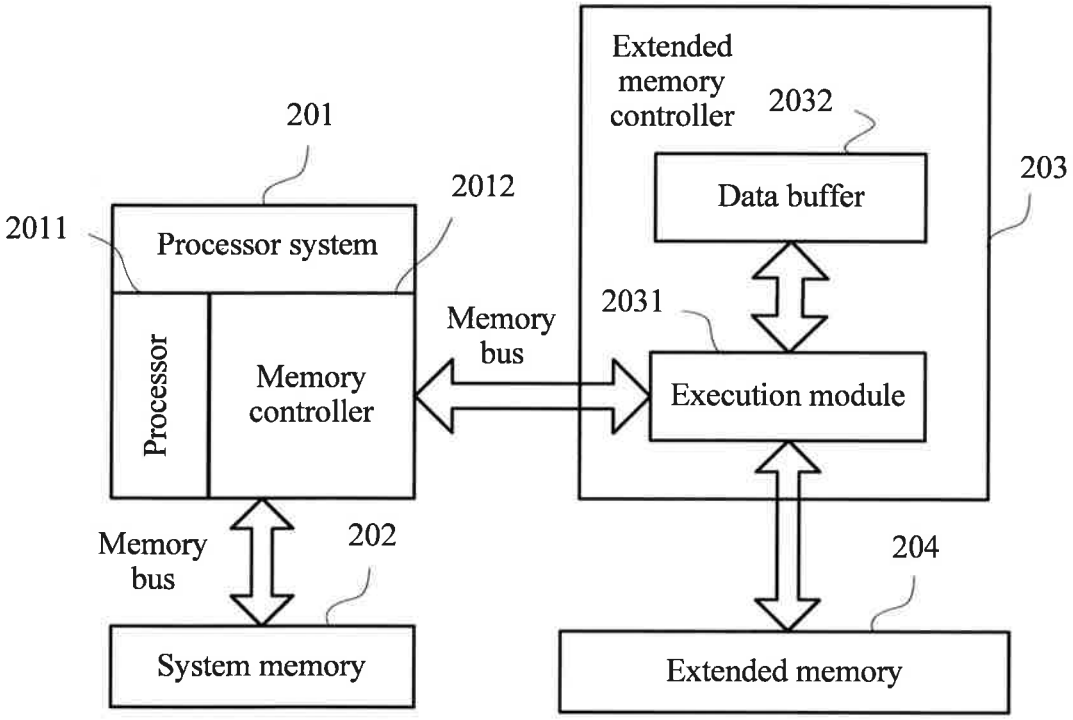

Extended memory controller
2032
201
Data buffer
203
2012
2011
Processor system
2031
Memory bus
Processor
Memory controller
Execution module
Memory bus
202
204
System memory
Extended memory

FIG. 2

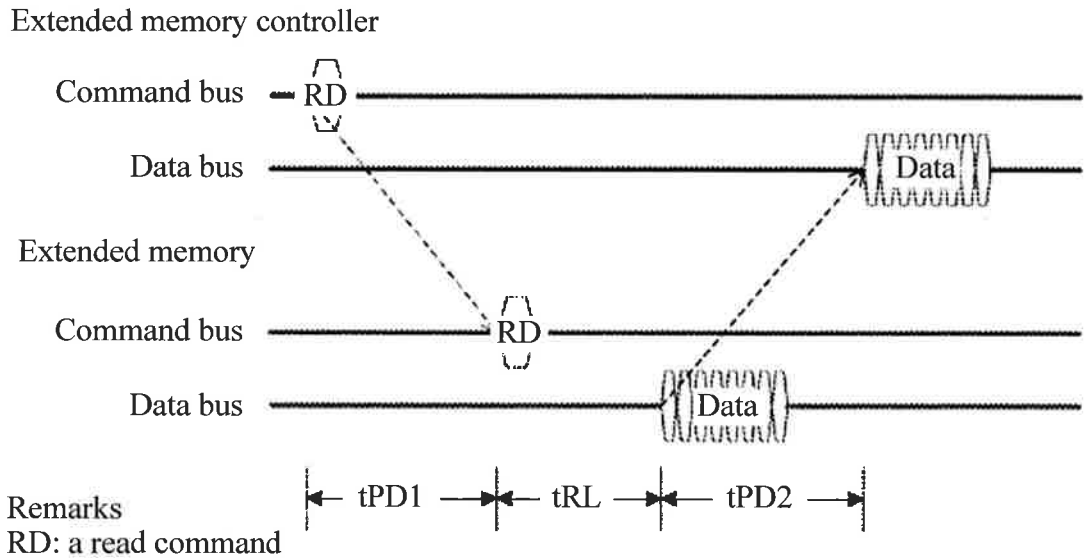
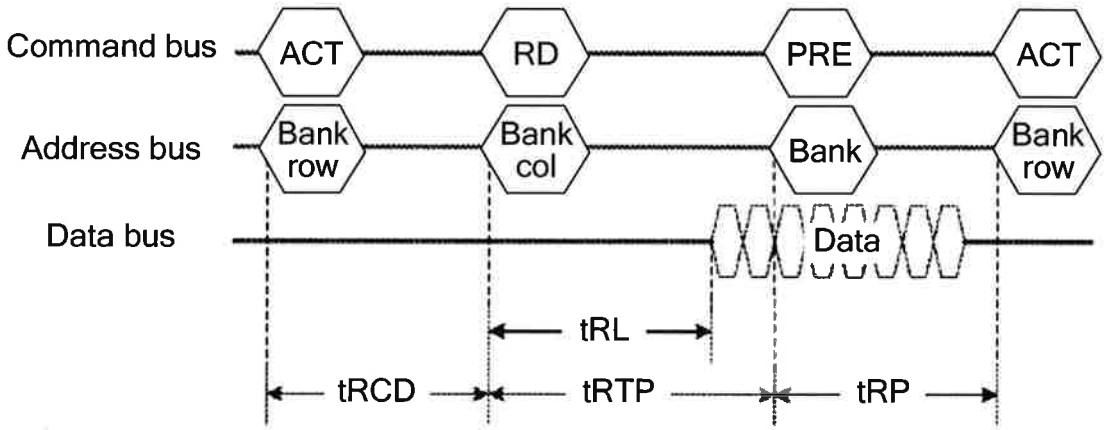


FIG. 3



Remarks:
ACT: activate, an activate instruction;
RD: a read instruction, a read data instruction;
PRE: a pre-charge instruction, a pre-charge instruction;
Bank row: a bank address and a row address;
Bank col: a bank address and a column address;
Bank: a bank address

FIG. 4

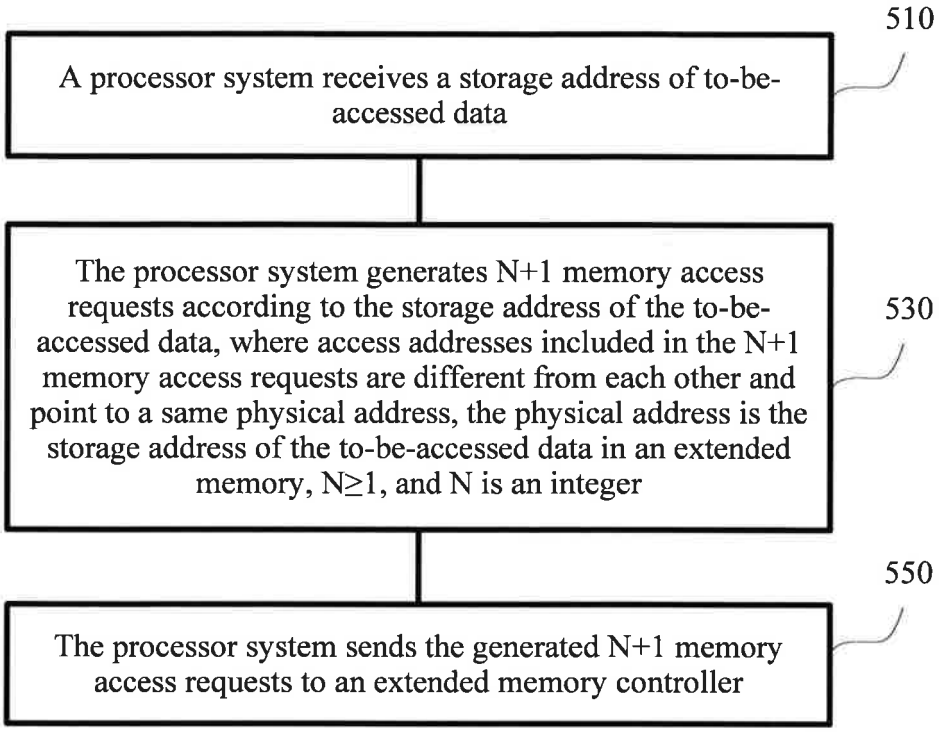

510
A processor system receives a storage address of to-be-accessed data
The processor system generates N+1 memory access requests according to the storage address of the to-be-accessed data, where access addresses included in the N+1 memory access requests are different from each other and point to a same physical address, the physical address is the storage address of the to-be-accessed data in an extended memory, N≥1, and N is an integer
530
550
The processor system sends the generated N+1 memory access requests to an extended memory controller

FIG. 5A

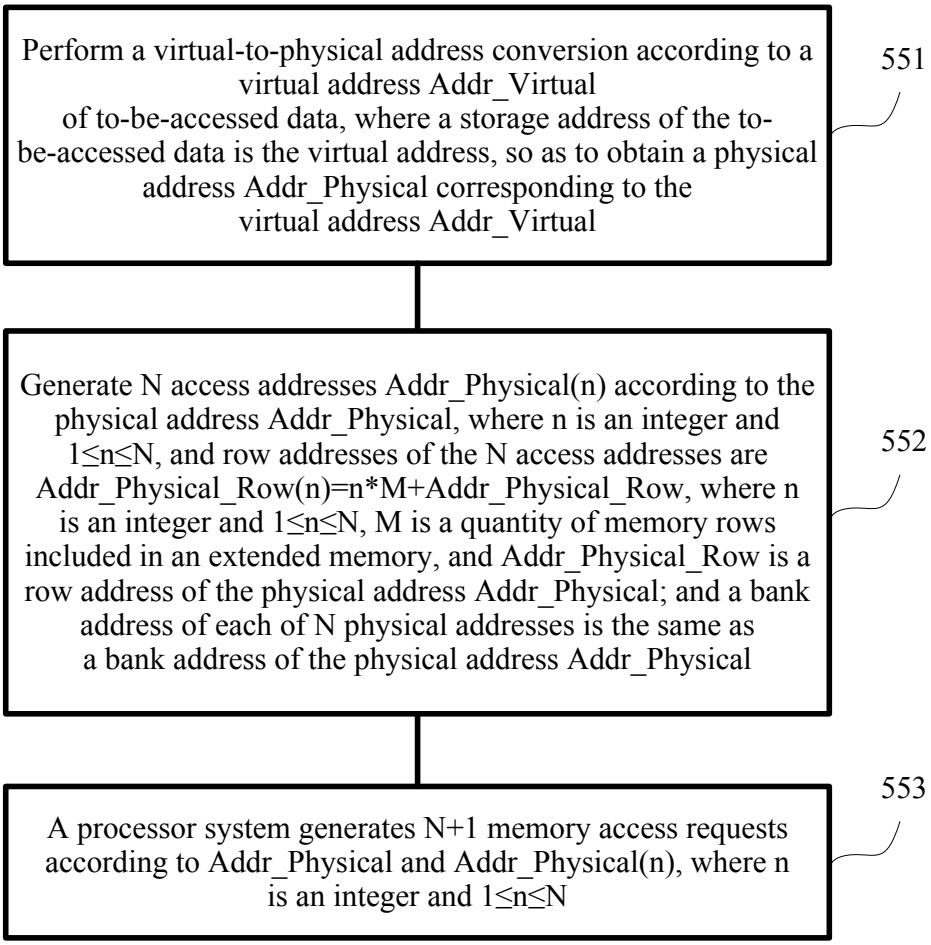

Perform a virtual-to-physical address conversion according to a virtual address Addr_Virtual of to-be-accessed data, where a storage address of the to-be-accessed data is the virtual address, so as to obtain a physical address Addr_Physical corresponding to the virtual address Addr_Virtual
551
Generate N access addresses Addr_Physical(n) according to the physical address Addr_Physical, where n is an integer and 1≤n≤N, and row addresses of the N access addresses are Addr_Physical_Row(n)=n*M+Addr_Physical_Row, where n is an integer and 1≤n≤N, M is a quantity of memory rows included in an extended memory, and Addr_Physical_Row is a row address of the physical address Addr_Physical; and a bank address of each of N physical addresses is the same as a bank address of the physical address Addr_Physical
552
A processor system generates N+1 memory access requests according to Addr_Physical and Addr_Physical(n), where n is an integer and 1≤n≤N
553

FIG. 5B

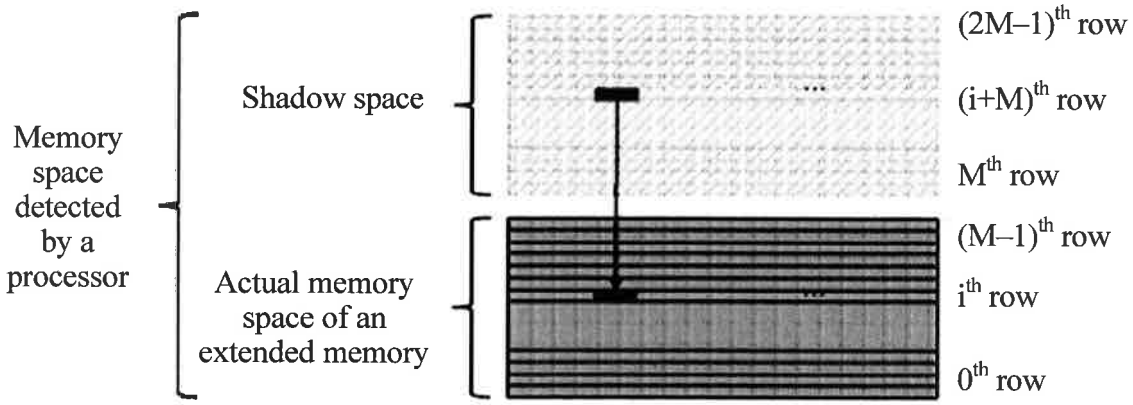

Memory space detected by a processor
Shadow space
Actual memory space of an extended memory
(2M–1)th row
(i+M)th row
Mth row
(M–1)th row
ith row
0th row

FIG. 6

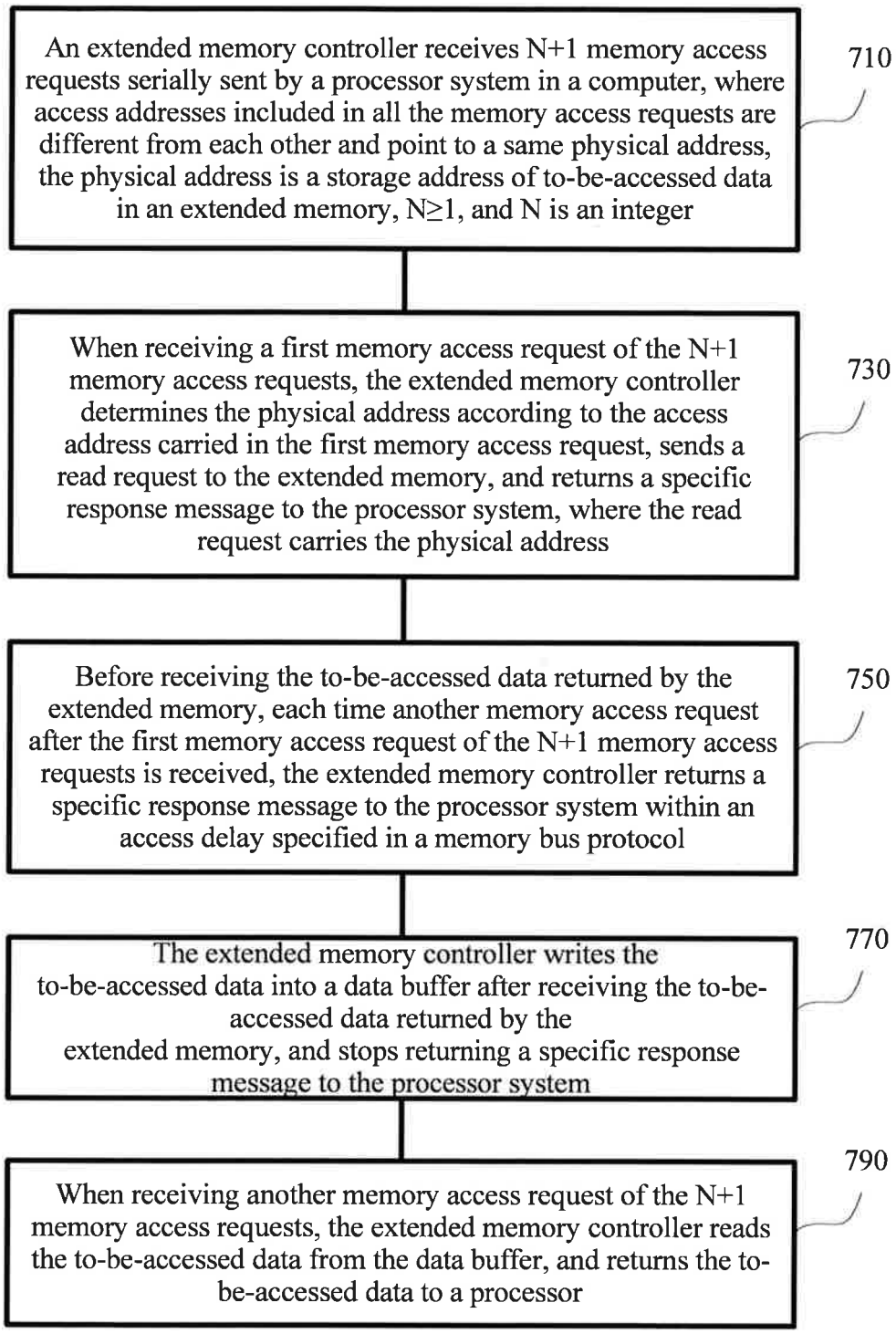

An extended memory controller receives N+1 memory access requests serially sent by a processor system in a computer, where access addresses included in all the memory access requests are different from each other and point to a same physical address, the physical address is a storage address of to-be-accessed data in an extended memory, N≥1, and N is an integer
710
When receiving a first memory access request of the N+1 memory access requests, the extended memory controller determines the physical address according to the access address carried in the first memory access request, sends a read request to the extended memory, and returns a specific response message to the processor system, where the read request carries the physical address
730
Before receiving the to-be-accessed data returned by the extended memory, each time another memory access request after the first memory access request of the N+1 memory access requests is received, the extended memory controller returns a specific response message to the processor system within an access delay specified in a memory bus protocol
750
The extended memory controller writes the to-be-accessed data into a data buffer after receiving the to-be-accessed data returned by the extended memory, and stops returning a specific response message to the processor system
770
When receiving another memory access request of the N+1 memory access requests, the extended memory controller reads the to-be-accessed data from the data buffer, and returns the to-be-accessed data to a processor
790

FIG. 7

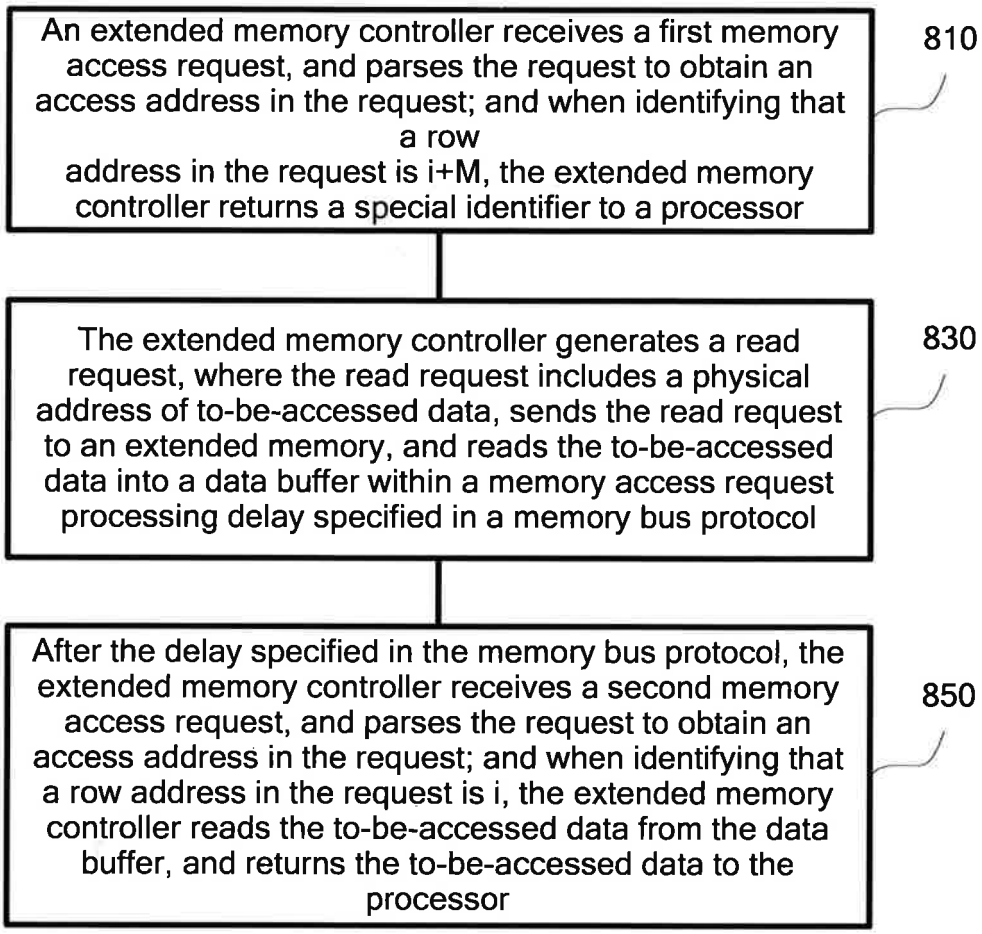

An extended memory controller receives a first memory access request, and parses the request to obtain an access address in the request; and when identifying that a row address in the request is i+M, the extended memory controller returns a special identifier to a processor
810
The extended memory controller generates a read request, where the read request includes a physical address of to-be-accessed data, sends the read request to an extended memory, and reads the to-be-accessed data into a data buffer within a memory access request processing delay specified in a memory bus protocol
830
After the delay specified in the memory bus protocol, the extended memory controller receives a second memory access request, and parses the request to obtain an access address in the request; and when identifying that a row address in the request is i, the extended memory controller reads the to-be-accessed data from the data buffer, and returns the to-be-accessed data to the processor
850

FIG. 8

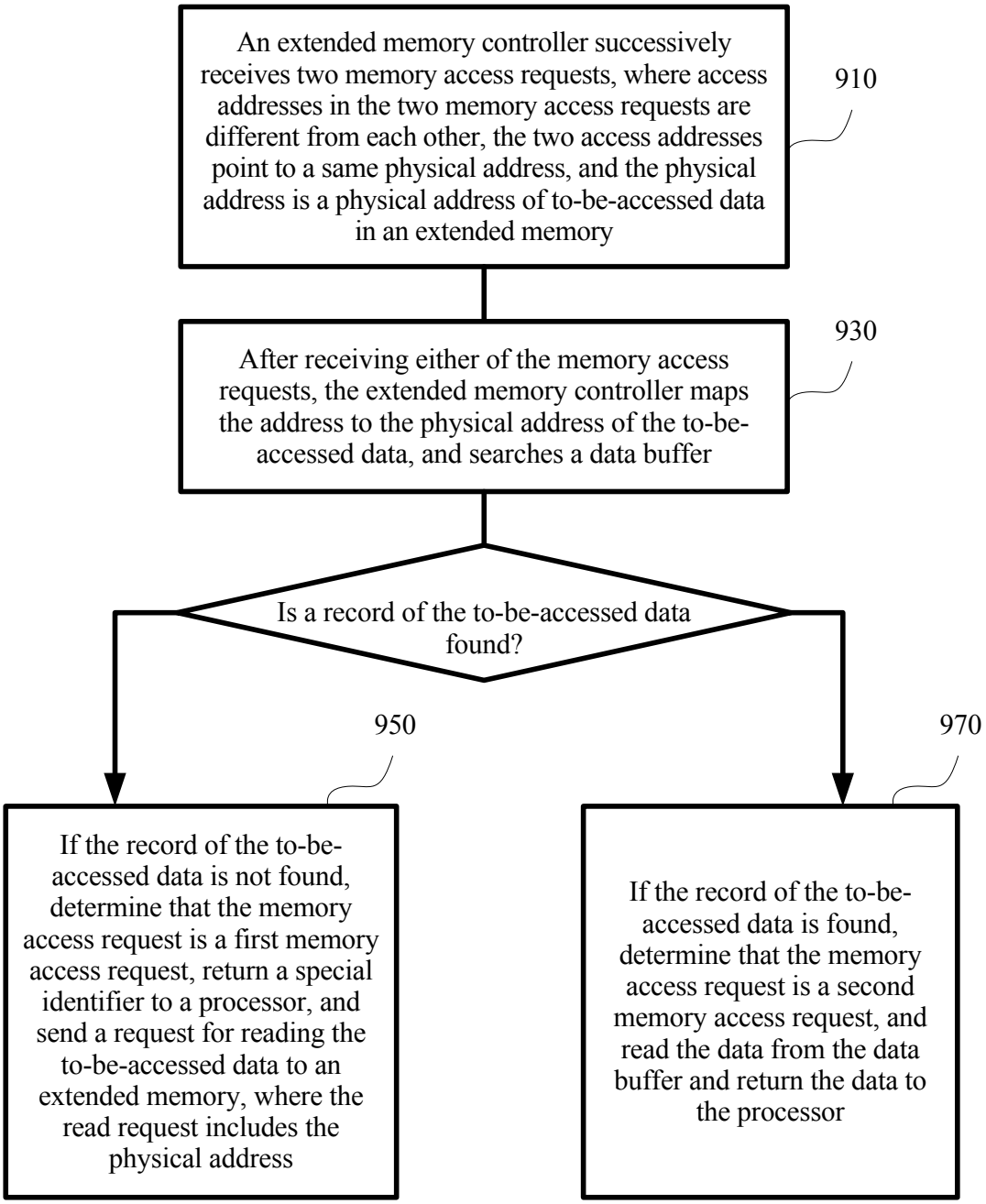

An extended memory controller successively receives two memory access requests, where access addresses in the two memory access requests are different from each other, the two access addresses point to a same physical address, and the physical address is a physical address of to-be-accessed data in an extended memory
910
After receiving either of the memory access requests, the extended memory controller maps the address to the physical address of the to-be-accessed data, and searches a data buffer
930
Is a record of the to-be-accessed data found?
950
If the record of the to-be-accessed data is not found, determine that the memory access request is a first memory access request, return a special identifier to a processor, and send a request for reading the to-be-accessed data to an extended memory, where the read request includes the physical address
970
If the record of the to-be-accessed data is found, determine that the memory access request is a second memory access request, and read the data from the data buffer and return the data to the processor

FIG. 9

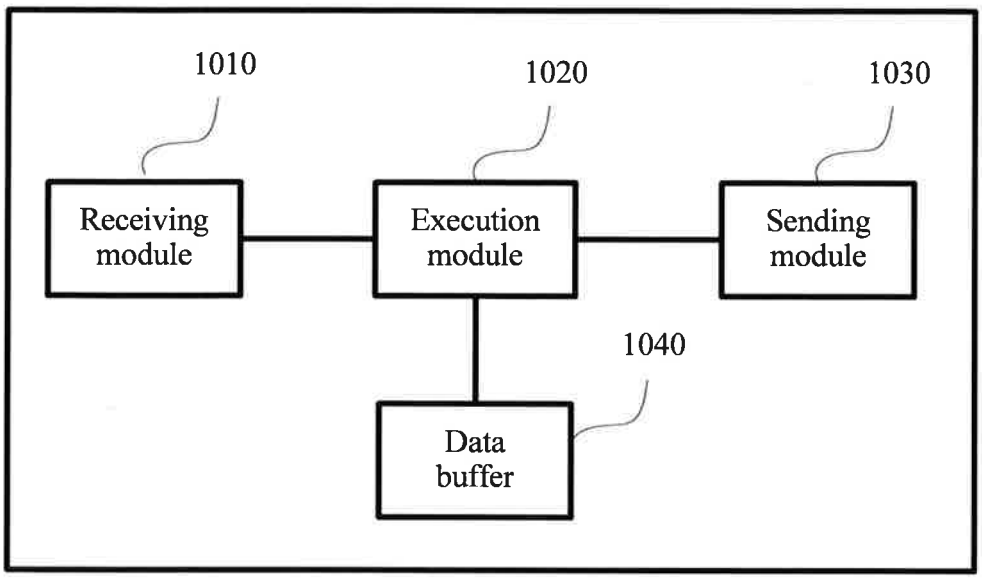

1010
1020
1030
Receiving module
Execution module
Sending module
1040
Data buffer

FIG. 10