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"A SEMICONDUCTOR ROM".

The present invention relates to a semiconductor ROM (read only memory).

A known circuit is designed to correct erroneous data read out from a defective memory cell, by the use of, e.g. the Hamming code or the
5 cyclic code (hereinbelow, termed "ECC (error correcting code) circuit").

We have investigated the possibility of building the ECC circuit in a semiconductor ROM to the end of correcting erroneous data read out from
10 a defective memory cell in the semiconductor ROM. However, when the ECC circuit is provided within the semiconductor ROM, the error correcting operation renders the read-out access time of the ROM long
15 and the operating speed thereof much lower. Moreover, a memory array must be provided with memory cells for redundant bits, and the arrangement of the ECC circuit is complicated, resulting in the disadvantage that the chip size of the semiconductor
20 ROM becomes large.

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It is an object of the present invention to provide a semiconductor ROM which is provided with an error correcting function without affecting the enhancement in the operating speed of the ROM on account
5 of the delay in the read-out access thereof.

Another object is to provide a semiconductor ROM which is furnished with an error correcting function without increasing the size of the chip.

We have taken note of the fact that erroneous
10 data read out from a defective memory cell in a ROM may be corrected merely by inverting the data.

According to the present invention there is provided a semiconductor ROM including:

(a) a memory array which includes a plurality
15 of memory cells;

(b) a selection circuit which selects one of the memory cells in response to input address signals;

(c) a detection circuit which is capable of detecting predetermined combinations of the input
20 address signals and providing a detection signal to identify a defective memory cell in the memory array;

(d) an output circuit which receives a one bit signal read out from said memory array and which delivers a signal of a logic level corresponding to said signal
25 read out from said memory portion when no detection signal is provided from said detection circuit, and a signal of a logic level not corresponding to said signal

read out from said memory portion when a detection signal is provided from said detection circuit;

whereby any erroneous data read out from a defective memory cell is inverted on the basis of
5 detecting signal to provide a corrected output signal.

Thus, with the above construction, the address information of a defective memory cell is stored within a semiconductor ROM in advance. In parallel with the information read-out operation of the defective memory
10 cell, the address information thereof is distinguished as the address information of the defective memory cell. As a result, a correcting signal is formed. Erroneous data read out from the defective memory cell is inverted on the basis of the correcting signal, whereupon the
15 corrected data is transmitted out of the ROM.

The defective memory cell is attributed to the imperfection of ROM producing technology as stated below. A photoresist film which is used for e.g. selectively implanting impurity ions into a
20 semiconductor substrate or selectively etching an insulating film or conductor layer is not removed agreeably to a desired pattern or comes to have undesired pinholes in many cases because of defects, moles or dust, which exist in or on a mask for
25 selectively exposing the photoresist film to light. When the photoresist film having such defects is used, the impurity ions cannot be implanted into the

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desired surface of the semiconductor substrate, or they are implanted into the undesired surface thereof. Further, the insulating film or conductor layer is not processed into the pattern as desired. The
5 insulating film, such as silicon oxide film, which is deposited on a semiconductor substrate, often has undesired uneven parts due to motes or dust. The conductor layer such as evaporated aluminium film becomes thin in its part corresponding to the step part
10 of an underlying surface on which it is to be deposited, because of the directivity of evaporation, with the result that the thin part is liable to disconnection.

With the above constructional features,
15 not only such defective memory cells ascribable to the imperfection of the ROM producing technology, but also memory cells as stated below are deemed defective memory cells.

In the case where, after the completion
20 of the design of a ROM, it is desired to change information to be retained by some memory cells, these memory cells do not deliver output information to be expected and can be regarded as defective memory cells.

25 Accordingly, it is to be understood that the "defective memory cell" signifies a memory cell which does not provide the correct output information.

The present invention will now be described in greater detail by way of example with reference to the accompanying drawings, wherein:-

Figure 1 is a block circuit diagram of a preferred form of a semiconductor ROM;

Figure 2 is a circuit diagram showing an essential portion of the semiconductor ROM shown in Figure 1; and

Figure 3 is a circuit diagram showing an example of a memory array of the semiconductor ROM.

Referring first to Figure 1, it should be noted that although not especially restricted thereto, circuit blocks enclosed with a two-dot chain line are formed on a single semiconductor substrate by a known semiconductor IC technique.

The semiconductor ROM includes a memory array 1, in which memory cells constituting a known mask type ROM are arranged in the shape of a matrix. The memory array 1 is shown in greater detail in Figure 3.

Referring to Figure 3, the respective memory cells are formed at the intersection points between word lines $W_1 - W_4$ to be selected by an X decoder 3 and data lines $D_1 - D_4$ to be selected by a Y decoder 4. Memory MOSFETs are connected to the respective intersection points between the word lines and the data lines. Each of the memory MOSFETs

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has a threshold voltage which corresponds to an information to be retained. For example, information "1" is brought into correspondence with a low threshold voltage, and information "0" with a high threshold voltage. In Figure 3, for the sake of clarity there are omitted those memory MOSFETs of the memory MOSFETs connected to the intersection points between the word lines and the data lines which have the high threshold voltage, namely, which maintain their "off" states even when the word lines have been selected. In this manner, the write-down of the information into each memory cell is executed depending upon whether or not the MOSFET is substantially formed. MOSFETs $Q_{25}-Q_{30}$ are selectively formed, thereby to write information in. MOSFETs $Q_{21}-Q_{24}$ constitute column switches which are controlled by the Y decoder 4. The column switches are provided in order to supply a sense amplifier 5 with any one of data read out on the data lines D_1-D_4 . MOSFETs $Q_{31}-Q_{34}$ are load MOSFETs which determine read-out levels for the respective data lines. These load MOSFETs are depletion-mode MOSFETs whose gates and sources are short-circuited. A MOSFET Q_{35} is provided in order to lower the power dissipation of the ROM. While the chip is not selected, the MOSFET Q_{35} is turned "off", whereby ineffective currents to

flow through the load MOSFETs Q_{31} - Q_{34} can be cut off. A gate input control pulse ϕ_1 for the MOSFET Q_{35} is formed by a pulse generator 7 (figure 1) to be described later.

5 Referring back to Figure 1, the semiconductor ROM also includes an address buffer 2, which receives external address signals A_0 - A_n applied to a group of external terminals T_i and forms internal address signals $a_0, \overline{a_0} - a_i, \overline{a_i}$ of complementary levels.

10 The X decoder 3 referred to above forms a one word line select signal in response to the X address signal fed from the address buffer 2.

The Y decoder 4 referred to above forms a one data line select signal in response to the Y address
15 signal fed from the address buffer 2.

The sense amplifier 5 referred to above receives a read-out signal from one memory cell selected by the X decoder 3 and the Y decoder 4 and decides the level thereof.

20 The semiconductor ROM also includes an output buffer 6, which forms a read out data D_{OUT} and delivers it to an external terminal T_1 . A supply voltage V_{CC} is applied across to external terminals T_4 and T_3 , the terminal T_3 being earthed at GND.

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The pulse generator 7 referred to above receives a chip enable signal $\overline{CE}$ applied to an external terminal T_2 to generate pulses. The operation of the various circuits in the semiconductor ROM are controlled by these pulses. For example, the circuit blocks are controlled into their operating states only when the chip has been selected. Such a control reduces the amount of power dissipation in the ROM. In addition, when the chip is not selected, the address buffer 2 is brought into its non-operating state, whereby an address setting operation based on indefinite external address signals can be prevented.

Since the circuit blocks 1,2,3,4,5,6 and 7 described above are well known specific examples will not be illustrated.

In the above described semiconductor ROM, the following circuits are provided in order to relieve defect bits, in other words, to correct erroneous data read out from defective memory cells. Thus, the semiconductor ROM further includes a defect address memory 8 in which the address information of the defective (non-conforming) memory cells are written and retained. The write-down of the defect address information is executed by the use of fuse means and depend upon the presence or absence of the blowout thereof, as will be described later. A terminal t is a control terminal

which is used for the write-down. The write-down is carried out after the ROM has been manufactured on the semiconductor wafer and before it is packaged. Accordingly, the terminal t need not be an external
5 terminal which is connected to a package lead.

A comparator 9 is provided to receive the defect address information from the defect address memory 8 and the read-out address information from the address buffer 2 and compares them so as to detect
10 the coincidence thereof.

An exclusive OR circuit 10 is provided as an error correcting code circuit and is located between the sense amplifier 5 and the output buffer 6.

One input of the exclusive OR circuit 10
15 is supplied with a read-out signal from the sense amplifier 5, while the other input thereof is supplied with the output signal EC of the comparator 9 as an error correcting signal. The output signal of the exclusive OR circuit 10 is transmitted to the input
20 of the output buffer 6, and is delivered as the read-out data D_{OUT} from the external terminal T_1 .

Regarding the exclusive OR circuit 10, when the two input signal levels are non-coincident, the output signal level becomes "1" and conversely, when
25 the two input signal levels are coincident, the output signal level is at "0". Therefore, when the error

correction is performed, in other words, when the information is read out from the defective memory cell, the level of the coincidence detection output signal EC of the comparator 9 may be brought to the level "1". That is, under the condition that the level of the signal EC is "1", if the output signal level of the sense amplifier 5 (read-out output signal level) is "0", the exclusive OR circuit 10 will invert this output signal level into "1" and deliver the latter, and if the read-out output signal level of the sense amplifier 5 is "1", the circuit 10 will invert this output signal level into "0" and deliver the latter. Thus, the error correction can be made.

On the other hand, under the condition that the level of the signal EC is "0", if the output signal level of the sense amplifier 5 (read-out output signal level) is "0", the output signal level of the exclusive OR circuit 10 will become "0", and if the read-out output signal level of the sense amplifier 5 is "1", the output signal level of the exclusive OR circuit 10 will become "1". That is, in the case where the level of the signal EC is "0", the exclusive OR circuit 10 transmits the read-out output signal from the sense amplifier 5 to the output buffer 6 as it is.

Figure 2 shows the circuit arrangement of a practicable embodiment of the defect address memory

8 as well as the comparator 9.

As shown, this arrangement is constructed of n-channel MOSFETs (insulated-gate field effect transistors). Among these MOSFETs, load MOSFETs
5 Q_3 and Q_{11} are of the depletion mode, and the other MOSFETs are of the enhancement mode.

Firstly, a circuit C_0 enclosed with a two-dot chain line will be explained. The write-down of the address information of the defective memory cell is
10 executed depending upon the presence or absence of the blowout of a fuse F_1 . The fuse F_1 and MOSFET Q_2 are connected in series between the supply voltage V_{CC} and earth (GND) of the circuit. Whether or not the fuse F_1 is blown, is determined by the "on"/"off"
15 of the MOSFET Q_2 . In order to selectively control the "on"/"off" of this MOSFET Q_2 , there are provided a MOSFET Q_1 which receives the writing address signal $\overline{a_0}$, and the internal terminal t which is connected to the drain of the MOSFET Q_1 . The drain output of
20 this MOSFET Q_1 is applied to the gate of the MOSFET Q_2 . The MOSFET Q_2 is provided with a resistor R_1 in parallel, the resistor having a high value of resistance. The resistor R_1 is preferably constructed of a high resistance of polycrystalline silicon. The drain output
25 of the MOSFET Q_2 is transmitted, firstly to an inverter which consists of MOSFETs Q_3 and Q_4 . The output of

this inverter is transmitted to the gate of a transfer gate MOSFET Q_5 . The drain output of the MOSFET Q_2 is transmitted secondly to the gate of a transfer gate MOSFET Q_6 . The MOSFETs Q_5 and Q_6 are connected in series, and the address signals $\overline{a_0}$ and a_0 for comparing addresses are respectively applied through these MOSFETs Q_5 and Q_6 . The MOSFETs $Q_3 - Q_6$ described above and the MOSFETs $Q_7 - Q_{11}$ to be described later constitute the comparator 9 which detects the coincidence of comparison.

In the case where address information required for selecting a desired 1-bit memory cell are composed of the $(n + 1)$ bits of from a_0 ($\overline{a_0}$) to a_n ($\overline{a_n}$), circuits C_1 to C_n similar to the circuit C_0 are respectively provided for the address signals a_1 ($\overline{a_1}$) to a_n ($\overline{a_n}$) other than a_0 ($\overline{a_0}$), though no special restriction is intended.

A fuse F_2 is provided in order to write down whether or not the error correcting function is added. More specifically, with the address memory and comparator circuit shown in Figure 2, even if the particular memory cell is not defective, the level of the error correcting signal EC will be made "1" when the levels of the address signals $a_0 - a_n$ are "0". The fuse F_2 serves to prevent such a situation arising. The writing internal terminal t is connected to the

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gate of a MOSFET Q_{12} which is connected in series with the fuse F_2 . The MOSFET Q_{12} is provided with a parallel resistor R_2 having a high value of resistance.

The outputs of the circuits $C_0 - C_n$ provided in correspondence with the address signals $a_0 (\overline{a_0}) - a_n (\overline{a_n})$, and the drain output of the MOSFET Q_{12} are transmitted to the gates of the MOSFETs Q_7 to Q_{10} which constitute a NOR gate in the positive logic. The error correcting signal EC is derived from the output of this NOR gate.

The circuits of the arrangement shown in Figure 2 form one set, and relieve one defective memory cell. Accordingly, in order to relieve the defects of m memory cells, m sets of identical circuits are provided. Error correcting signals as described above and numbering m are transmitted to the exclusive OR circuit 10 through an OR circuit (not shown).

The write-down of the address information of the defective memory cell is performed as follows. First, all the bits of the memory array 1 shown in Figure 1 are read out and checked. That is, written data and read data are compared. When both do not agree, the address of the defective memory cell in which the particular data has been stored is detected. The address information $A_i (A_0 - A_n)$ of this defective memory cell are inputted from the plurality of external address terminals T_i . Amongst the

internal address signals of complementary levels
($a_0, \overline{a_0}$) - ($a_n, \overline{a_n}$) formed by the address buffer 2 in
accordance with the address information, the inverted
address signals $\overline{a_0} - \overline{a_n}$ are used as input data (write-
5 down address information) to the defect address
memory 8. That is, the inverted address signals
 $\overline{a_0} - \overline{a_n}$ are transmitted to the gates of the MOSFETs Q_1 .
In addition, a signal ϕ_p to be applied to the internal
terminal $\underline{t}$ is made the high level. At this time,
10 when the level of the write-down address signal $\overline{a_0}$
is "1" (high level), the MOSFET Q_1 turns "on" to turn
"off" the MOSFET Q_2 . Accordingly, no current flows
through the fuse F_1 , so that the fuse F_1 does not
blow. In contrast, when the level of the write-down
15 address signal $\overline{a_0}$ is "0" (low level), the MOSFET Q_1
turns "off" to turn "on" the MOSFET Q_2 . Therefore,
a current flows through the fuse F_1 , and the fuse
 F_1 blows.

The same applies to the other address
20 signals $\overline{a_1} - \overline{a_n}$.

Further, the MOSFET Q_{12} is turned "on" by
the high level of the signal ϕ_p applied to the
internal terminal $\underline{t}$, so that the fuse F_2 is
automatically blown.

25 In this way, the address information of the
defective memory cell (defect address information)

are written down.

As regards the address memory and comparator circuit in which the defect address information are not written down, the fuse F_2 is not blown. Therefore, 5 even when all the address signals $a_0 - a_n$ are "0", the MOSFET Q_{10} is "on", so that the level of the error correcting signal EC is not made "1".

At any time other than the write-down stated above, for example, at the read-out operation 10 of the ROM, the terminal t is held in its floating state. However, the MOSFET Q_2 is not turned "on" by the floating state. The reason is that a leakage current flowing through the MOSFET Q_1 renders the potential of the terminal t the earth potential, 15 which is maintained by a stray capacitance coupled to the terminal. The potential of the terminal t is also brought to earth potential when the address signal $\overline{a_0}$ is rendered to the high level to turn "on" the MOSFET Q_1 . In the read-out operation, when the 20 fuses F_1 and F_2 have been blown, the drain outputs of the MOSFETs Q_2 and Q_{12} become the low level "0" owing to the respective high values of resistance of the resistors R_1 and R_2 .

Now, in the case where the fuse F_1 is not 25 blown (when the address signal a_0 whose level is "0" has been written in the defect address memory shown

in Figure 2), the MOSFET Q_6 is "on" and the MOSFET Q_5 is "off". Accordingly, when the level of the read-out address signal a_0 is "1", this level "1" is transmitted to the gate of the MOSFET Q_7 through the MOSFET Q_6 so as to turn "on" the MOSFET Q_7 . On the other hand, when the level of the read-out address signal a_0 is "0", this level "0" is transmitted to the gate of the MOSFET Q_7 through the MOSFET Q_6 so as to turn "off" the MOSFET Q_7 .

In addition, in the case where the fuse F_1 has been blown (when the address signal a_0 whose level is "1" has been written in the defect address memory shown in Figure 2), the MOSFET Q_5 is "on" and the MOSFET Q_6 is "off". Accordingly, when the level of the read-out address signal a_0 is "0", the level "1" of the complementary signal $\overline{a_0}$ thereof is transmitted to the gate of the MOSFET Q_7 through the MOSFET Q_5 so as to turn "on" the MOSFET Q_7 . On the other hand, when the level of the read-out address signal a_0 is "1", the level "0" of the complementary signal $\overline{a_0}$ thereof is transmitted to the gate of the MOSFET Q_7 through the MOSFET Q_5 so as to turn "off" the MOSFET Q_7 .

Thus, according to the circuit described above, in the case where the level of the address signal a_0 stored in the defect address memory and that

of the read-out address signal a_0 are non-coincident, the MOSFET Q_7 can be turned "on". In the case where they are coincident, the MOSFET Q_7 can be turned "off".

When all the read-out address signals a_0 ($\overline{a_0}$)
5 - a_n ($\overline{a_n}$) have coincided with the address signals stored in the defect address memory 8, that is, when the MOSFETs Q_7 to Q_9 are "off" (Q_{10} is always "off" owing to the blowout of the fuse F_2), the selection of the defective memory cell is distinguished. As a result,
10 the comparator 9 brings the level of the error correcting signal EC to "1". The exclusive OR circuit 10 receives the signal EC of the level "1" and the information from the defective memory cell, and corrects the error of the information.

15 The operation of distinguishing whether or not the defective memory cell is selected, is performed in parallel with the operation of reading out the memory cell information. When the read output signal is to be delivered from the sense
20 amplifier 5, the error correcting signal EC has already been formed. In the error correcting system, the time delay of the read-out access corresponds only to one stage of the exclusive OR circuit, and this delay time is very small. Therefore, even
25 when the error correcting function is furnished, the speed of the read-out access can be enhanced.

In the case of employing the ECC circuit for the error correction, a large number of redundant bits are required. In contrast with the above described circuit construction, no redundant bit is necessary, so that the occupying area of the memory array is not increased.

Moreover, the circuit which corrects the error data upon detecting the fact of the address information of the defective memory cell is simpler in arrangement than the ECC circuit. Therefore, even when the error correcting function is furnished, the chip size of the ROM is not rendered large.

The read-out and check of all the bits of the memory array 1 and the write-down of the address information of the defective memory cells are carried out when the ROM has been finished up on the semiconductor wafer, and the terminal t for the write-down may be formed as the internal terminal in advance. Therefore, no external terminal is added when the ROM has been manufactured.

A number of modified or alternative constructions will now be briefly outlined.

The fuse may take the form of a conductor layer of aluminium which is formed on a semiconductor chip through an insulating film or a MOSFET which is broken down.

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The invention is applicable to ROMs other than the mask ROM. For example, it is also applicable to an EPROM (Erasable and Programmable ROM) employing memory devices into which information are electrically
5 written. Besides, it is applicable to PROMs of the fuse type, or the diode breakdown type. In the EPROM, it is also allowed to replace the fuse with the memory devices and to write the address information of defective memory cells into the memory devices.

10 Such a memory device has a source, a drain and a floating gate. When sufficient charge are stored in the floating gate, an inversion layer is formed between the source and the drain, and the source - drain path is steadily held in a conductive
15 state. Depending upon whether the source - drain path is conductive or non-conductive, an information for this memory device is written down. In order to erase the write-down information, the stored charges of the floating gate may be discharged by,
20 e.g. the irradiation of the floating gate with ultraviolet-rays.

Using such a memory device instead of the fuse, lower power dissipation for the write-down of the information can be achieved. The reason is
25 that the comparatively large current necessary to blow the fuse is not needed for the write-down into

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such a memory device.

It is also possible to utilize the mask ROM for the memory array and to write the address information of the defective memory cell by utilizing
5 the memory device stated above.

Further, in a ROM wherein n memory cells are appointed by one reading operation so as to obtain read-out data of n bits, defect bit positional information (digit) may be written down simultaneously
10 with the write-down of the address information of the defective memory cell, whereby n exclusive OR circuits are selectively operated on the basis of the defect bit positional information so as to correct only specified defect data.

15 The application of the above described circuit arrangements is not restricted only to the defective memory cells. In the case where undesired data has been written by mistake into a normal memory cell as to which write-down data and read-out data
20 coincide, such erroneous data can be corrected and then delivered out of the ROM.

CLAIMS.

1. A semiconductor ROM including:
 - (a) a memory array which includes a plurality of memory cells;
 - (b) a selection circuit which selects one of
5 the memory cells in response to input address signals;
 - (c) a detection circuit which is capable of detecting predetermined combinations of the input address signals and providing a detection signal to identify a defective memory cell in the memory array;
 - 10 (d) an output circuit which receives a one bit signal read out from said memory array and which delivers a signal of a logic level corresponding to said signal read out from said memory portion when no detection signal is provided from said detection circuit,
15 and a signal of a logic level not corresponding to said signal read out from said memory portion when a detection signal is provided from said detection circuit;whereby any erroneous data read out from a defective memory cell is inverted on the basis of
20 detecting signal to provide a corrected output signal.
2. A semiconductor ROM according to claim 1, wherein said detection circuit includes programmable address information memory elements.
3. A semiconductor ROM according to claim 2,
25 wherein said address information memory elements are fuses.



4. A semiconductor ROM according to Claim 3,
wherein said detection circuit includes: a plurality
of address comparators each comprising a fuse; a pair
of switching elements which are controlled "on" and
5 "off" complementarily by said fuse and which select
either opf the complementary address signals; and a
decoder circuit which receives outputs of said plurality
of address comparators.
5. A semiconductor ROM according to Claim 1,
10 wherein said output circuit includes an exclusive OR
circuit which receives the signal supplied from said
memory portion and the detection signal supplied from
said detection circuit.
6. A semiconductor ROM constructed and arranged
15 to operate substantially as herein described with
reference to and as illustrated in the accompanying
drawings.
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