

HK/MG PROCESS FLOWS FOR P-TYPE SEMICONDUCTOR DEVICES

ABSTRACT

The present disclosure provides semiconductor device structures with a first PMOS active region and a second PMOS active region provided within a semiconductor substrate. A silicon germanium channel layer (208, 308, 408, 508) is only formed over the second PMOS active region. Gate electrodes are formed over the first and second PMOS active regions, wherein the gate electrode over the second PMOS active region is formed over the silicon germanium channel (208, 308, 408, 508).

FIG. 3b