CLAIMS

1. A method of operating a ferroelectric memory cell, comprising:

virtually grounding a digit line that is in electronic communication with the ferroelectric memory cell;

discharging a first offset capacitor that is in electronic communication with a first switching component; and

transferring a stored charge of the ferroelectric memory cell to a sense capacitor through the first switching component, wherein the stored charge is transferred while the digit line is virtually grounded and after the first offset capacitor has discharged.

2. The method of claim 1, wherein discharging the first offset capacitor comprises:

activating the first switching component.

3. The method of claim 2, further comprising:

maintaining the digit line at virtual ground using the first switching component and based at least in part on discharging the first offset capacitor.

4. The method of claim 2, wherein the first switching component comprises a p-type field effect transistor (FET), and wherein a capacitance of the first offset capacitor is based at least in part on a threshold voltage of the p-type FET, the method further comprising:

applying the threshold voltage to a gate of the p-type FET based at least in part on discharging the first offset capacitor.

5. The method of claim 4, wherein transferring the stored charge of the ferroelectric memory cell to the sense capacitor comprises:

connecting a drain of the p-type FET with the sense capacitor through a second switching component;

selecting the ferroelectric memory cell; and

applying a voltage to a ferroelectric capacitor of the ferroelectric memory cell.

6. The method of claim 5, wherein selecting the ferroelectric memory cell comprises:

activating a selection component that is in electronic communication with the ferroelectric capacitor and the digit line, wherein the ferroelectric memory cell comprises the selection component and the ferroelectric capacitor.

7. The method of claim 4, wherein virtually grounding the digit line comprises:

virtually grounding the digit line through a second switching component, wherein the digit line is in electronic communication with a source of the p-type FET.

8. The method of claim 1, further comprising:

activating a sense amplifier that is in electronic communication with the sense capacitor; and

comparing a voltage of the sense capacitor to a reference voltage based at least in part on activating the sense amplifier.

9. The method of claim 1, further comprising:

virtually grounding a first terminal of the first offset capacitor through a second switching component, wherein the first switching component comprises a p-type field effect transistor (FET), and wherein the first terminal of the first offset capacitor is in electronic communication with a gate of the p-type FET and a drain of the p-type FET; and

charging a second terminal of the first offset capacitor while the first terminal is virtually grounded.

10. The method of claim 9, wherein discharging the first offset capacitor comprises:

electrically isolating the first terminal of the first offset capacitor from virtual ground; and

discharging the second terminal of the first offset capacitor, wherein the discharging transfers a stored charge from the first terminal of the first offset capacitor to the gate of the p-type FET.

11. The method of claim 10, wherein discharging the second terminal of the first offset capacitor comprises applying a zero voltage to the second terminal of the first offset capacitor.

12. The method of claim 9, further comprising:

electrically isolating the drain of the p-type FET from the gate of the p-type FET through a third switching component.

13. The method of claim 1, further comprising:

virtually grounding a reference digit line that is in electronic communication with a reference circuit;

discharging a second offset capacitor that is in electronic communication with a second switching component, wherein the first offset capacitor and the second offset capacitor are in electronic communication with a common signal line; and

transferring a stored charge of the reference circuit to a reference capacitor through the second switching component while the reference digit line is virtually grounded and after the first offset capacitor has discharged.

14. The method of claim 13, wherein the second switching component comprises a p-type field effect transistor (FET), the method further comprising:

applying a threshold voltage to a gate of the p-type FET based at least in part on discharging the second offset capacitor; and

maintaining the reference digit line at virtual ground while transferring the stored charge of the reference circuit to the reference capacitor.

15. An electronic memory apparatus, comprising:

a first p-type field effect transistor (FET);

a ferroelectric memory cell in electronic communication with a source of the first p-type FET through a digit line;

a sense capacitor in electronic communication with a drain of the first p-type FET through a first switching component; and

a first terminal of a first offset capacitor in electronic communication with a gate of the first p-type FET.

16. The electronic memory apparatus of claim 15, further comprising:

a sense amplifier in electronic communication with the sense capacitor.

17. The electronic memory apparatus of claim 15, wherein the drain of the first p-type FET is in electronic communication with the gate of the first p-type FET through a second switching component.

18. The electronic memory apparatus of claim 15, further comprising:

a third switching component, wherein the first terminal of the first offset capacitor and the gate of the first p-type FET are in electronic communication to a virtual ground through the third switching component.

19. The electronic memory apparatus of claim 15, further comprising:

a voltage source in electronic communication with a second terminal of the first offset capacitor.

20. The electronic memory apparatus of claim 15, wherein the digit line is in electronic communication with a virtual ground through a fourth switching component.

21. The electronic memory apparatus of claim 15, further comprising:

a reference circuit in electronic communication with a reference capacitor through a second p-type FET, wherein the reference capacitor is in electronic communication with a sense amplifier; and

a second offset capacitor in electronic communication with a gate of the second p-type FET, wherein the first offset capacitor and the second offset capacitor are in electronic communication with a common signal line, and wherein the first p-type FET and the second p-type FET have different threshold voltages.

22. The electronic memory apparatus of claim 21, wherein the reference circuit comprises one or more ferroelectric memory cells.

23. An electronic memory apparatus, comprising:

a ferroelectric memory cell that comprises a ferroelectric capacitor and a selection component;

a sense amplifier in electronic communication with the selection component through a digit line;

a first switching component in electronic communication with the digit line and the sense amplifier;

an offset capacitor in electronic communication with the first switching component; and

a controller in electronic communication with the selection component, the sense amplifier, and the offset capacitor, wherein the controller is operable to:

operate a second switching component to virtually ground the digit line;

discharge the offset capacitor to transfer charge to the first switching component while the digit line is grounded; and

activate the sense amplifier after the offset capacitor has discharged.

24. The electronic memory apparatus of claim 23, wherein the controller is operable to:

activate the selection component to select the ferroelectric memory cell; and

operate the ferroelectric capacitor of the ferroelectric memory cell to charge a sense capacitor based at least in part on selecting the ferroelectric memory cell.

25. The electronic memory apparatus of claim 23, wherein the controller is operable to:

compare a voltage of a sense capacitor to a voltage of a reference capacitor to read a logic value of the ferroelectric memory cell, wherein the sense capacitor is in electronic communication with the sense amplifier.