

ABSTRACT

A memory device includes a row decoder, a column decoder, and a repair control circuit, which is configured to: (i) compare a row address with a stored failed row address, (ii) compare a column address with a stored failed column address, (iii) control the row decoder to activate the at least one of a plurality of redundancy word lines when the row address corresponds to the failed row address, and (iv) control the column decoder to activate at least one of a plurality of redundancy bit lines when the column address corresponds to the failed column address. The repair control circuit varies a repair unit according to an address input during a repair operation.

FIG. 1